# SN74CBTLV3383 Low-Voltage 10-Bit FET Bus-Exchange Switch

## 1 Features

- 5-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- $I_{off}$ Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A
  - 200-V Machine Model (A115-A)

## 2 Applications

- Gaming
- Rack Server
- Communication Board

## 3 Description

The SN74CBTLV3383 provides ten bits of high-speed bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device operates as a 10-bit bus switch or as a 5-bit bus exchanger, which provides swapping of the A and B pairs of signals. The bus-exchange function is selected when BX is high, and $\overline{BE}$ is low.

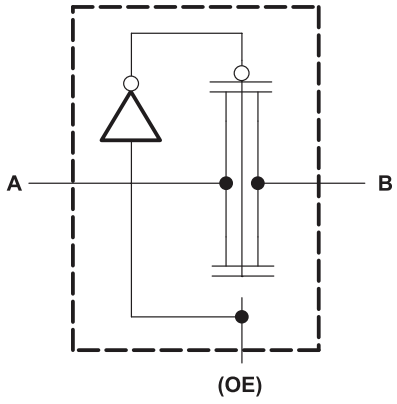
This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74CBTLV3383 | QSOP − DBQ | 8.65 mm x 3.90 mm |
| | SOIC − DW | 15.4 mm x 7.50 mm |
| | TSSOP − PW | 7.80 mm x 4.40 mm |
| | TVSOP − DGV | 5.00 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic, Each FET Switch**



# Table of Contents



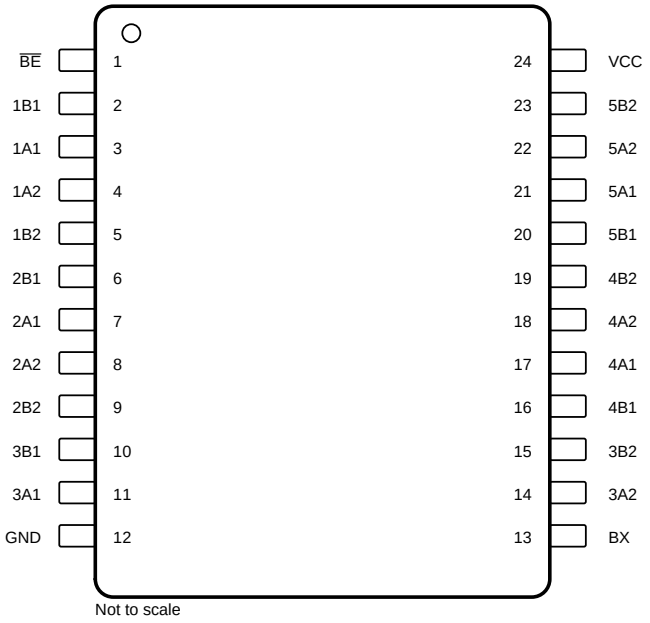
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision G (October 2003) to Revision H | Page |
|---|---|
| • Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. | 1 |

# 5 Pin Configuration and Functions

**DBQ, DGV, DW, OR PW Package**
**24-Pin**
**Top View**




Not to scale

## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $\overline{BE}$ | 1 | I | Active low enable: When this pin is high, all switches are turned off. When this pin is low, BX pin controls the signal path selection. |
| 1B1 | 2 | I/O | Signal path. Can be an input or output |
| 1A1 | 3 | I/O | Signal path. Can be an input or output |
| 1A2 | 4 | I/O | Signal path. Can be an input or output |
| 1B2 | 5 | I/O | Signal path. Can be an input or output |
| 2B1 | 6 | I/O | Signal path. Can be an input or output |
| 2A1 | 7 | I/O | Signal path. Can be an input or output |
| 2A2 | 8 | I/O | Signal path. Can be an input or output |
| 2B2 | 9 | I/O | Signal path. Can be an input or output |
| 3B1 | 10 | I/O | Signal path. Can be an input or output |
| 3A1 | 11 | I/O | Signal path. Can be an input or output |
| GND | 12 | P | Ground (0V) reference |
| BX | 13 | I | Controls state of switches |
| 3A2 | 14 | I/O | Signal path. Can be an input or output |
| 3B2 | 15 | I/O | Signal path. Can be an input or output |
| 4B1 | 16 | I/O | Signal path. Can be an input or output |
| 4A1 | 17 | I/O | Signal path. Can be an input or output |
| 4A2 | 18 | I/O | Signal path. Can be an input or output |
| 4B2 | 19 | I/O | Signal path. Can be an input or output |
| 5B1 | 20 | I/O | Signal path. Can be an input or output |
| 5A1 | 21 | I/O | Signal path. Can be an input or output |
| 5A2 | 22 | I/O | Signal path. Can be an input or output |
| 5B2 | 23 | I/O | Signal path. Can be an input or output |
| $V_{CC}$ | 24 | P | Positive power supply. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | –0.5 | 4.6 | V |
| $V_I$ | Input voltage range | –0.5 | 4.6 | V |
| | Continuous channel current . | | 128 | mA |
| $I_{IK}$ | Input clamp current, $V_{I/O} < 0$ | | –50 | mA |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.3 | | 3.6 | V |
| $V_{IH}$ | High-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | | V |
| $V_{IL}$ | Low-level control input voltage | $V_{CC}$ = 2.3 V to 2.7 V | | | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | | 0.8 | V |
| $T_A$ | Operating free-air temperature | | –40 | | 85 | °C |

(1) All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74CBTLV3383 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | DBQ (QSOP) | DVG (TVSOP) | DW (SPIC) | PW (TSSOP) | |
| | | 24 PINS | 24 PINS | 24 PINS | 24 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 86.6 | 105.6 | 66.6 | 90.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 40.5 | 36.9 | 36.7 | 34.12 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 40.8 | 51.1 | 36.6 | 45.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 7.8 | 2.6 | 13.1 | 2.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 40.4 | 50.6 | 36.4 | 44.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | n/a | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Clamp current | $V_{CC}$ = 3 V | $I_I$ = –18 mA | | | | –1.2 | V |
| $I_I$ | Input current | $V_{CC}$ = 3.6 V | $V_I$ = $V_{CC}$ or GND | | –1 | | 1 | µA |
| $I_{off}$ | Partial power down mode operation | $V_{CC}$ = 0 V | $V_I$ or $V_{IO}$ = 0 to 3.6 V | | | | 10 | µA |
| $I_{CC}$ | Supply current | $V_{CC}$ = 3.6 | $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | | | | 10 | µA |
| $\Delta I_{CC}$(2) | Supply current - Control inputs | $V_{CC}$ = 3.6 V | One input at 3V | Other inputs at VCC or GND | | | 300 | µA |
| $C_I$ | Input Capacitance - Control inputs | $V_I$ = 3 V or 0 | | | | 3.5 | | pF |
| $C_{IO(OFF)}$ | Input to output capacitance | $V_O$ = 3 V or 0 | $\overline{BE}$ = $V_{CC}$ | | | 13.5 | | pF |
| $r_{(on)}$(3) | On-state resistance | $V_{CC}$ = 2.3 V TYP at VCC = 2.5 V | $V_I$ = 0 | $I_I$ = 64 mA | | 5 | 8 | Ω |
| | | | | $I_I$ = 24 mA | | 5 | 8 | Ω |
| | | | $V_I$ = 1.7 V | $I_I$ = 15 mA | | 27 | 40 | Ω |
| | | $V_{CC}$ = 3 V | $V_I$ = 0 | $I_I$ = 64 mA | | 5 | 7 | Ω |
| | | | | $I_I$ = 24 mA | | 5 | 7 | Ω |
| | | | $V_I$ = 2.4 V | $I_I$ = 15 mA | | 10 | 15 | Ω |

(1) All typical values are at $V_{CC}$ = 3.3 V (unless otherwise noted), $T_A$ = 25°C
(2) This is the increase in supply current for each input that is at the specified voltage level, rather than $V_{CC}$ or GND.
(3) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

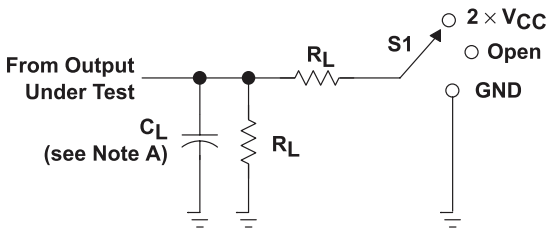
## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | FROM (INPUT) | TO (OUTPUT) | MIN | MAX | MIN | MAX | |
| $t_{pd}$ (1) | Propagation delay time | A or B | Bo or A | | 0.15 | | 0.25 | ns |
| $t_{pd}$ | Propagation delay time | BX | A or B | 1.5 | 5.8 | 1.5 | 4.7 | ns |
| $t_{en}$ | Enable time | $\overline{BE}$ | A or B | 1.5 | 5.3 | 1.5 | 4.7 | ns |
| $t_{dis}$ | Disable time | $\overline{BE}$ | A or B | 1 | 6 | 1 | 6 | ns |

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## 7 Parameter Measurement Information




| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$<br>$t_{PLZ}/t_{PZL}$<br>$t_{PHZ}/t_{PZH}$ | Open<br>$2 \times V_{CC}$<br>GND |

| $V_{CC}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|
| 2.5 V ±0.2 V | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ±0.3 V | 50 pF | 500 Ω | 0.3 V |

**Figure 1. Load Current**

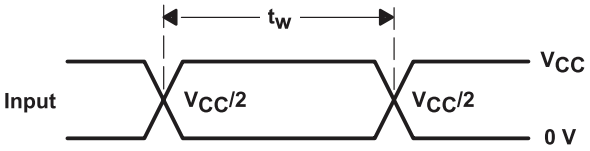



**Figure 2. Voltage Waveforms Pulse Duration**

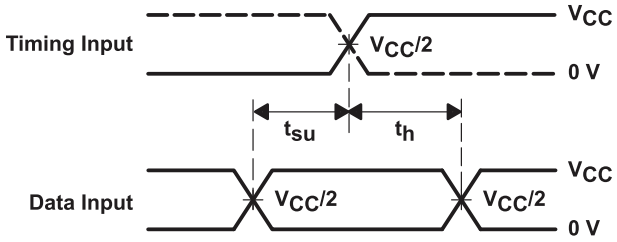



**Figure 3. Voltage Waveforms Setup and Hold Times**

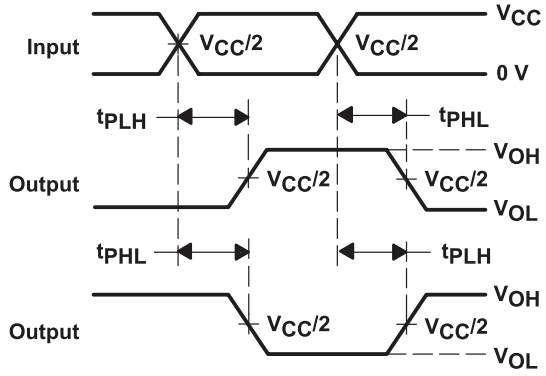



**Figure 4. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs**

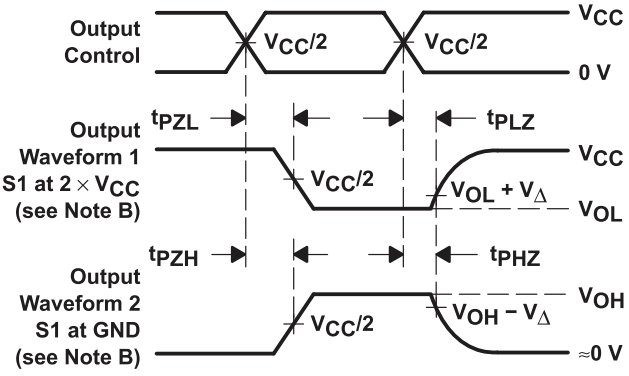



**Figure 5. Voltage Waveforms Enable And Disable Times Low- and High-Level Enabling**

Notes:

A. $C_L$ includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.

D. The outputs are measured one at a time with one transition per measurement.

E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.

F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.

G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

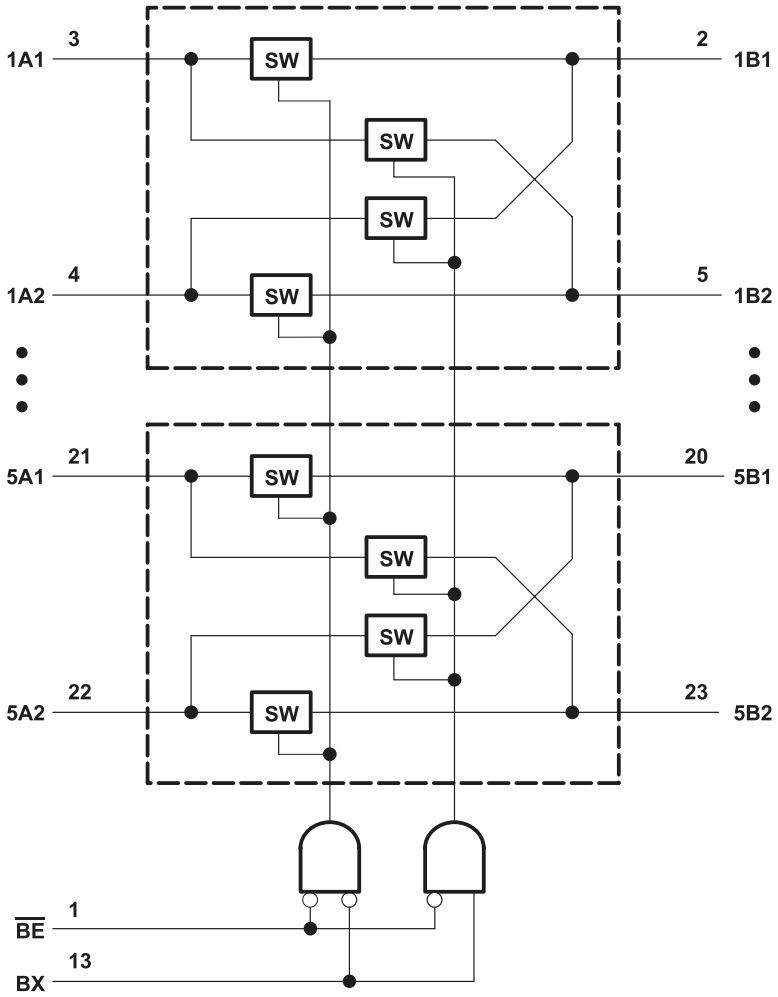
H. H. All parameters and waveforms are not applicable to all devices.

# 8 Detailed Description

## 8.1 Overview

The SN74CBTLV3383 device is a 10-bit high-speed bus exchange FET switch. The low ONstate resistance of the switch allows connections to be made with minimal propagation delay. The select (BX) input controls the data flow. The FET multiplexers and demultiplexers are disabled when the output-enable (BE) input is high. This device is fully specified for partial-power-down applications using Ioff. The Ioff feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off. To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

Bidirectional Operation

The SN74CBTLV3383 conducts equally well from source (xA1, xA2) to drain (xB1,xB2). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

Rail-to-rail switching

The SN74CBTLV3383 will support signals on the I/O path across the full supply range 0 to $V_{CC}$

## 8.4 Device Functional Modes

Shows the functional modes of the SN74CBTLV3383.

**Table 1. Function Table**

| INPUTS | | INPUTS–OUTPUTS | |
|---|---|---|---|
| $\overline{BE}$ | BX | 1A1–5A1 | 1A2-5A2 |
| L | L | 1B1–5B1 | 1B2–5B2 |
| L | H | 1B2–5B2 | 1B1–5B1 |
| H | X | Z | Z |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74CBTLV3383 device operates as a 10-bit bus switch or as a 5-bit bus exchanger, which provides swapping of the A and B pairs of signals. The bus-exchange function is selected when BX is high, and BE is low. The application shown here is a 5-bit bus being multiplexed between two devices. The BE and BX pins are used to control the chip from the bus controller. This is a generic example, and could apply to many situations.

## 9.2 Typical Application

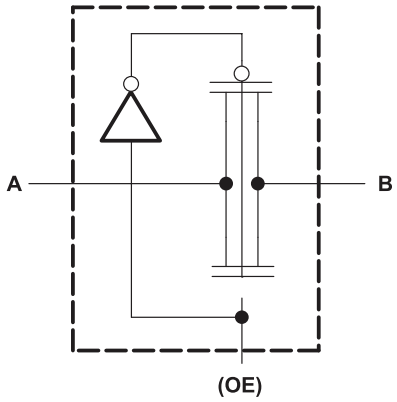



**Figure 6. Simple Schematic**

### 9.2.1 Design Requirements

1. Recommended Input Conditions:
   - For specified high and low levels, see $V_{IH}$ and $V_{IL}$ in Recommended Operating Conditions.
   - Inputs and outputs are overvoltage tolerant slowing them to go as high as 4.6 V at any valid VCC.
2. Recommended Output Conditions:
   - Load currents should not exceed ±128 mA per channel.
3. Frequency Selection Criterion:
   - Maximum frequency tested is 200 MHz.

### 9.2.2 Detailed Design Procedure

The SN74CBTLV3383 can be operated without any external components. All inputs signals passing through the switch must fall within the recommend operating conditions of the SN74CBTLV3383 including signal range and continuous current. For this design example, with a supply of 3.3 V, the signals can range from 0 V to 3.3 V when the device is powered. The max continuous current can be 128 mA.

## 10 Power Supply Recommendations

The SN74CBTLV3383 operates across a wide supply range of 2.3 V to 3.6 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Power-supply bypassing improves noise margin and prevents switching noise propagation from the VDD supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from VDD to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

# 11 Layout

## 11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

## 11.2 Layout Example

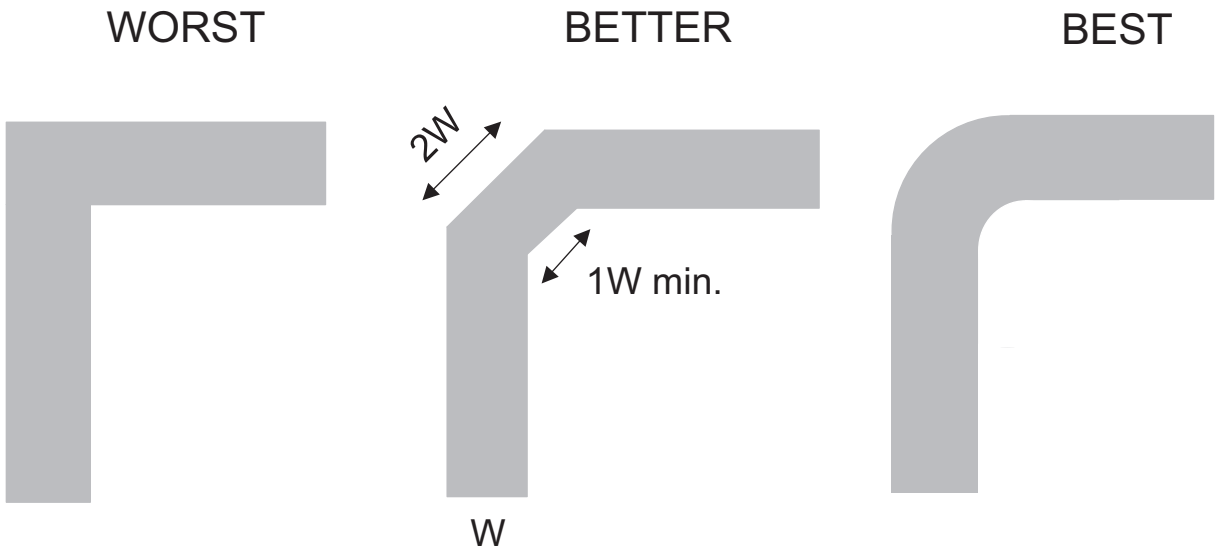



**Figure 7. Example Layout**

# 12 Device and Documentation Support

## 12.1 Documentation Support

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74CBTLV3383DBQR | ACTIVE | SSOP | DBQ | 24 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CBTLV3383 | Samples |
| SN74CBTLV3383DGVR | ACTIVE | TVSOP | DGV | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CL383 | Samples |
| SN74CBTLV3383DW | ACTIVE | SOIC | DW | 24 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBTLV3383 | Samples |
| SN74CBTLV3383DWE4 | ACTIVE | SOIC | DW | 24 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBTLV3383 | Samples |
| SN74CBTLV3383DWR | ACTIVE | SOIC | DW | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBTLV3383 | Samples |
| SN74CBTLV3383PW | ACTIVE | TSSOP | PW | 24 | 60 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CL383 | Samples |
| SN74CBTLV3383PWG4 | ACTIVE | TSSOP | PW | 24 | 60 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CL383 | Samples |
| SN74CBTLV3383PWR | ACTIVE | TSSOP | PW | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CL383 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

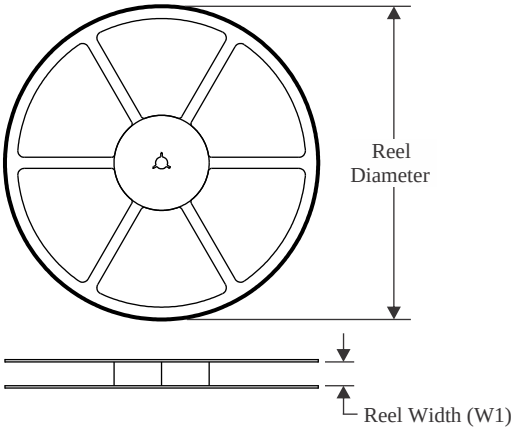
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

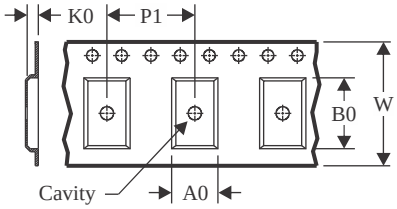
**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

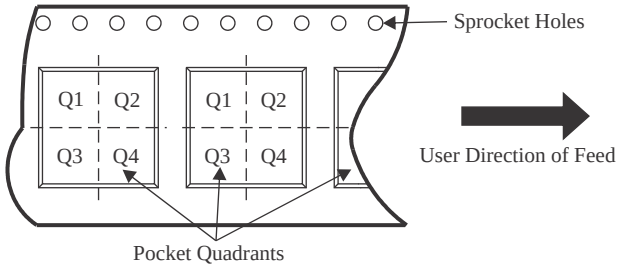



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

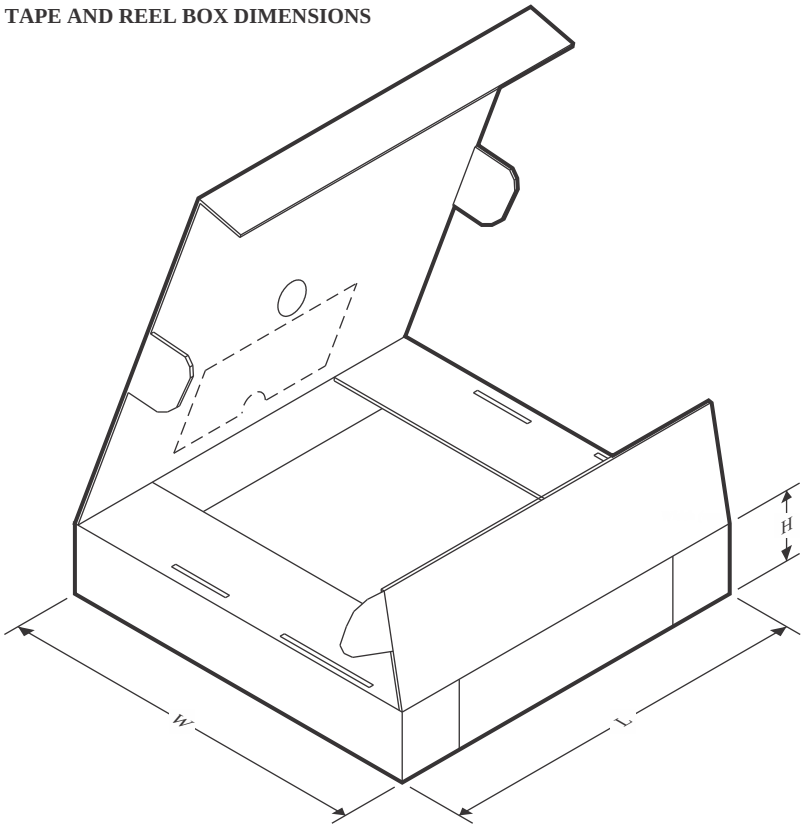
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74CBTLV3383DBQR | SSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74CBTLV3383DGVR | TVSOP | DGV | 24 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74CBTLV3383DWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74CBTLV3383PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

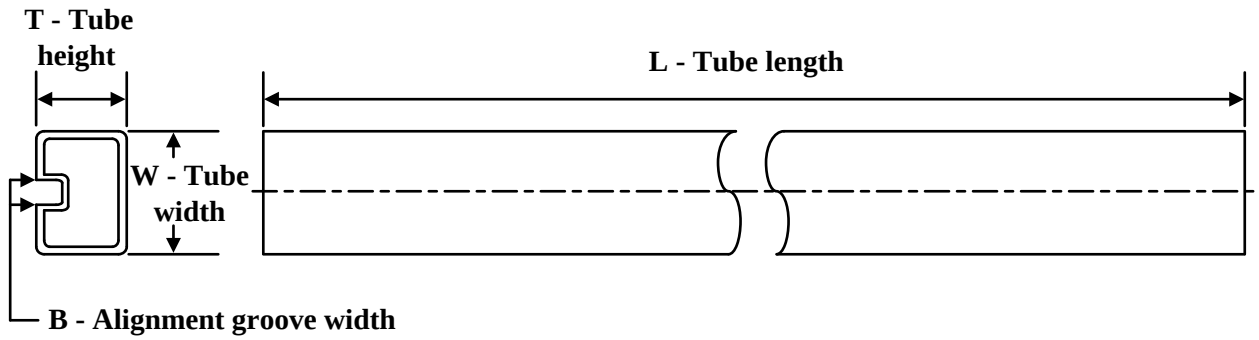
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74CBTLV3383DBQR | SSOP | DBQ | 24 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74CBTLV3383DGVR | TVSOP | DGV | 24 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74CBTLV3383DWR | SOIC | DW | 24 | 2000 | 350.0 | 350.0 | 43.0 |
| SN74CBTLV3383PWR | TSSOP | PW | 24 | 2000 | 356.0 | 356.0 | 35.0 |

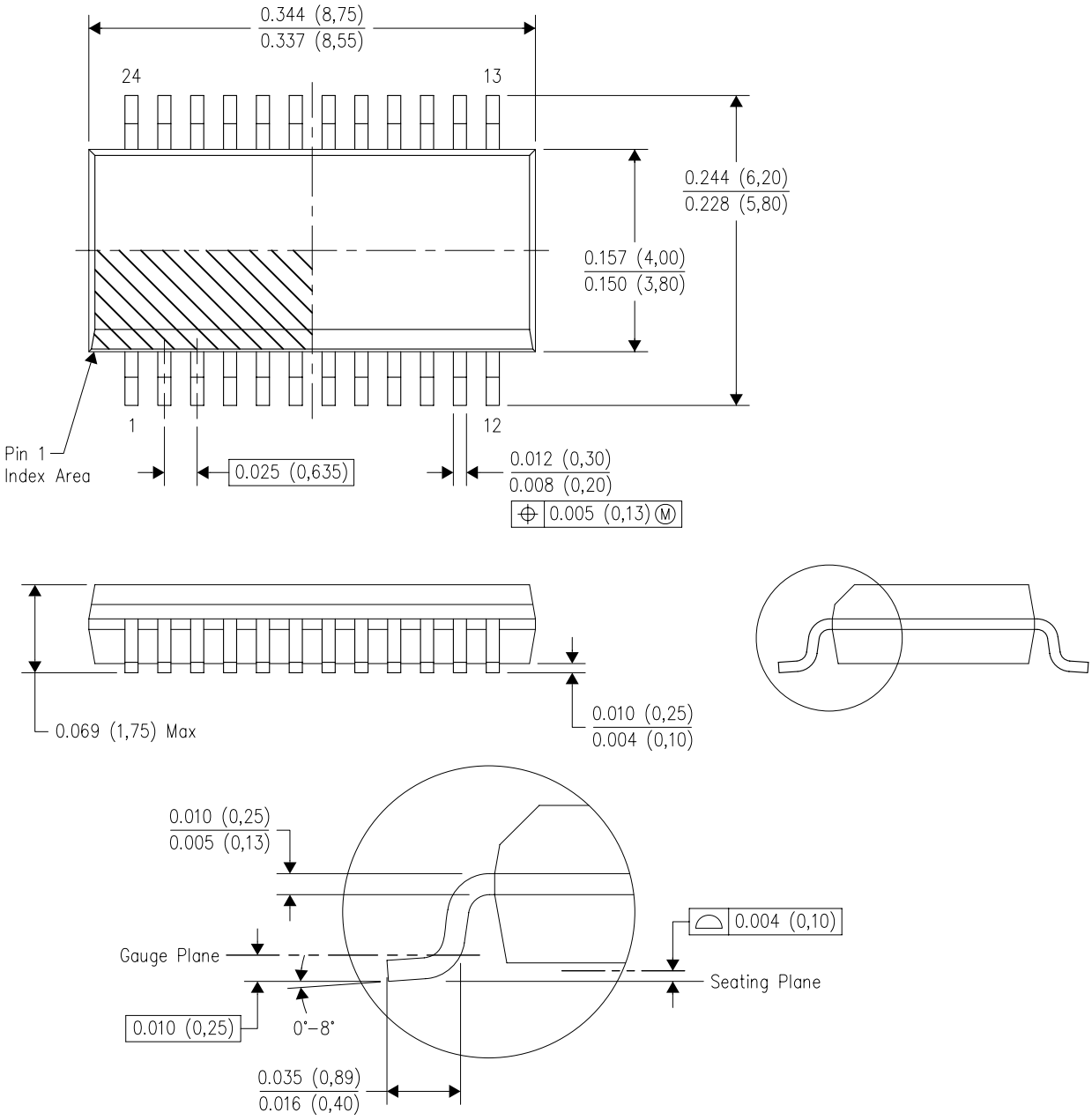
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74CBTLV3383DW | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74CBTLV3383DWE4 | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74CBTLV3383PW | PW | TSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |
| SN74CBTLV3383PWG4 | PW | TSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



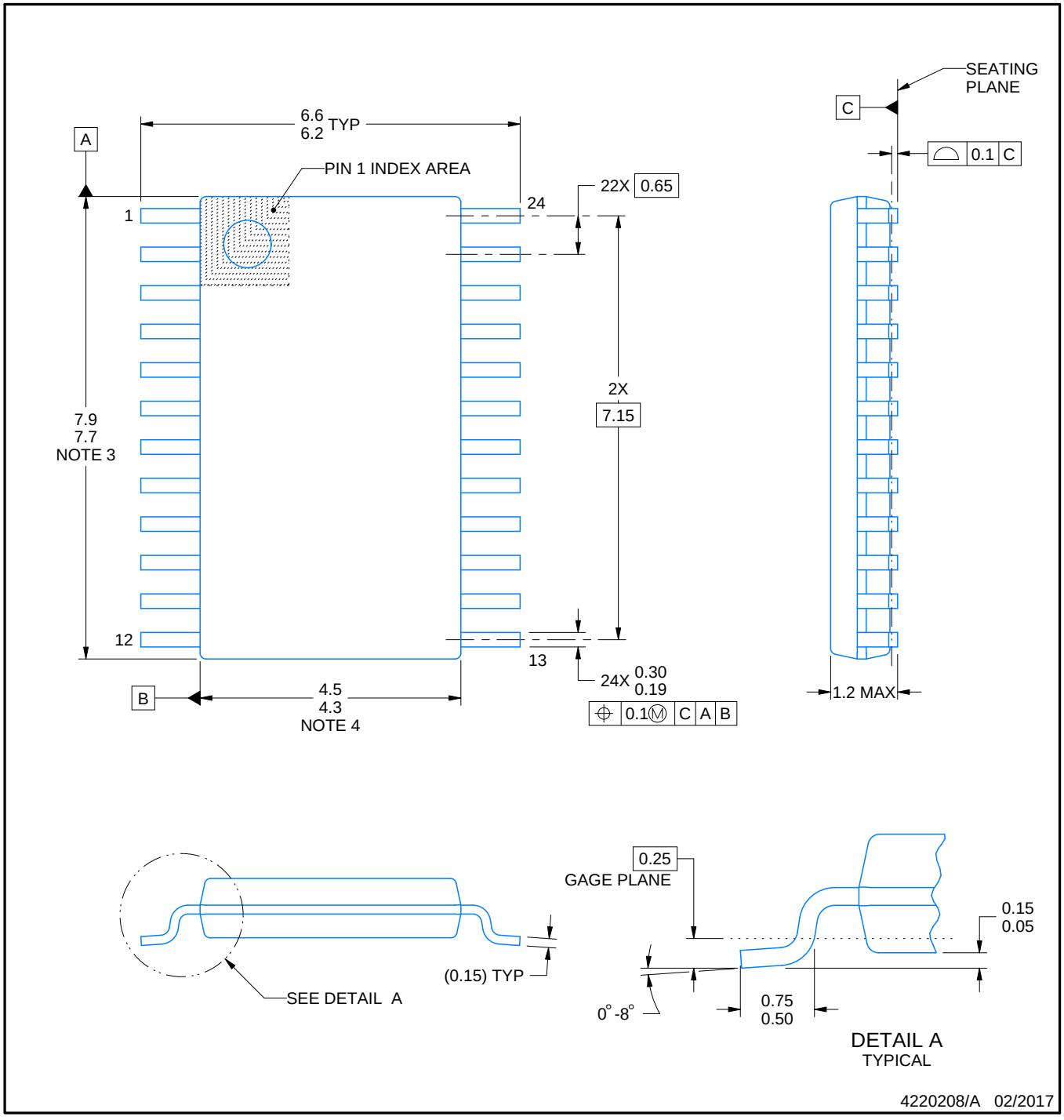

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

# PACKAGE OUTLINE

## PW0024A

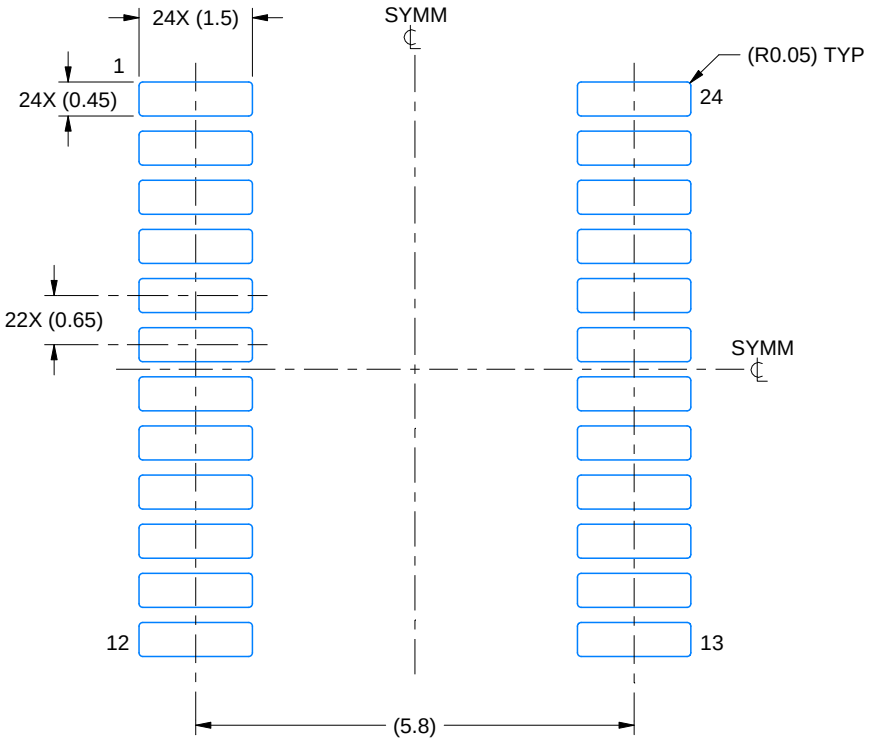
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

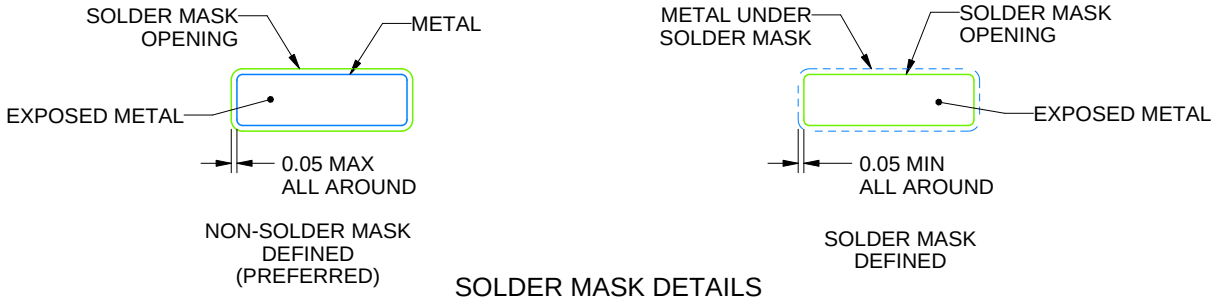



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

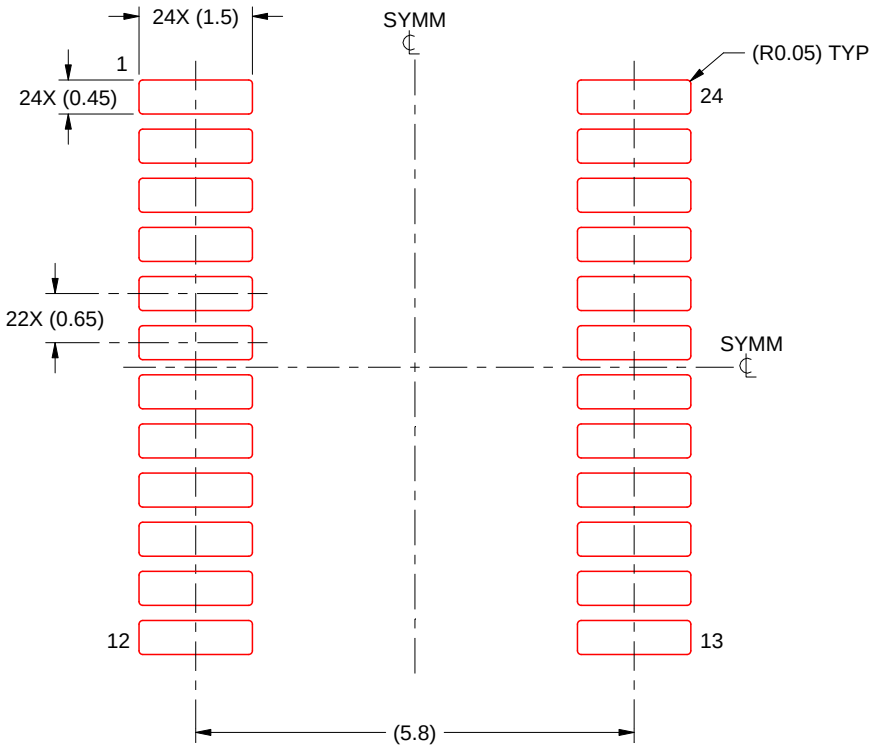



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

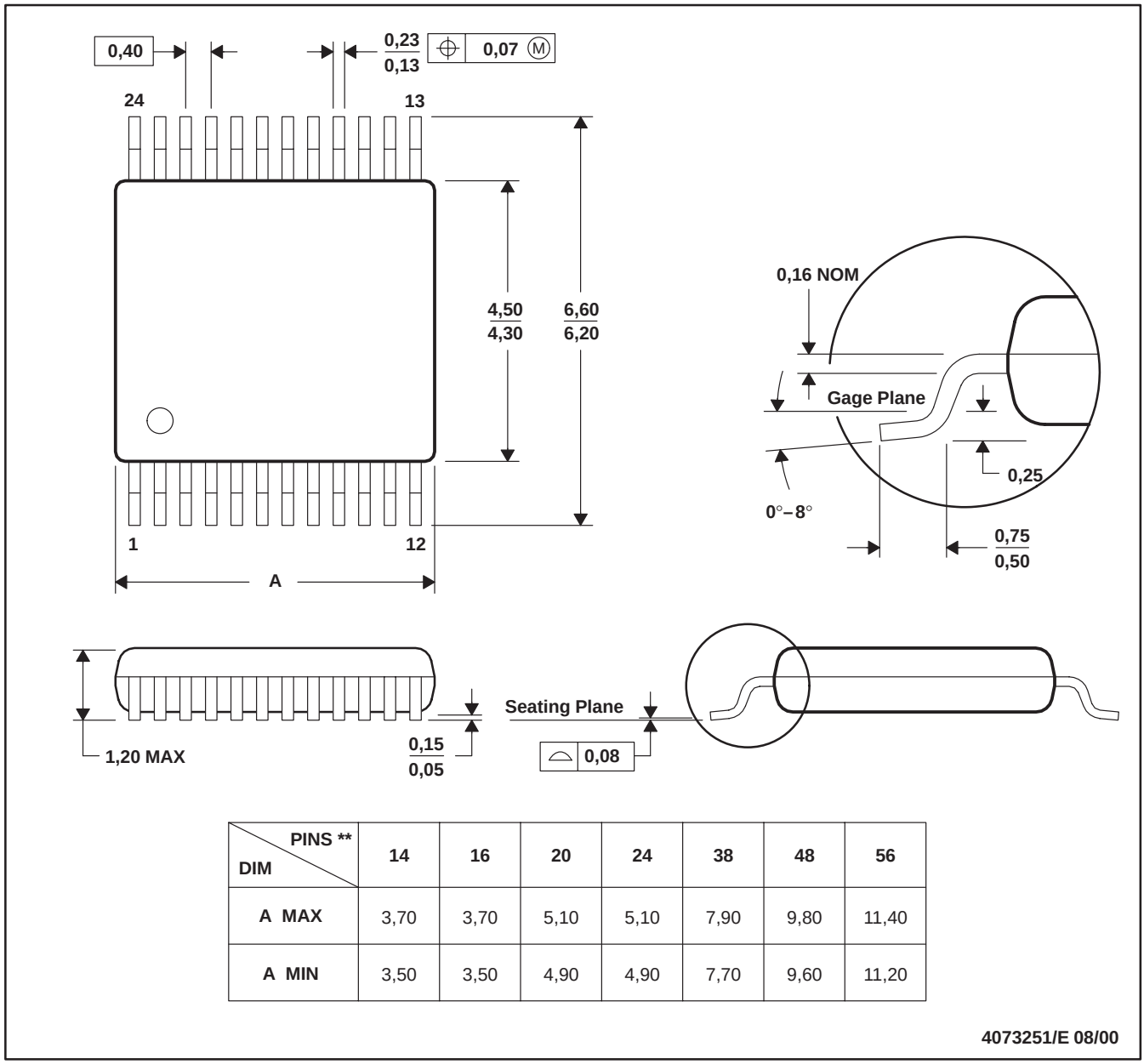
4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

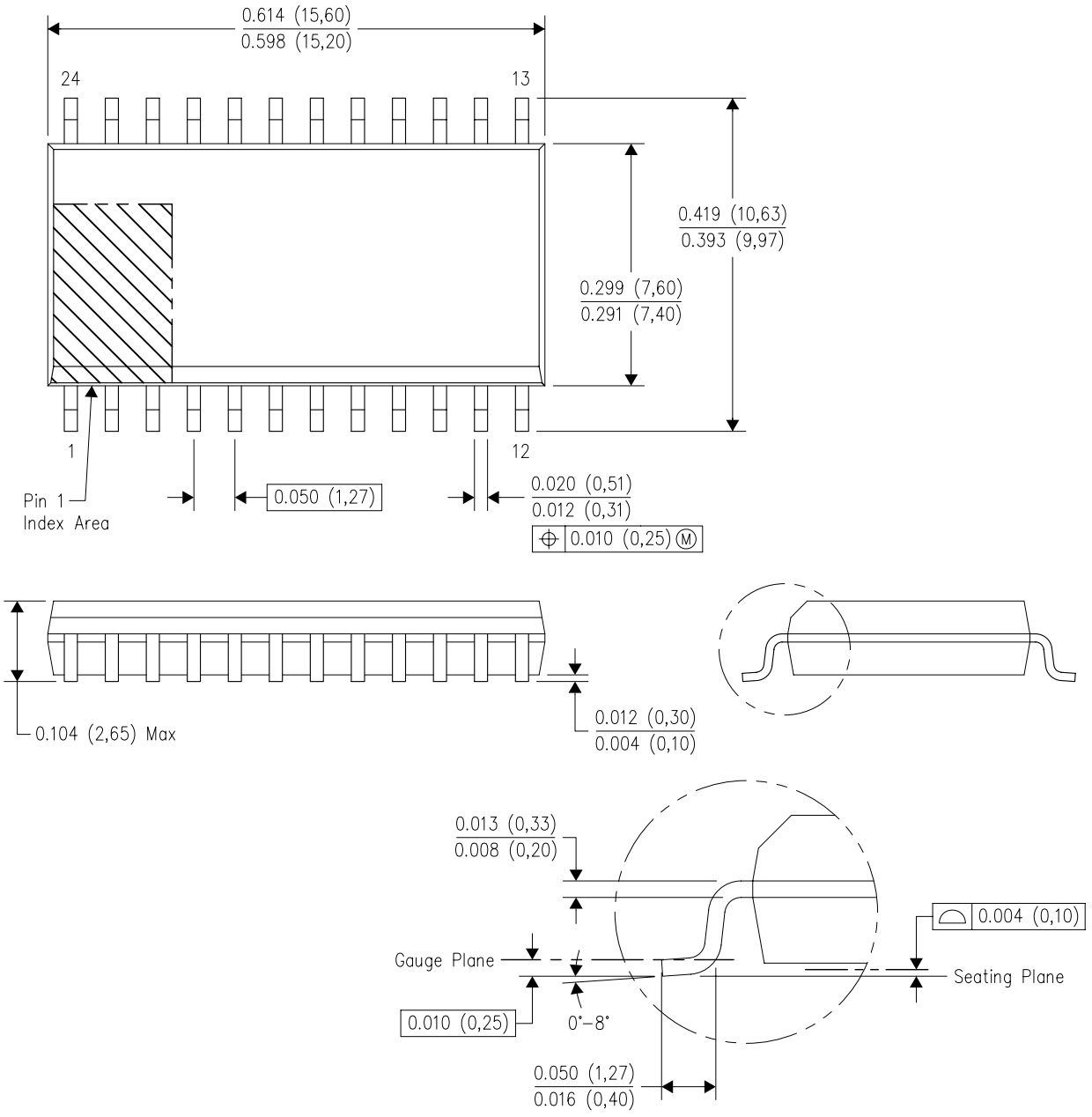



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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