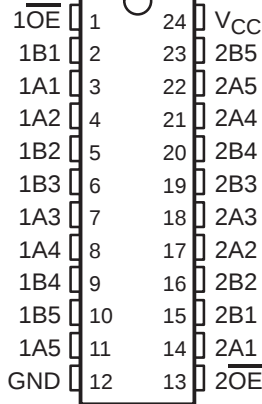


SN54CBTD3384, SN74CBTD3384 10-BIT FET BUS SWITCHES WITH LEVEL SHIFTING

SCDS025R – MAY 1995 – REVISED JANUARY 2004

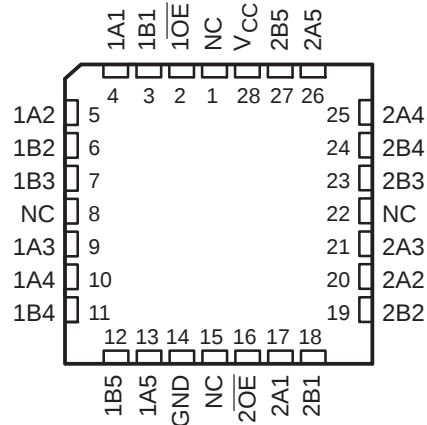
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

SN54CBTD3384 . . . JT OR W PACKAGE
SN74CBTD3384 . . . DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



- Designed to Be Used in Level-Shifting Applications

SN54CBTD3384 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'CBTD3384 devices provide ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switches allows connections to be made without adding propagation delay. A diode to V_{CC} is integrated on the die to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

These devices are organized as two 5-bit switches with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the switch is on, and port A is connected to port B. When $\overline{OE}$ is high, the switch is open, and the high-impedance state exists between the two ports.

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74CBTD3384DW	CBTD3384
		Tape and reel	SN74CBTD3384DWR	
	SSOP – DB	Tape and reel	SN74CBTD3384DBR	CC384
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBTD3384DBQR	CBTD3384
	TSSOP – PW	Tube	SN74CBTD3384PW	CC384
		Tape and reel	SN74CBTD3384PWR	
–55°C to 125°C	TVSOP – DGV	Tape and reel	SN74CBTD3384DGVR	CC384
	CDIP – JT	Tube	SNJ54CBTD3384JT	SNJ54CBTD3384JT
	CFP – W	Tube	SNJ54CBTD3384W	SNJ54CBTD3384W
	LCCC – FK	Tube	SNJ54CBTD3384FK	SNJ54CBTD3384FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

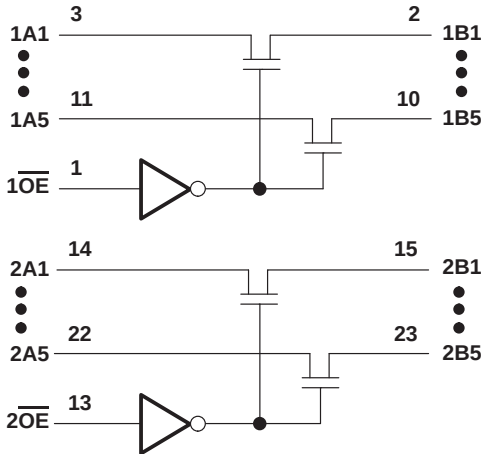
SN54CBTD3384, SN74CBTD3384 10-BIT FET BUS SWITCHES WITH LEVEL SHIFTING

SCDS025R – MAY 1995 – REVISED JANUARY 2004

FUNCTION TABLE
(each 5-bit bus switch)

INPUTS		INPUTS/OUTPUTS	
1OE	2OE	1B1-1B5	2B1-2B5
L	L	1A1-1A5	2A1-2A5
L	H	1A1-1A5	Z
H	L	Z	2A1-2A5
H	H	Z	Z

logic diagram (positive logic)



Pin numbers shown are for the DB, DBQ, DGV, DW, JT, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	63°C/W
DBQ package	61°C/W
DGV package	86°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54CBTD3384, SN74CBTD3384 10-BIT FET BUS SWITCHES WITH LEVEL SHIFTING

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recommended operating conditions (see Note 3)

		SN54CBTD3384		SN74CBTD3384		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level control input voltage	2		2		V
V _{IL}	Low-level control input voltage		0.8		0.8	V
T _A	Operating free-air temperature	–55	125	–40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54CBTD3384			SN74CBTD3384			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA			–1.2			–1.2	V
V _{OH}		See Figure 2							
I _I		V _{CC} = 5.5 V, V _I = 5.5 V or GND			±1			±1	μA
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND			1.5			1.5	mA
ΔI _{CC} ‡	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			2.5			2.5	mA
C _i	Control inputs	V _I = 3 V or 0			3			3	pF
C _{io} (OFF)		V _O = 3 V or 0, $\overline{\text{OE}}$ = V _{CC}			3.5			3.5	pF
r _{on} §		V _{CC} = 4.5 V			I _I = 64 mA			I _I = 7	Ω
					I _I = 30 mA			I _I = 7	
					V _I = 2.4 V, I _I = 15 mA			35 50	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54CBTD3384		SN74CBTD3384		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A		0.25		0.25	ns
t _{en}	$\overline{\text{OE}}$	A or B	2.2	9.7	2.3	7	ns
t _{dis}	$\overline{\text{OE}}$	A or B	1.5	8.6	1.7	5.3	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

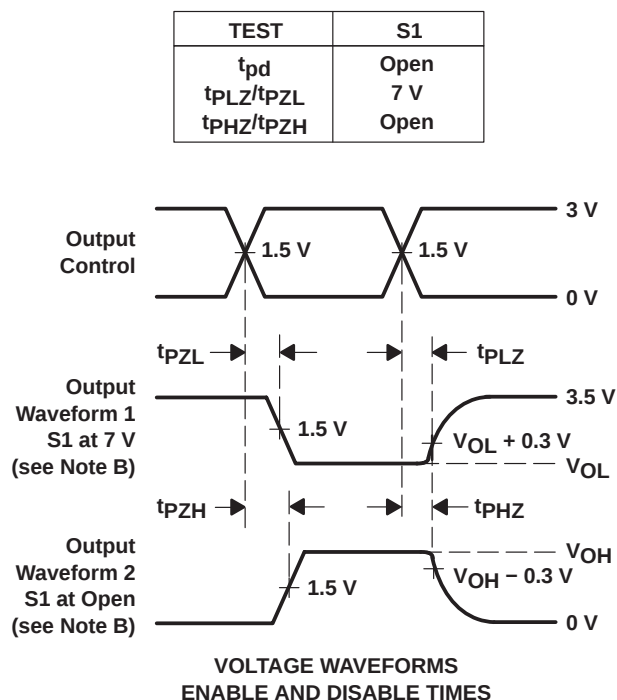
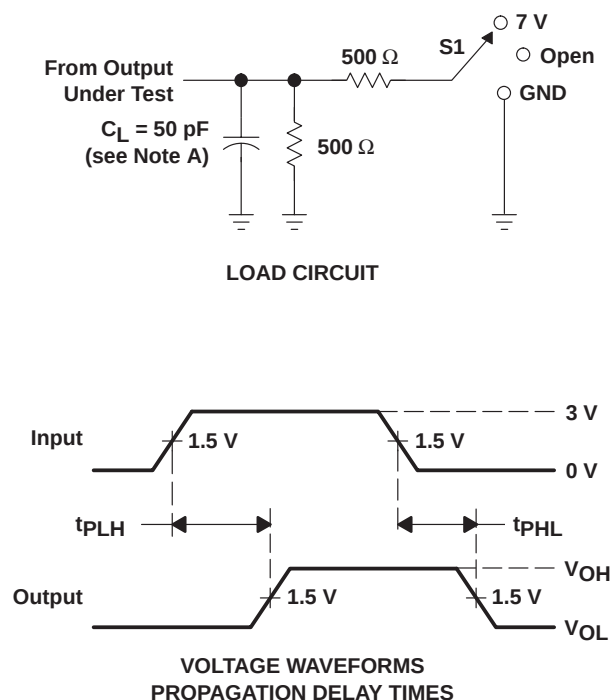
SN54CBTD3384, SN74CBTD3384

10-BIT FET BUS SWITCHES

WITH LEVEL SHIFTING

SCDS025R – MAY 1995 – REVISED JANUARY 2004

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

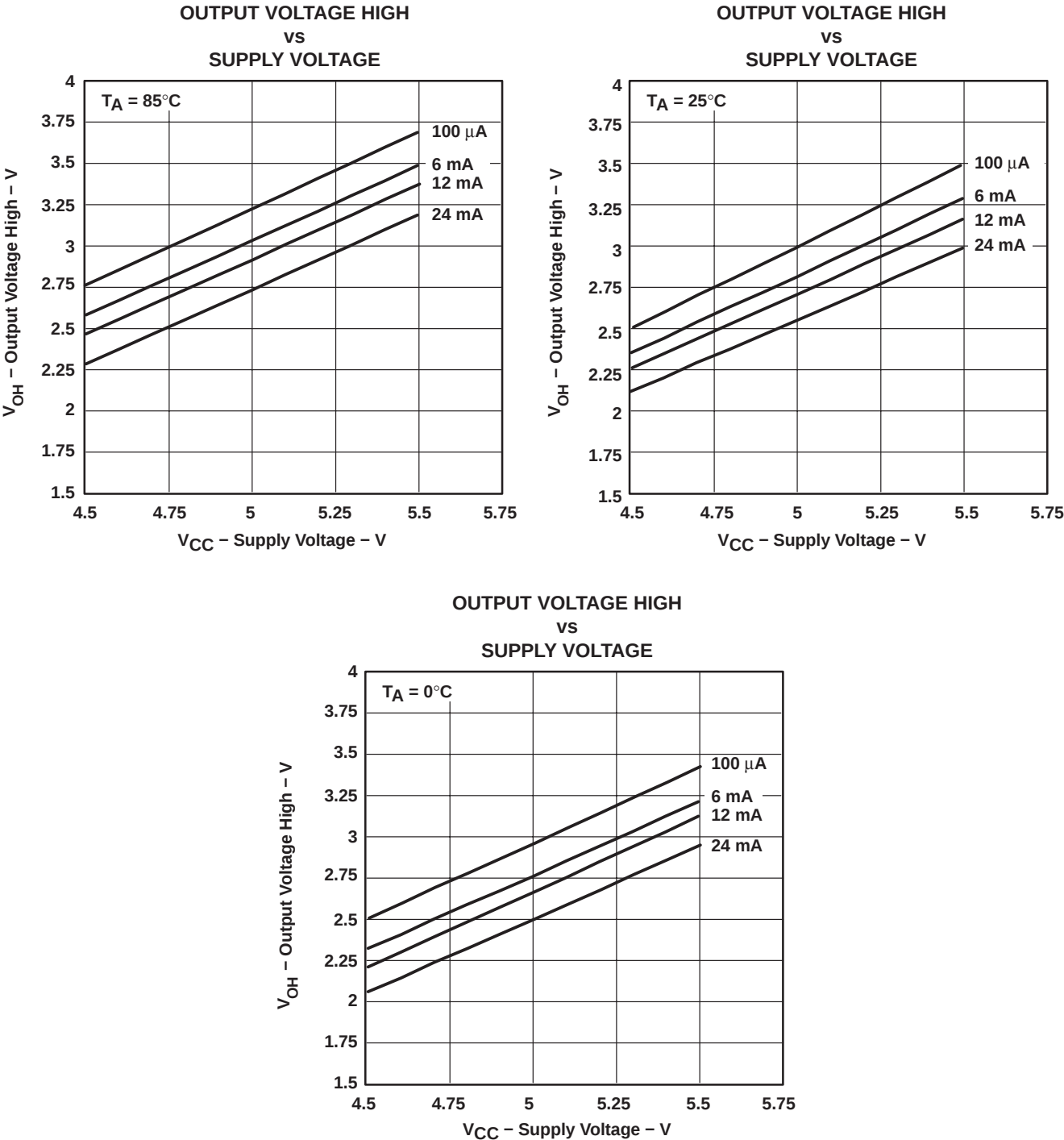
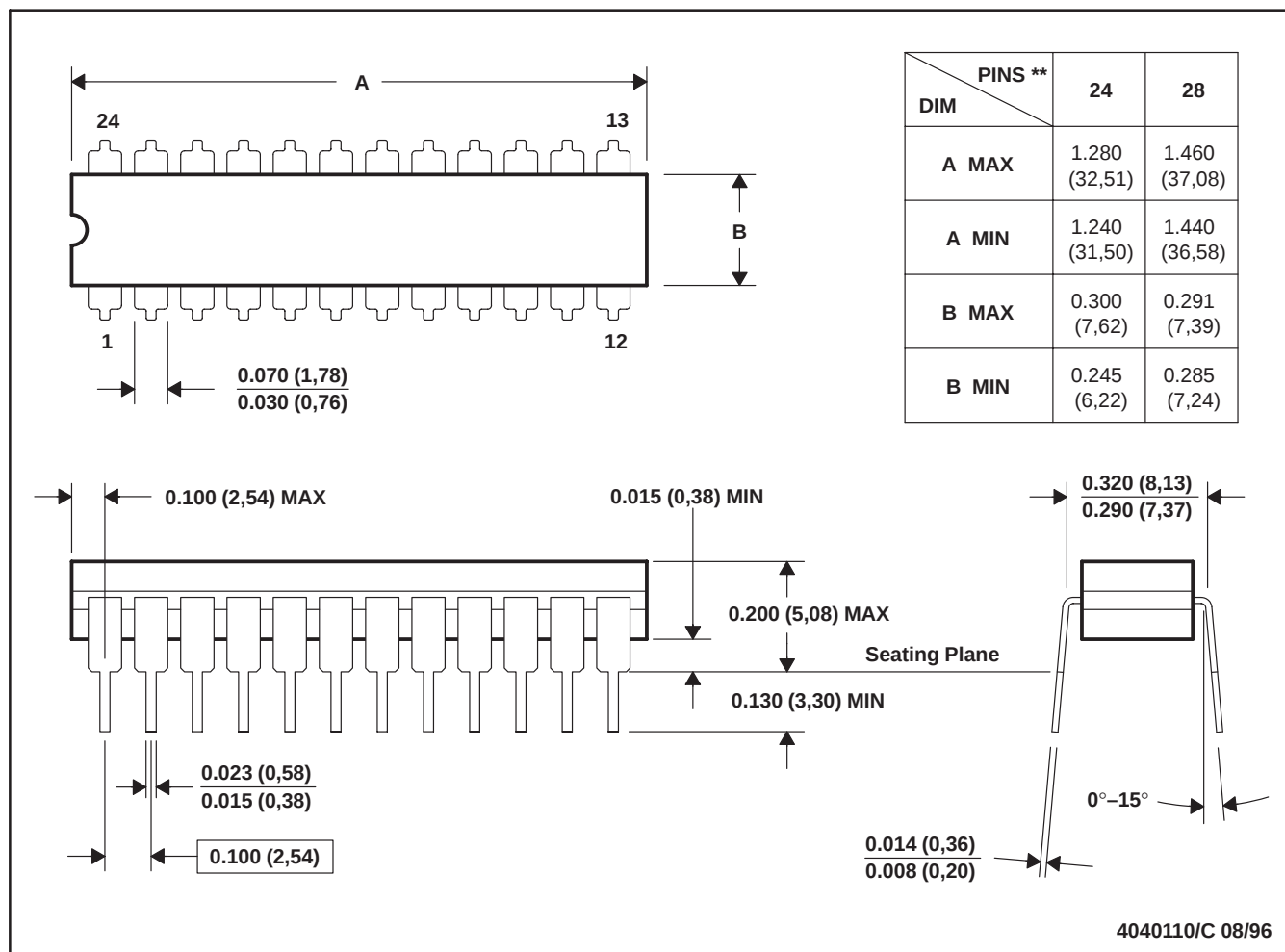


Figure 2. VOH Values

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

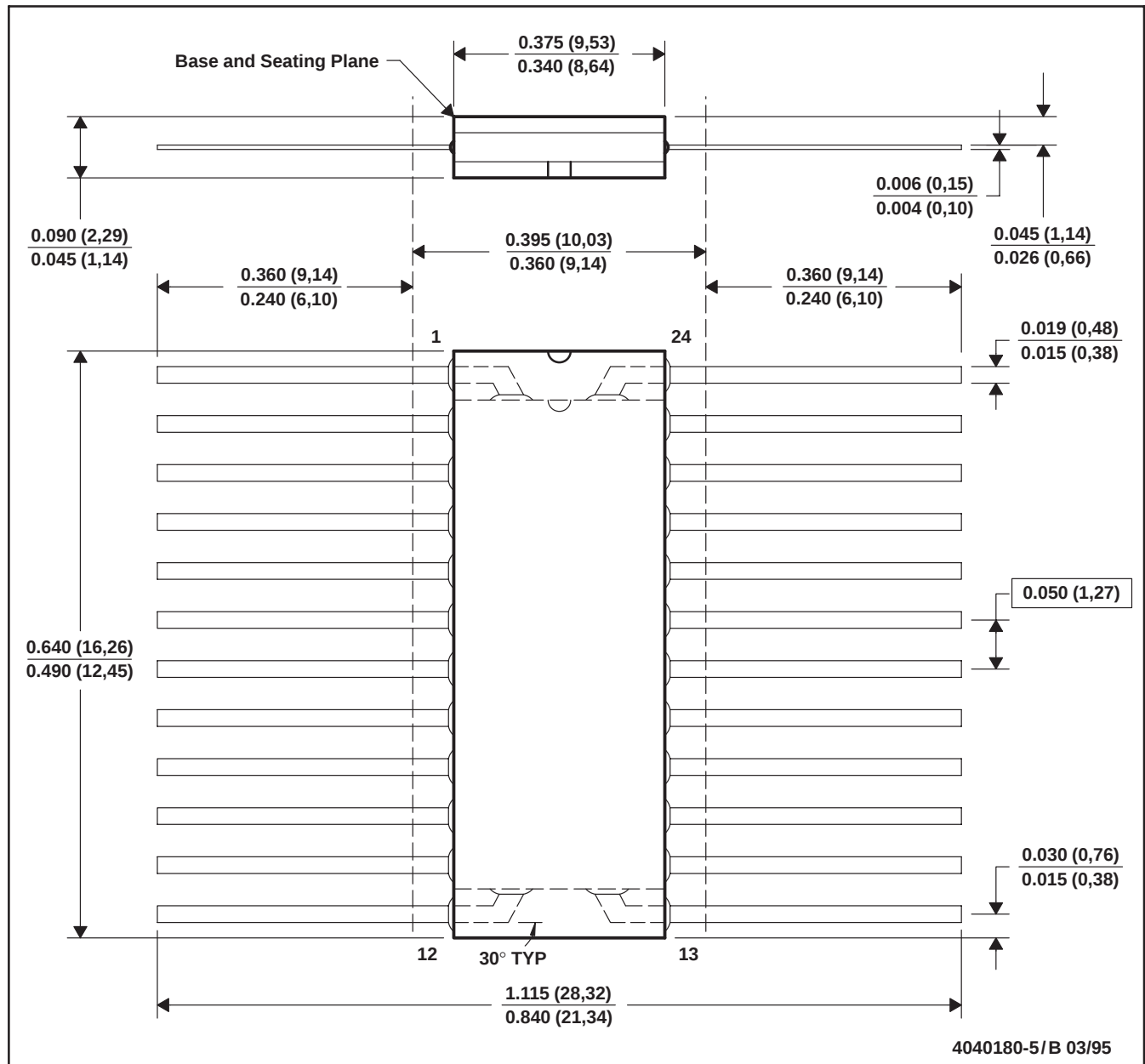
24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 - E. Index point is provided on cap for terminal identification only.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

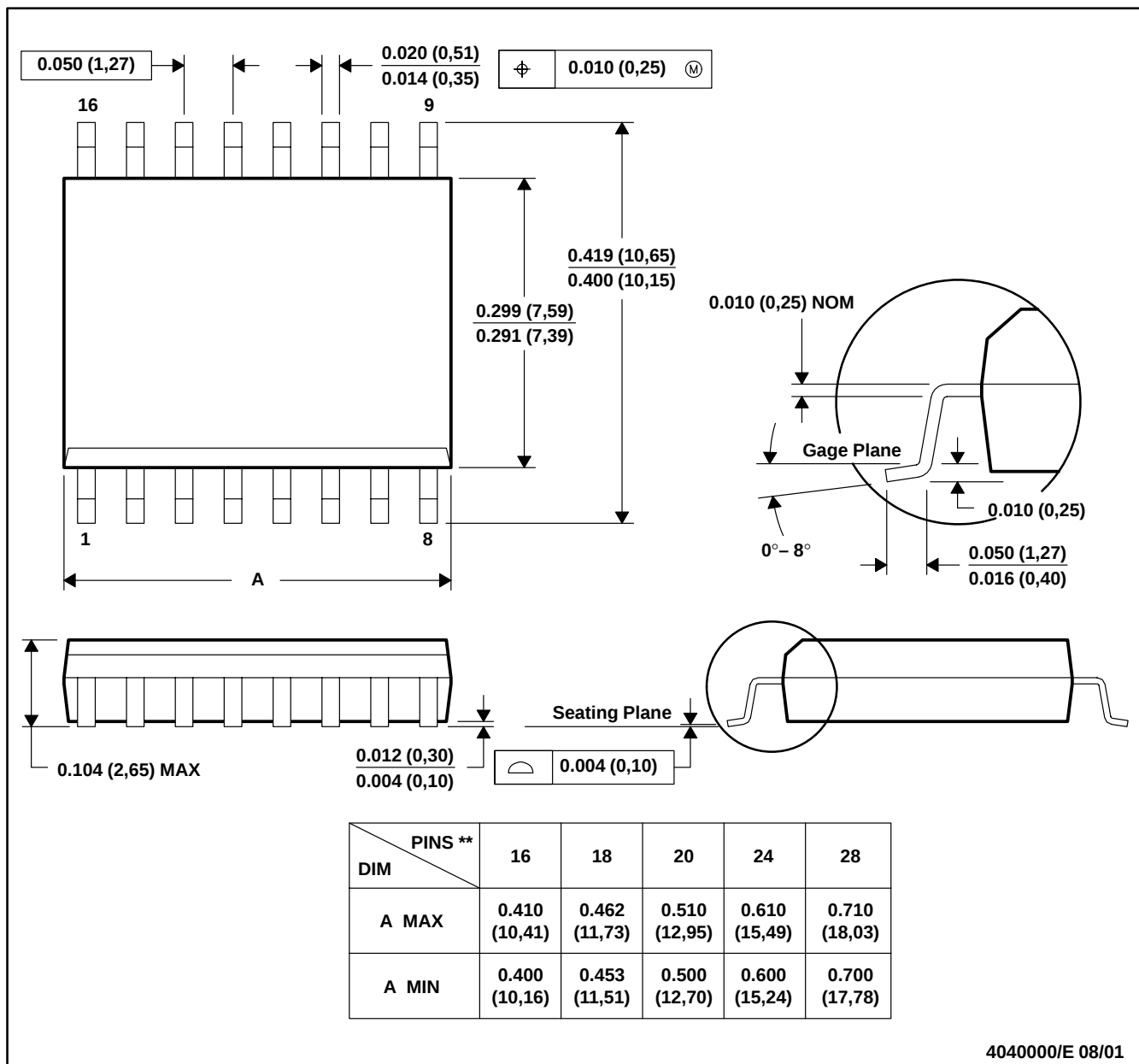


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

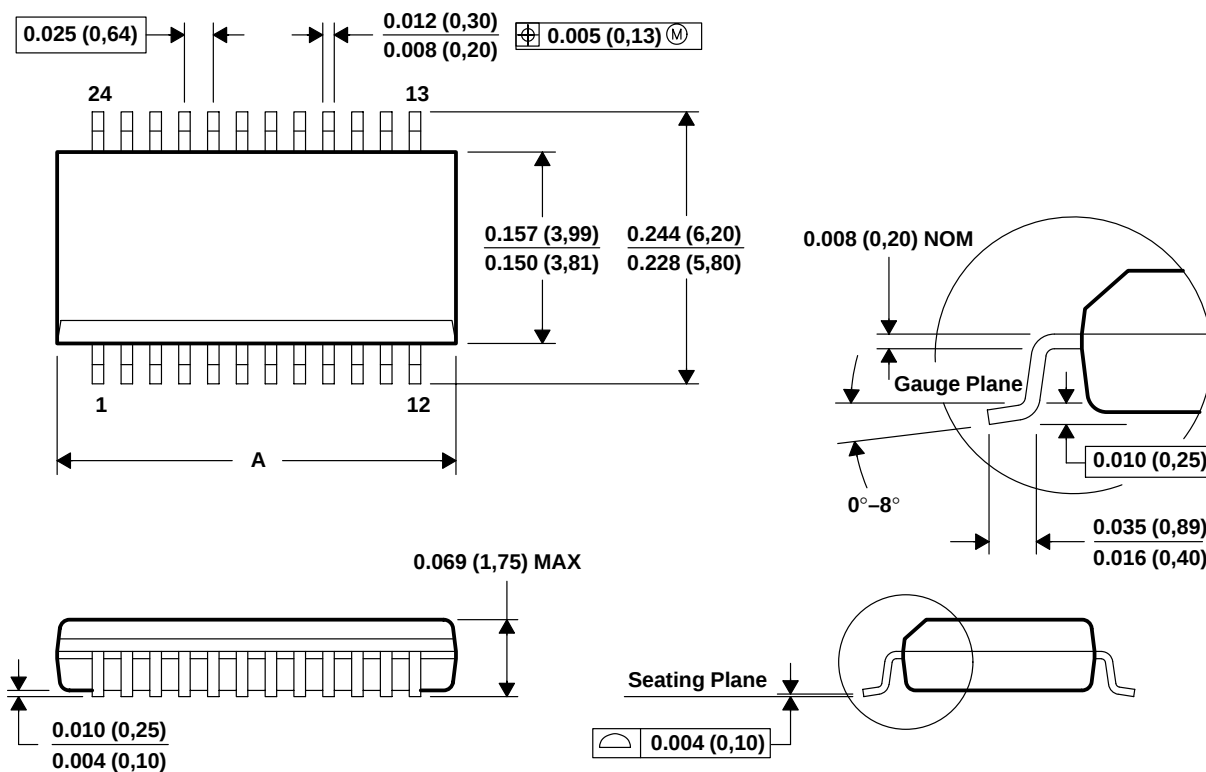
16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

DBQ (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE



PINS **	16	20	24	28
DIM				
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)	0.394 (10,01)
A MIN	0.189 (4,80)	0.337 (8,56)	0.337 (8,56)	0.386 (9,80)
M0-137 VARIATION	AB	AD	AE	AF

4073301/F 02/02

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-137.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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