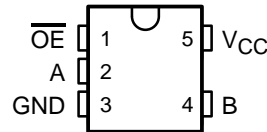


# SN74CBTD1G125 SINGLE FET BUS SWITCH WITH LEVEL SHIFTING

SCDS063K – JULY 1998 – REVISED JANUARY 2003

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

DBV OR DCK PACKAGE  
(TOP VIEW)



## description/ordering information

The SN74CBTD1G125 features a single high-speed line switch. The switch is disabled when the output-enable ( $\overline{OE}$ ) input is high. A diode to  $V_{CC}$  is integrated on the chip to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	SOT (SOT-23) – DBV	Reel of 3000	SN74CBTD1G125DBVR	P25_
		Reel of 250	SN74CBTD1G125DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74CBTD1G125DCKR	PM_
		Reel of 250	SN74CBTD1G125DCKT	

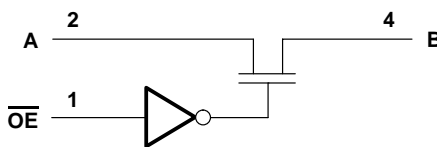
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

‡ The actual top-side marking has one additional character that designates the assembly/test site.

## FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

## logic diagram (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# SN74CBTD1G125 SINGLE FET BUS SWITCH WITH LEVEL SHIFTING

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, $I_{IK}$ ( $V_{I/O} < 0$ )	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5.5	V
$V_{IH}$ High-level control input voltage	2		V
$V_{IL}$ Low-level control input voltage		0.8	V
$T_A$ Operating free-air temperature	-40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT	
$V_{IK}$	$V_{CC} = 4.5$ V, $I_I = -18$ mA			-1.2	V	
$V_{OH}$	See Figure 2					
$I_I$	$V_{CC} = 5.5$ V, $V_I = 5.5$ V or GND			±1	µA	
$I_{CC}$	$V_{CC} = 5.5$ V, $I_O = 0$ , $V_I = V_{CC}$ or GND			1.5	mA	
$\Delta I_{CC}$ §	Control input $V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND			2.5	mA	
$C_i$	Control input $V_I = 3$ V or 0		2		pF	
$C_{io(OFF)}$	$V_O = 3$ V or 0, $\overline{OE} = V_{CC}$		3.5		pF	
$r_{on}$ ¶	$V_{CC} = 4.5$ V	$V_I = 0$	$I_I = 64$ mA	5	7	Ω
			$I_I = 30$ mA	5	7	
		$V_I = 2.4$ V,	$I_I = 15$ mA	35	50	

‡ All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

¶ Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.



# SN74CBTD1G125 SINGLE FET BUS SWITCH WITH LEVEL SHIFTING

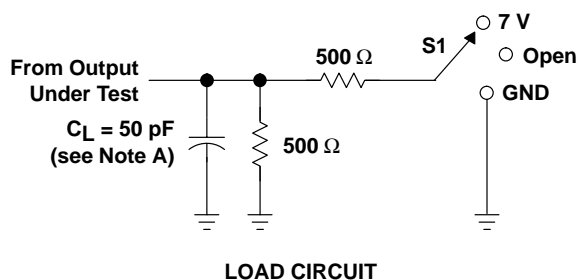
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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

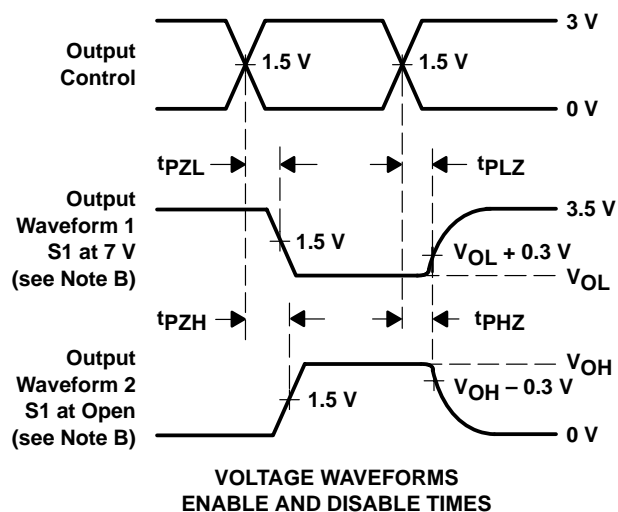
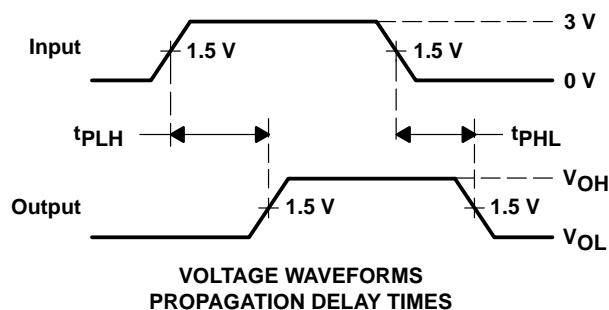
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{pd}^\dagger$	A or B	B or A		0.25	ns
$t_{en}$	$\overline{OE}$	A or B	2	5.9	ns
$t_{dis}$	$\overline{OE}$	A or B	1	4.7	ns

<sup>†</sup> The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**SN74CBTD1G125**  
**SINGLE FET BUS SWITCH**  
**WITH LEVEL SHIFTING**

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**TYPICAL CHARACTERISTICS**

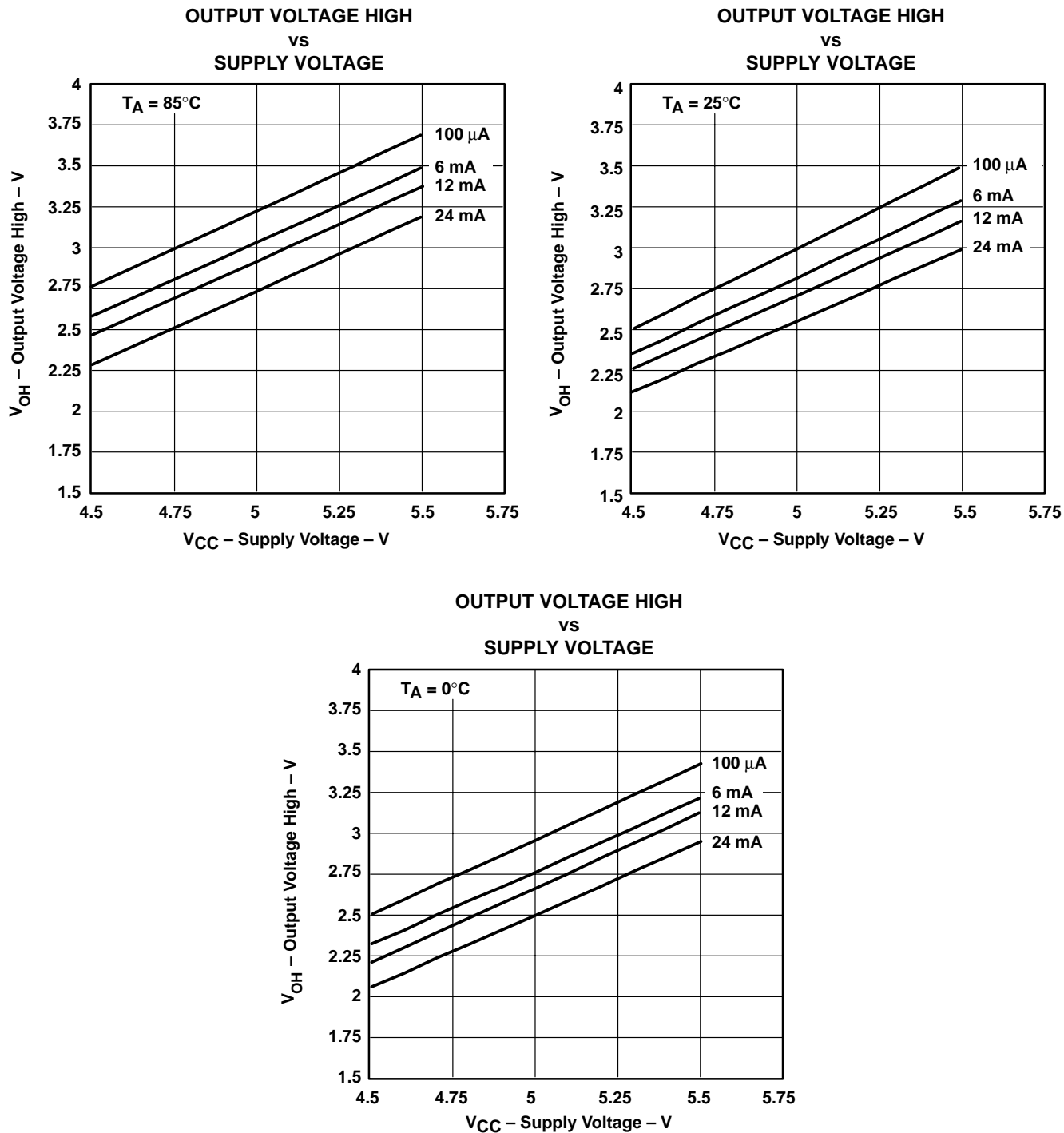


Figure 2.  $V_{OH}$  Values

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### Mailing Address:

Texas Instruments  
Post Office Box 655303  
Dallas, Texas 75265