

SN74CBTD16210 20-BIT FET BUS SWITCH WITH LEVEL SHIFTING

SCDS049H – MARCH 1998 – REVISED JULY 2002

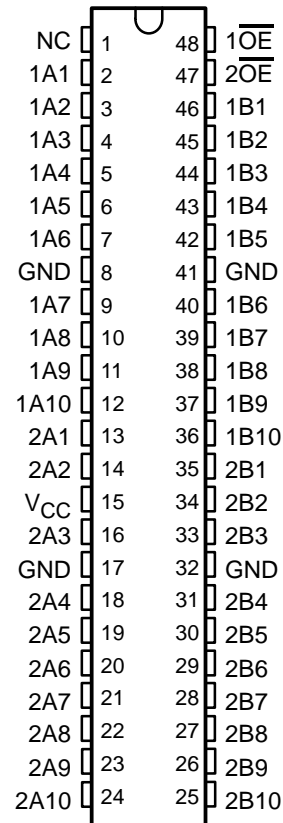
- Member of Texas Instruments Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Designed to Be Used in Level-Shifting Applications

description/ordering information

The SN74CBTD16210 provides 20 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. A diode to V_{CC} is integrated in the circuit to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

The device is organized as a dual 10-bit bus switch with separate output-enable (\overline{OE}) inputs. It can be used as two 10-bit bus switches or as one 20-bit bus switch. When \overline{OE} is low, the associated 10-bit bus switch is on, and port A is connected to port B. When \overline{OE} is high, the switch is open, and the high-impedance state exists between the ports.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CBTD16210DL	CBTD16210
		Tape and reel	SN74CBTD16210DLR	
	TSSOP – DGG	Tape and reel	SN74CBTD16210DGGR	CBTD16210
		TVSOP – DGV	Tape and reel	SN74CBTD16210DGV

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each 10-bit bus switch)

INPUT OE	FUNCTION
L	A port = B port
H	Z



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V	
V_{OH}		See Figure 2						
I_I		$V_{CC} = 0\text{ V}$,	$V_I = 5.5\text{ V}$			10	μA	
		$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V or GND}$			± 1		
I_{CC}		$V_{CC} = 5.5\text{ V}$,	$I_O = 0$,			1.5	mA	
ΔI_{CC}^\ddagger	Control inputs	$V_{CC} = 5.5\text{ V}$,	One input at 3.4 V,			2.5	mA	
C_i	Control inputs	$V_I = 3\text{ V or 0}$				4.5	pF	
$C_{io(OFF)}$		$V_O = 3\text{ V or 0}$,	$\overline{OE} = V_{CC}$			5.5	pF	
r_{on}^\S		$V_{CC} = 4.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$		5	7	Ω
				$I_I = 30\text{ mA}$		5	7	
			$V_I = 2.4\text{ V}$,	$I_I = 15\text{ mA}$		35	50	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

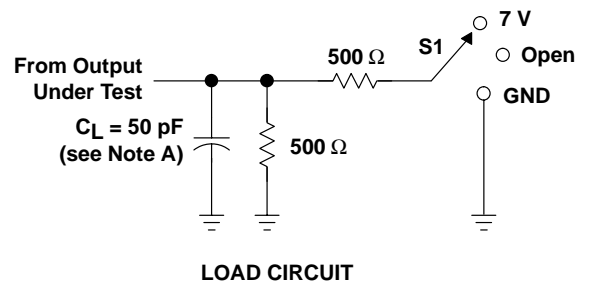
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}^\parallel	A or B	B or A		0.25	ns
t_{en}	\overline{OE}	A or B	1.5	9.8	ns
t_{dis}	\overline{OE}	A or B	1.5	8.9	ns

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

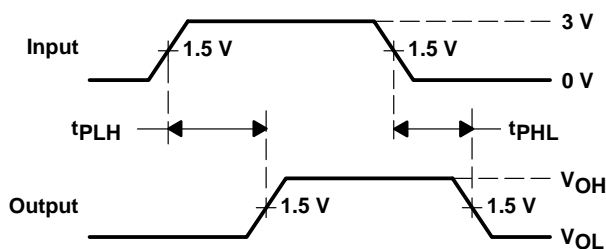
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PARAMETER MEASUREMENT INFORMATION

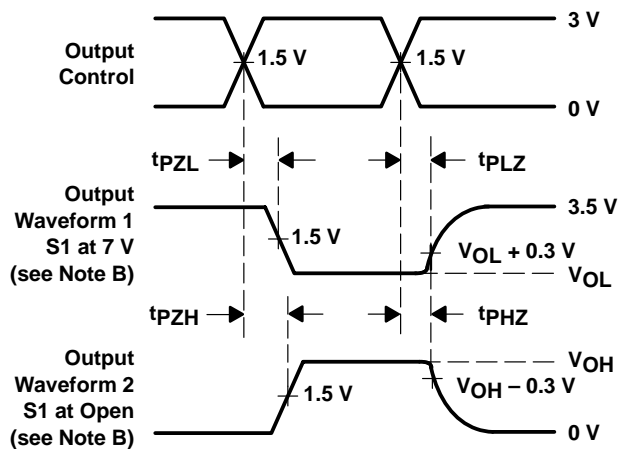


LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

TEST	S1
t _{pd}	Open
t _{PLZ} /t _{PZL}	7 V
t _{PHZ} /t _{PZH}	Open



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - t_{PZL} and t_{PZH} are the same as t_{en}.
 - t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

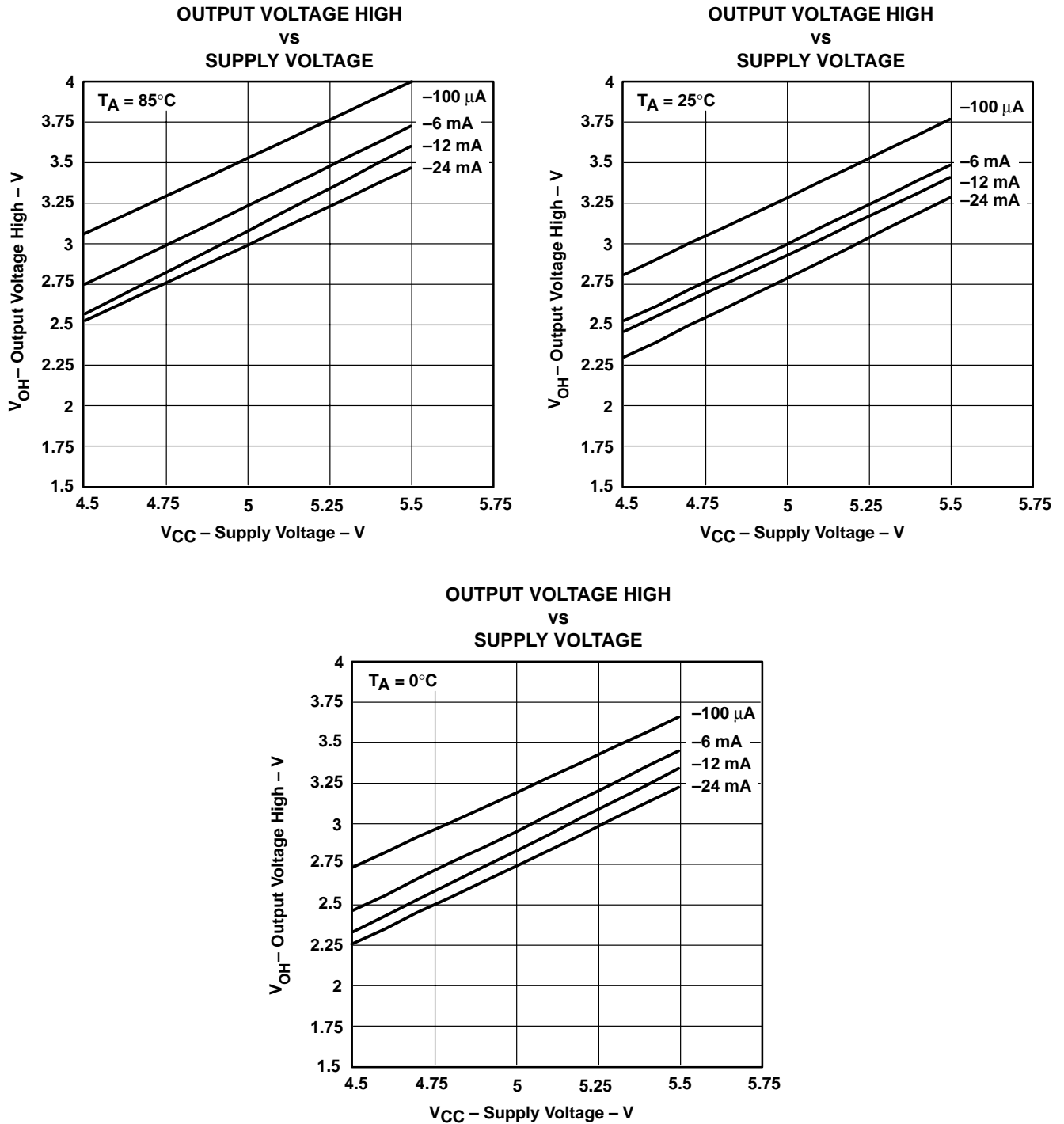


Figure 2. V_{OH} Values

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