

SN54CBT3383, SN74CBT3383 10-BIT FET BUS-EXCHANGE SWITCHES

SCDS0030 – NOVEMBER 1992 – REVISED JULY 2004

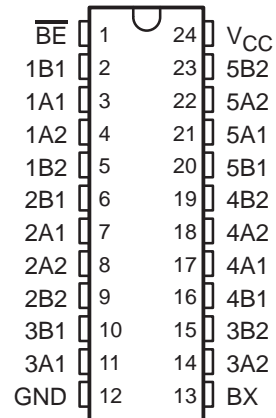
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

SN54CBT3383 . . . JT OR W PACKAGE
SN74CBT3383 . . . DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)

description/ordering information

The 'CBT3383 devices provide ten bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The devices operate as a 10-bit bus switch or a 5-bit bus exchanger, which provides swapping of the A and B pairs of signals. The bus-exchange function is selected when BX is high. The switches are connected when \overline{BE} is low.



ORDERING INFORMATION

| TA | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-------------------|----------------|-----------------------|------------------|
| -40°C to 85°C | SOIC – DW | Tube | SN74CBT3383DW | CBT3383 |
| | | Tape and reel | SN74CBT3383DWR | |
| | SSOP – DB | Tape and reel | SN74CBT3383DBR | CU383 |
| | SSOP (QSOP) – DBQ | Tape and reel | SN74CBT3383DBQR | CBT3383 |
| | TSSOP – PW | Tube | SN74CBT3383PW | CU383 |
| Tape and reel | | SN74CBT3383PWR | | |
| -55°C to 125°C | TVSOP – DGV | Tape and reel | SN74CBT3383DGVR | CU383 |
| | CDIP – JT | Tube | SNJ54CBT3383JT | SNJ54CBT3383JT |
| | CFP – W | Tube | SNJ54CBT3383W | SNJ54CBT3383W |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

| INPUTS | | INPUTS/OUTPUTS | |
|-----------------|----|----------------|---------|
| \overline{BE} | BX | 1A1–5A1 | 1A2–5A2 |
| L | L | 1B1–5B1 | 1B2–5B2 |
| L | H | 1B2–5B2 | 1B1–5B1 |
| H | X | Z | Z |



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

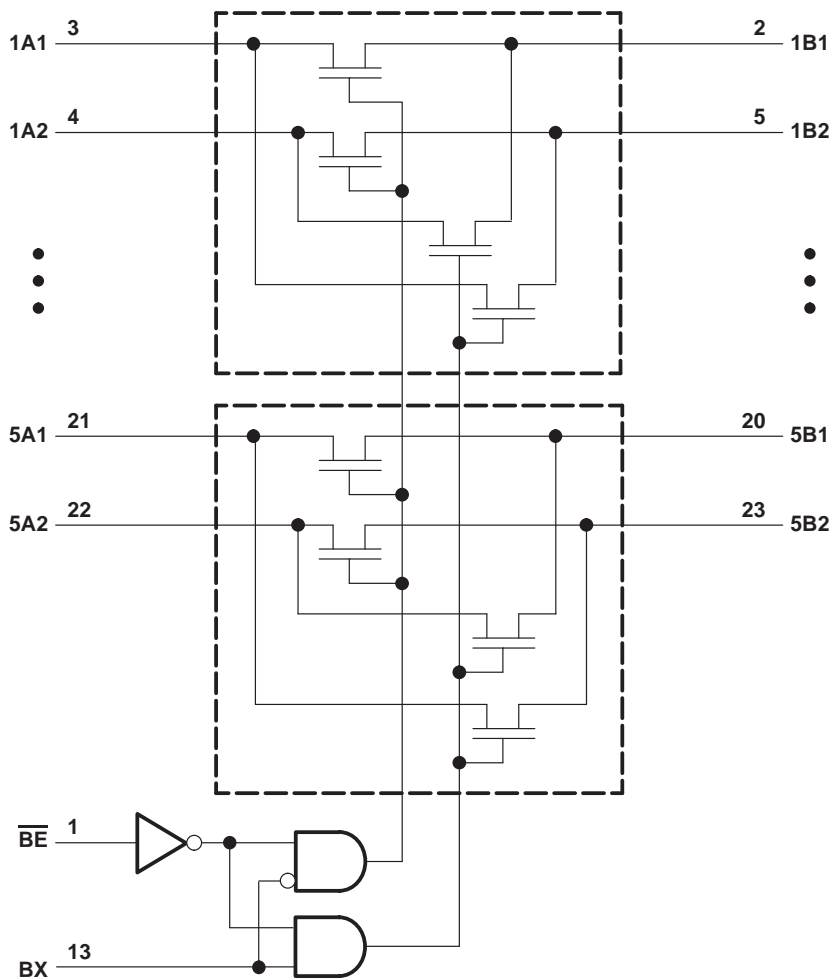
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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Continuous channel current | 128 mA |
| Input clamp current, I_{IK} ($V_{I/O} < 0$) | -50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): | |
| DB package | 63°C/W |
| DBQ package | 61°C/W |
| DGV package | 86°C/W |
| DW package | 46°C/W |
| PW package | 88°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.



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recommended operating conditions (see Note 3)

| | | SN54CBT3383 | | SN74CBT3383 | | UNIT |
|----------|----------------------------------|-------------|-----|-------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} | High-level control input voltage | 2 | | 2 | | V |
| V_{IL} | Low-level control input voltage | | 0.8 | | 0.8 | V |
| T_A | Operating free-air temperature | -55 | 125 | 0 | 70 | °C |

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54CBT3383 | | SN74CBT3383 | | UNIT | | |
|----------------------|--|---|----------------------|-------------|-----|------|------|-----|
| | | MIN | TYP† | MAX | MIN | | TYP† | MAX |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | | | -1.2 | | -1.2 | V | |
| I_I | $V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$ or GND | | | ±5 | | ±1 | μA | |
| I_{CC} | $V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND | | | 50 | | 50 | μA | |
| $\Delta I_{CC}‡$ | Control inputs $V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at V_{CC} or GND | | | 2.5 | | 2.5 | mA | |
| C_i | Control inputs $V_I = 3\text{ V}$ or 0 | | | | | 3 | pF | |
| | $V_I = 2.5\text{ V}$ | | | 5 | | | | |
| $C_{iO}(\text{OFF})$ | $V_O = 3\text{ V}$ or 0, $\overline{BE} = V_{CC}$ | | | | | 6 | pF | |
| | $V_O = 2.5\text{ V}$, $\overline{BE} = V_{CC}$ | | | 6 | | | | |
| $r_{on}§$ | $V_{CC} = 4.5\text{ V}$ | $V_I = 0$ | $I_I = 64\text{ mA}$ | 5 | 9.2 | 5 | 7 | Ω |
| | | | $I_I = 30\text{ mA}$ | | | 5 | 7 | |
| | | $V_I = 2.4\text{ V}$, $I_I = 15\text{ mA}$ | 10 | 17 | 10 | 15 | | |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

§ Measured by the voltage drop between the input terminal and the output terminal at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

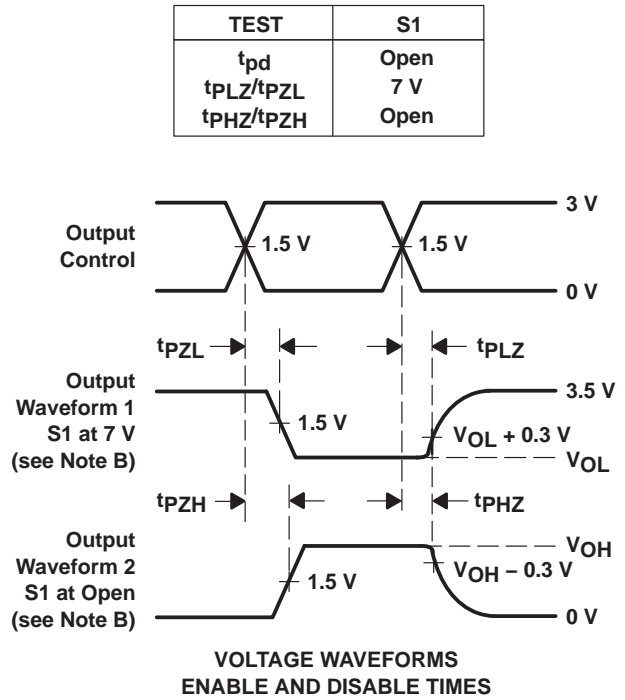
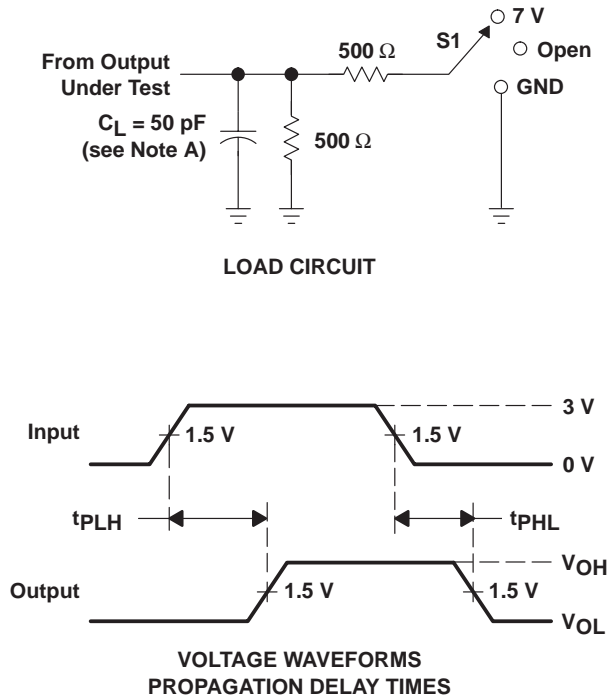
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54CBT3383 | | SN74CBT3383 | | UNIT |
|-----------|-----------------|-------------|-------------|------|-------------|------|------|
| | | | MIN | MAX | MIN | MAX | |
| $t_{pd}¶$ | A or B | B or A | | 1.5 | | 0.25 | ns |
| t_{pd} | BX | A or B | 1 | 10.2 | 1 | 9.2 | ns |
| t_{en} | \overline{BE} | A or B | 1 | 10.8 | 1 | 8.6 | ns |
| t_{dis} | \overline{BE} | A or B | 1 | 8.2 | 1 | 7.5 | ns |

¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PZL} and t_{PHZ} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|---------------------------------------|-------------------------|
| 5962-9668801QKA | ACTIVE | CFP | W | 24 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9668801QK A SNJ54CBT3383W | Samples |
| 5962-9668801QLA | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9668801QL A SNJ54CBT3383JT | Samples |
| SN74CBT3383DBLE | OBSOLETE | SSOP | DB | 24 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74CBT3383DBQR | ACTIVE | SSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CBT3383 | Samples |
| SN74CBT3383DBR | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CU383 | Samples |
| SN74CBT3383DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBT3383 | Samples |
| SN74CBT3383DWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBT3383 | Samples |
| SN74CBT3383DWRG4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CBT3383 | Samples |
| SN74CBT3383PW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CU383 | Samples |
| SN74CBT3383PWLE | OBSOLETE | TSSOP | PW | 24 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74CBT3383PWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CU383 | Samples |
| SN74CBT3383PWRG4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CU383 | Samples |
| SNJ54CBT3383JT | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9668801QL A SNJ54CBT3383JT | Samples |
| SNJ54CBT3383W | ACTIVE | CFP | W | 24 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9668801QK A SNJ54CBT3383W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54CBT3383, SN74CBT3383 :

● Catalog: [SN74CBT3383](#)

● Military: [SN54CBT3383](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CBT3383DBQR | SSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74CBT3383DBR | SSOP | DB | 24 | 2000 | 330.0 | 16.4 | 8.2 | 8.8 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74CBT3383DWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74CBT3383PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74CBT3383DBQR | SSOP | DBQ | 24 | 2500 | 367.0 | 367.0 | 38.0 |
| SN74CBT3383DBR | SSOP | DB | 24 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74CBT3383DWR | SOIC | DW | 24 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74CBT3383PWR | TSSOP | PW | 24 | 2000 | 367.0 | 367.0 | 38.0 |

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

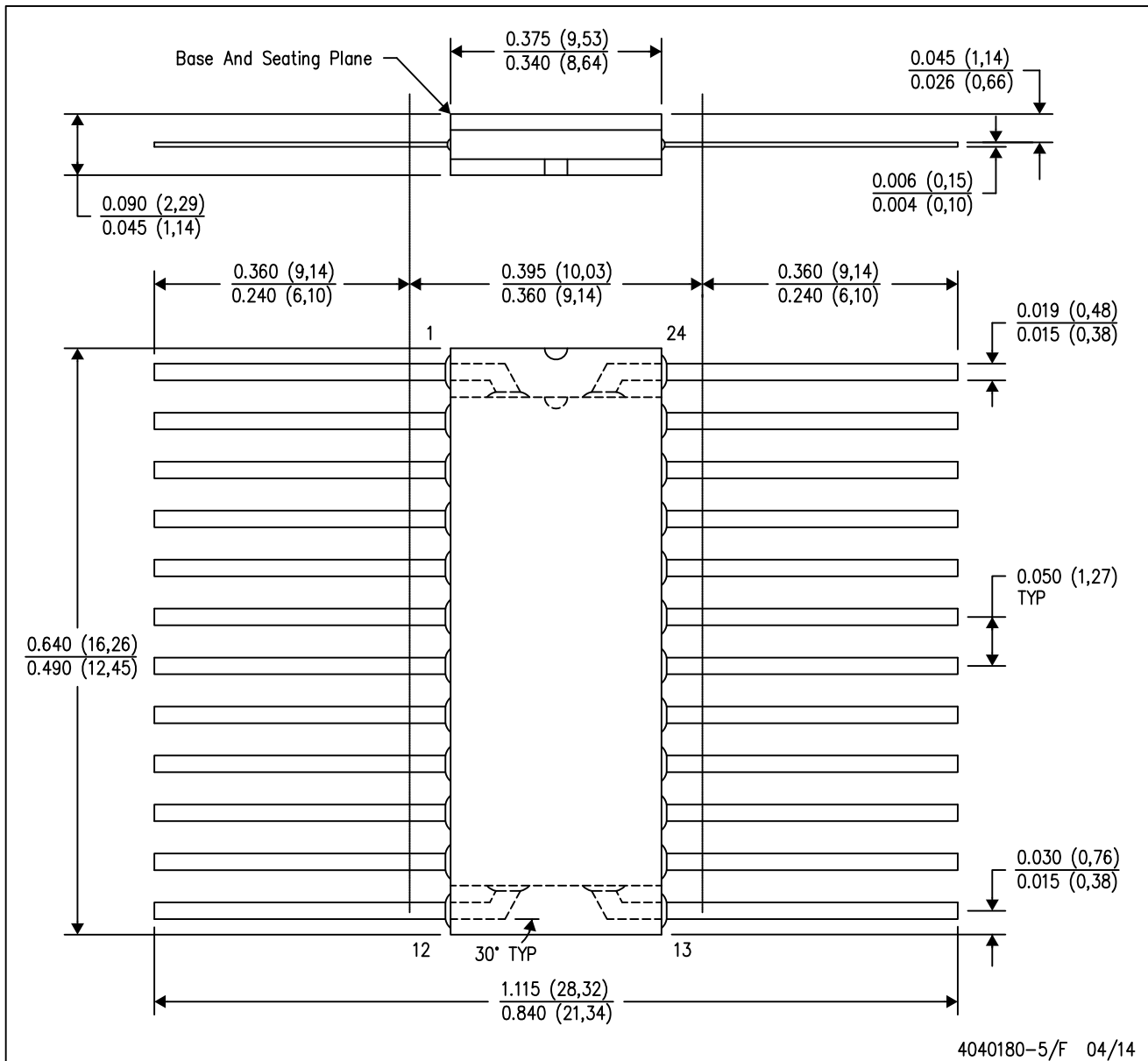
24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

DW (R-PDSO-G24)

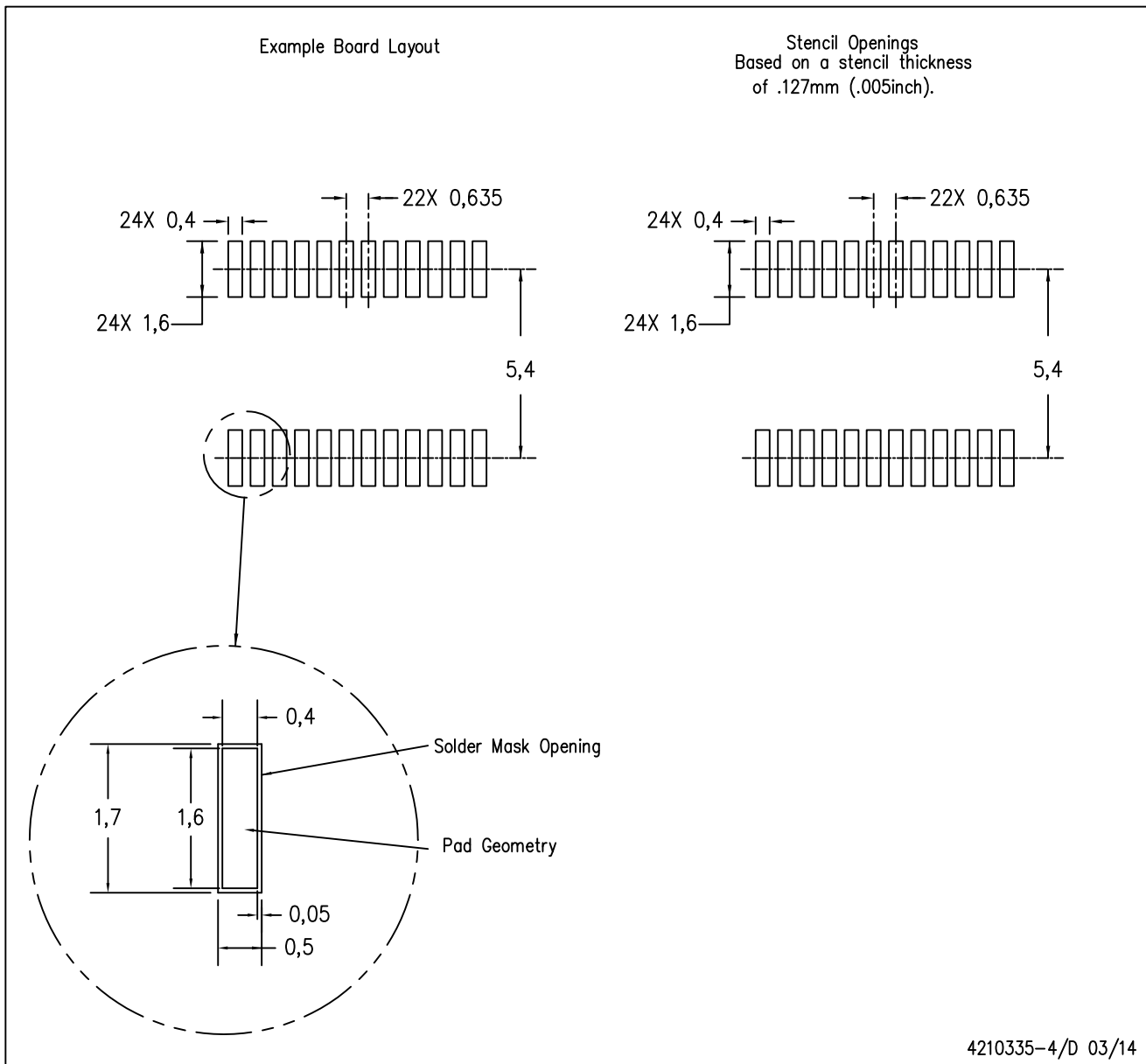
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

DBQ (R-PDSO-G24)

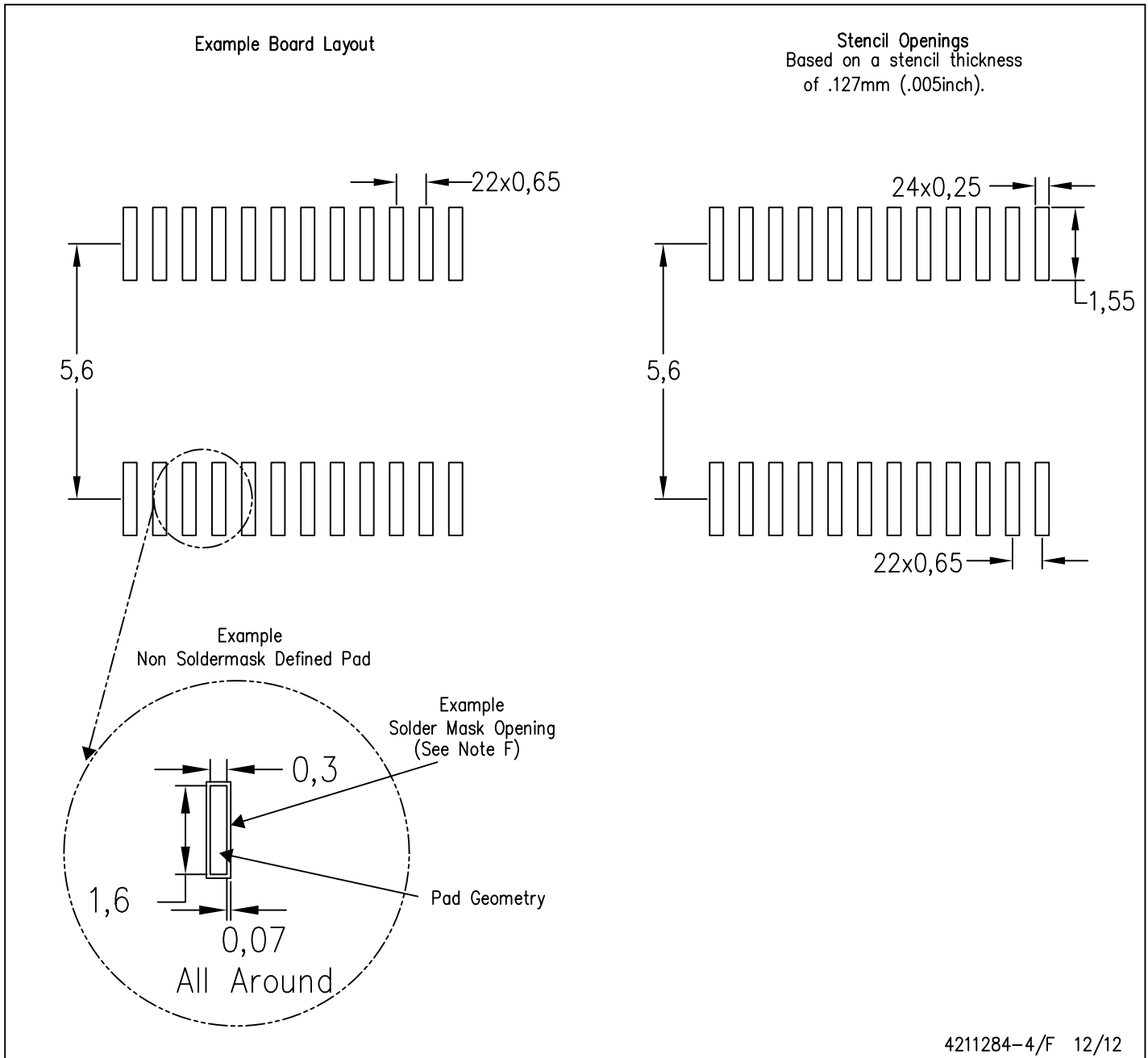
PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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