

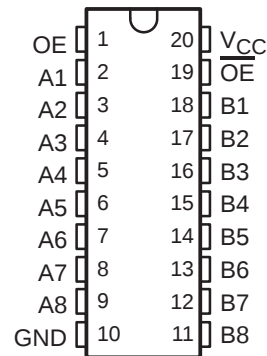
- Standard '245-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

description/ordering information

The SN74CBT3345 provides eight bits of high-speed TTL-compatible bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 8-bit switch bank with dual output-enable (OE and $\overline{\text{OE}}$) inputs. When $\overline{\text{OE}}$ is low or OE is high, the switch is on, and port A is connected to port B. When $\overline{\text{OE}}$ is high and OE is low, the switch is open, and the high-impedance state exists between the two ports.

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – DW	Tube	SN74CBT3345DW	CBT3345
		Tape and reel	SN74CBT3345DWR	
	SSOP – DB	Tape and reel	SN74CBT3345DBR	CU345
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBT3345DBQR	CBT3345
	TSSOP – PW	Tube	SN74CBT3345PW	CU345
		Tape and reel	SN74CBT3345PWR	
	TVSOP – DGV	Tape and reel	SN74CBT3345DGVR	CU345

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		FUNCTION
OE	$\overline{\text{OE}}$	
H	X	A port = B port
X	L	A port = B port
L	H	Disconnect



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

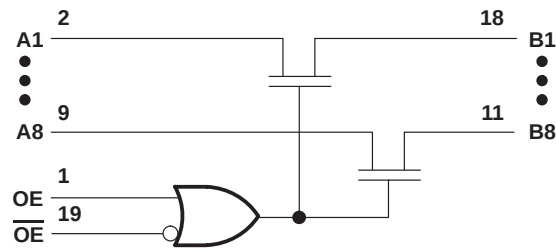
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SN74CBT3345
8-BIT FET BUS SWITCH

SCDS027I – MAY 1995 – REVISED JANUARY 2004

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C
DBQ package	68°C
DGV package	92°C
DW package	58°C
PW package	83°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.5	5.5	V
V_{IH} High-level control input voltage	2		V
V_{IL} Low-level control input voltage		0.8	V
T_A Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP [†]	MAX	UNIT	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA					-1.2	V	
I _I	All inputs	V _{CC} = 5.5 V, V _I = 5.5 V or GND					±1	μA	
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND					50	μA	
ΔI _{CC} [‡]	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND					3.5	mA	
C _i	Control inputs	V _I = 3 V or 0					3	pF	
C _{io} (OFF)		V _O = 3 V or 0, $\overline{\text{OE}}$ = V _{CC} or OE = GND					6	pF	
r _{on} [§]		V _{CC} = 4.5 V	V _I = 0	I _I = 64 mA			5	7	Ω
				I _I = 30 mA			5	7	
			V _I = 2.4 V, I _I = 15 mA			10	15		

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

[§] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	
$t_{pd}^{\parallel}$	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$ or OE	A or B	1	9.1	ns
t_{dis}	$\overline{OE}$ or OE	A or B	1	8.7	ns

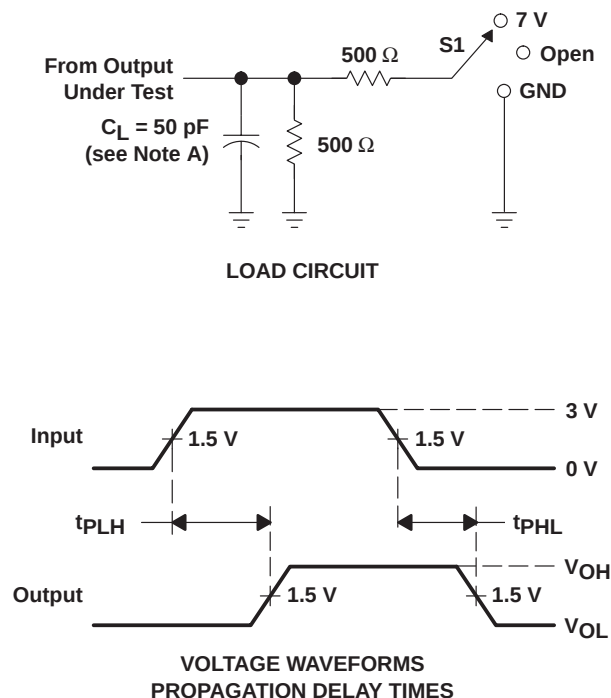
^{||} The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

SN74CBT3345

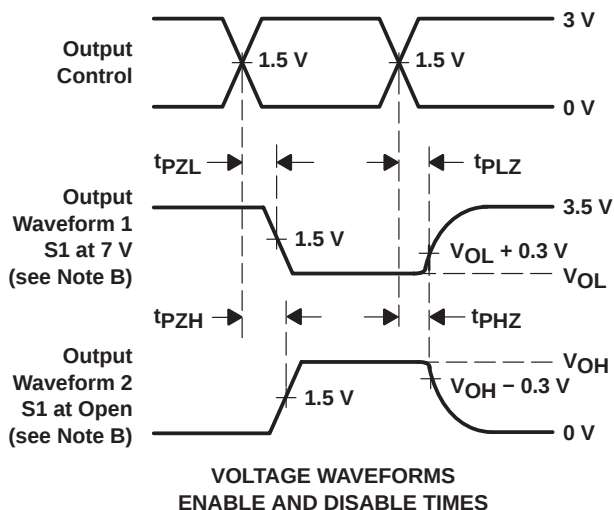
8-BIT FET BUS SWITCH

SCDS0271 – MAY 1995 – REVISED JANUARY 2004

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



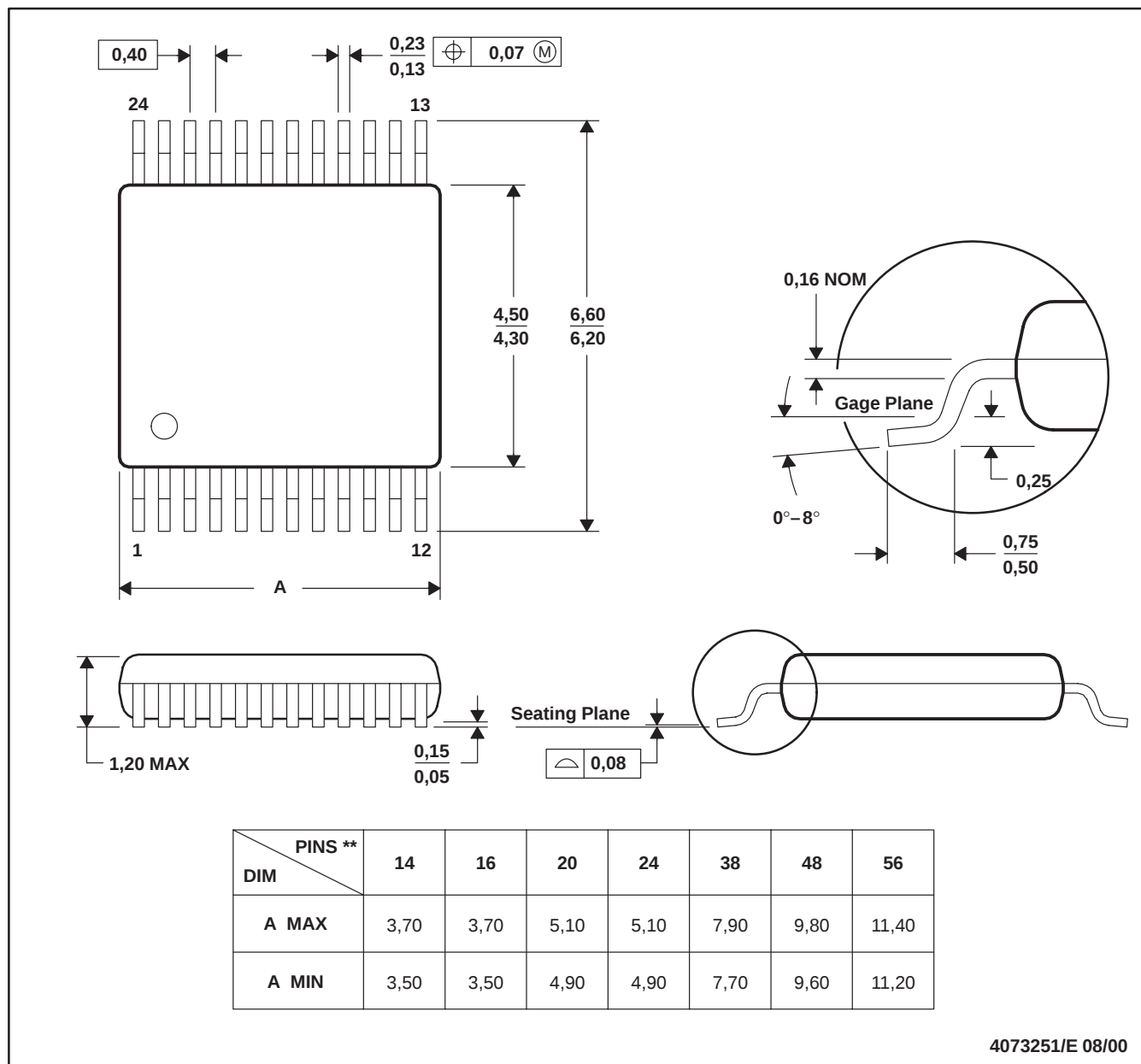
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

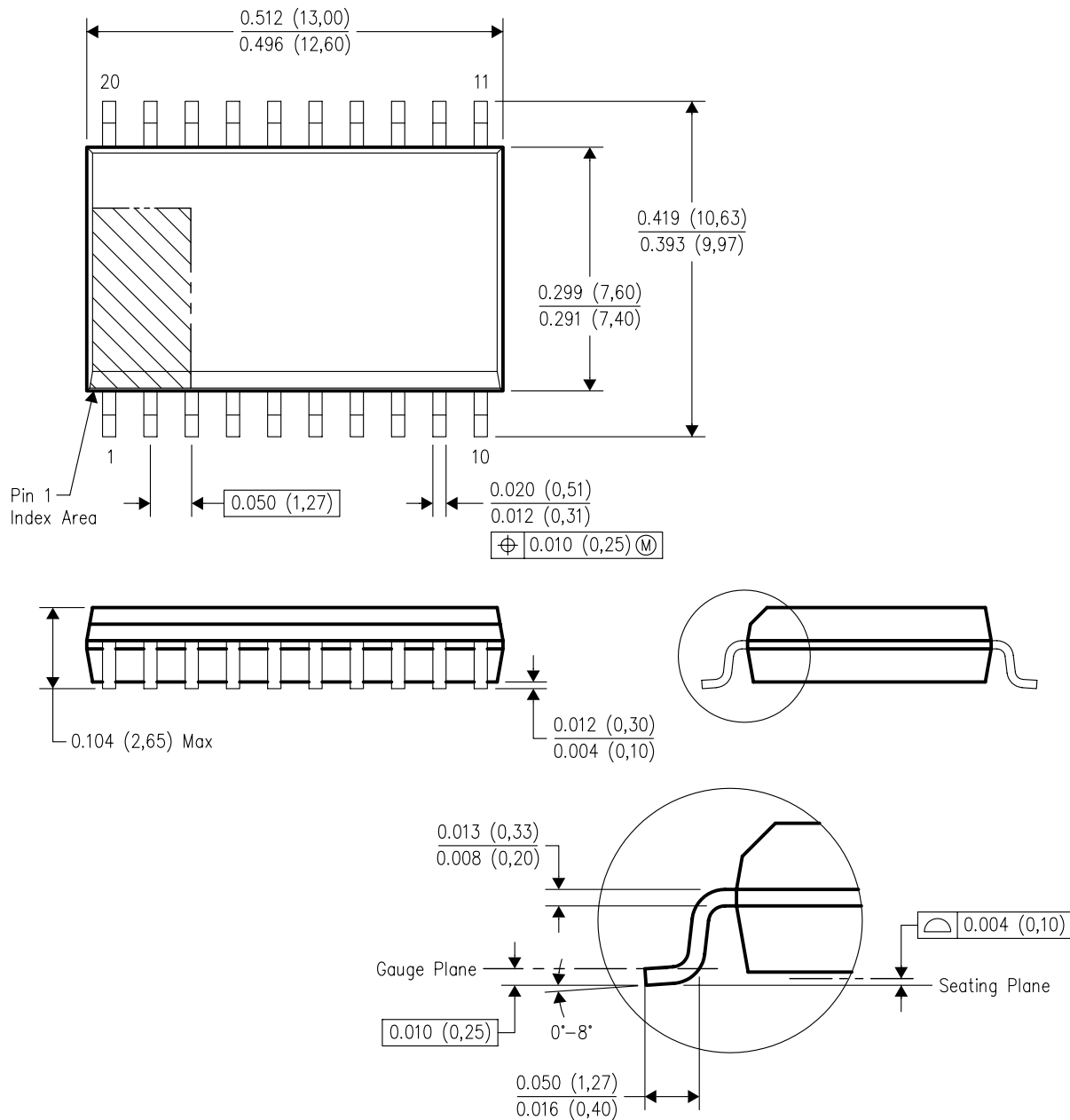
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE

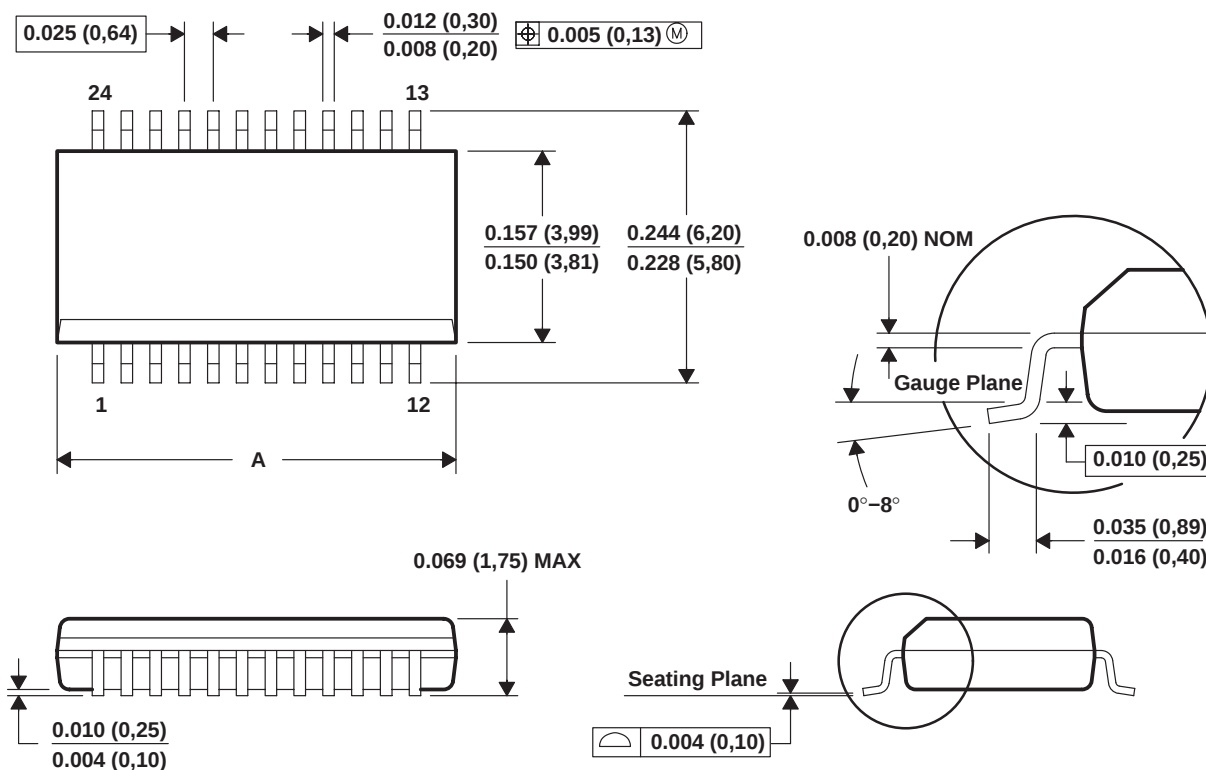


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- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AC.

DBQ (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE



PINS **	16	20	24	28
DIM				
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)	0.394 (10,01)
A MIN	0.189 (4,80)	0.337 (8,56)	0.337 (8,56)	0.386 (9,80)
M0-137 VARIATION	AB	AD	AE	AF

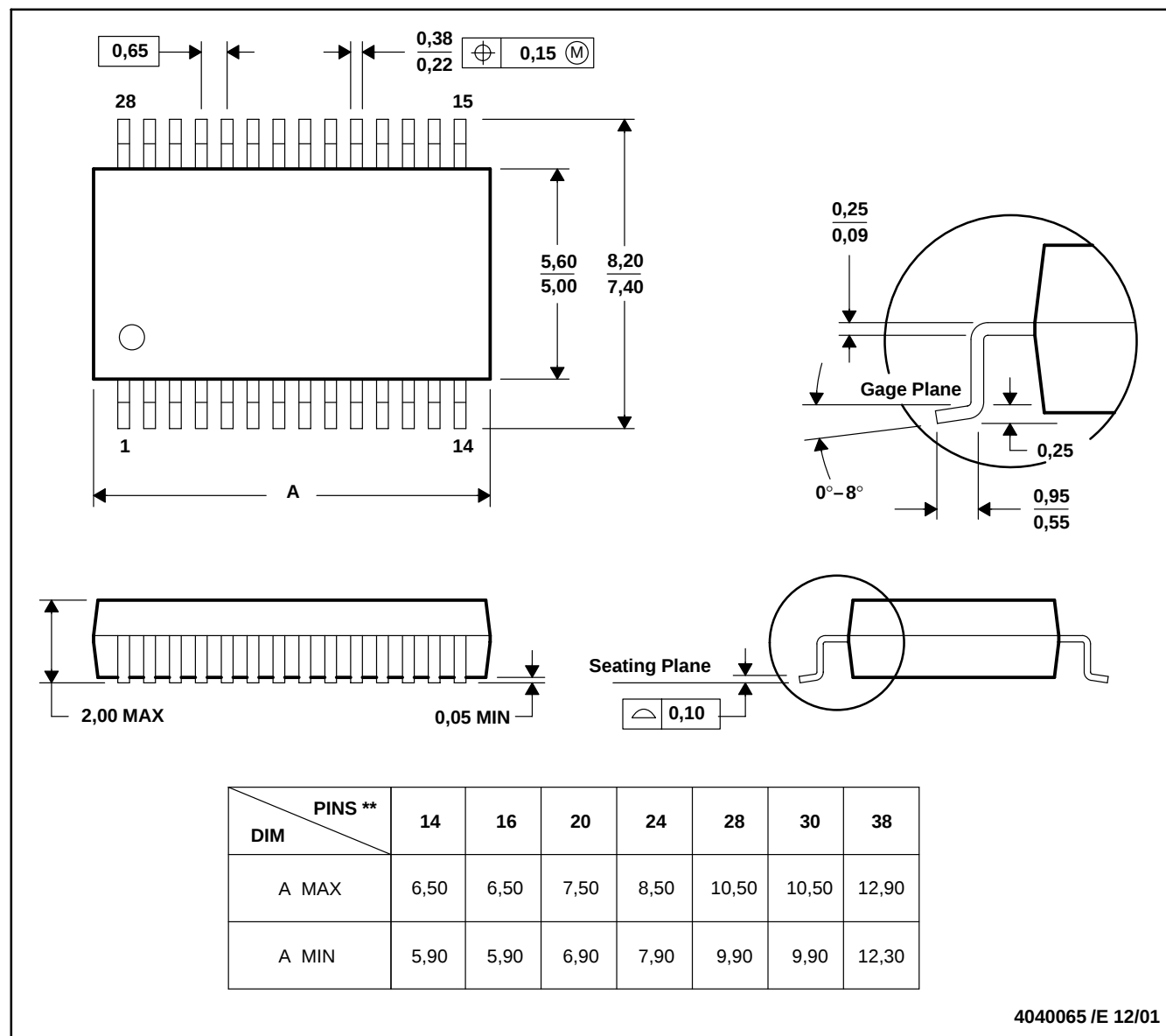
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- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-137.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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