

SN74CBT16390

16-BIT TO 32-BIT FET MULTIPLEXER/DEMULTIPLEXER BUS SWITCH

SCDS035E – OCTOBER 1997 – REVISED OCTOBER 2000

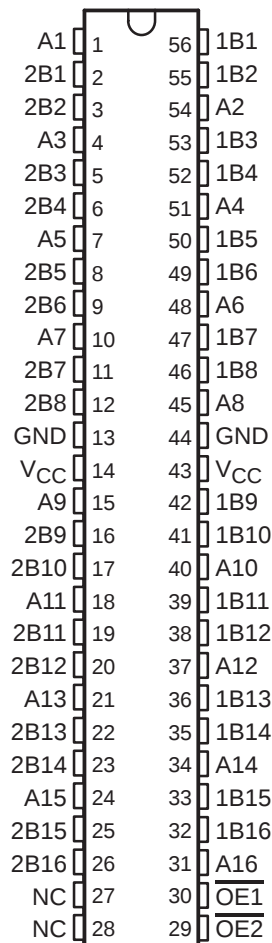
- Member of Texas Instruments' Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

description

The SN74CBT16390 is a 16-bit to 32-bit switch used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path. This device can be used for memory interleaving, in which two different banks of memory must be addressed simultaneously. This device also can be used to connect or isolate the PCI bus to one or two slots simultaneously.

Two output enables ($\overline{OE1}$ and $\overline{OE2}$) control the data flow. When $\overline{OE1}$ is low, A port is connected to 1B port. When $\overline{OE2}$ is low, A port is connected to 2B port. When both $\overline{OE1}$ and $\overline{OE2}$ are low, the A port is connected to both 1B and 2B ports. The control inputs can be driven with a 5-V CMOS, 5-V TTL, or an LVTTTL driver.

DGG, DGV, OR DL PACKAGE (TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74CBT16390DL	CBT16390
		Tape and reel	SN74CBT16390DLR	
	TSSOP – DGG	Tape and reel	SN74CBT16390DGGR	CBT16390
	TVSOP – DGV	Tape and reel	SN74CBT16390DGVR	CY390

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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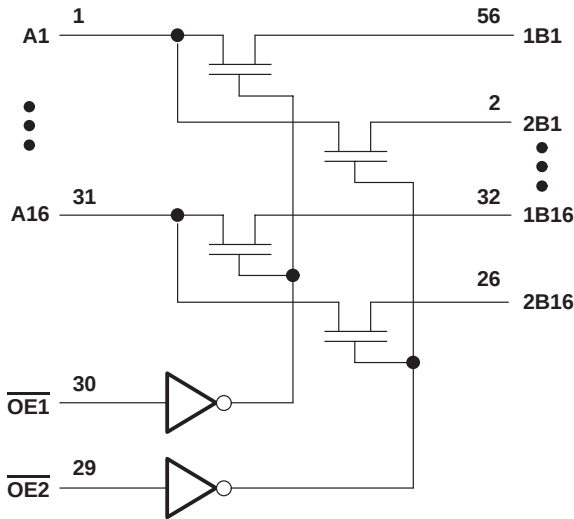
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FUNCTION TABLE

INPUTS		FUNCTION
OE1	OE2	
L	L	A = 1B and A = 2B
L	H	A = 1B
H	L	A = 2B
H	H	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	−0.5 V to 7 V
Input voltage range, V _I (see Note 1)	−0.5 V to V _{CC} + 0.5 V
Continuous channel current	128 mA
Input clamp current, I _{IK} (V _I < 0)	−50 mA
Package thermal impedance, θ _{JA} (see Note 2): DGG package	64°C/W

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
VCC Supply voltage	4.5	5.5	V
VIH High-level control input voltage	2		V
VIL Low-level control input voltage		0.8	V
TA Operating free-air temperature	−40	85	°C

NOTE 3: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
I_I		$V_{CC} = 0$,	$V_I = 5.5\text{ V}$			10	μA
		$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V or GND}$			± 1	
I_{CC}		$V_{CC} = 5.5\text{ V}$,	$I_O = 0$,			3	μA
$\Delta I_{CC}^{\ddagger}$	Control inputs	$V_{CC} = 5.5\text{ V}$,	One input at 3.4 V, Other input at V_{CC} or GND			2.5	mA
C_i	Control inputs	$V_I = 3\text{ V or 0}$				5	pF
$C_{io(OFF)}$		$V_O = 3\text{ V or 0}$				5.5	pF
$r_{on}^{\S}$		$V_{CC} = 4.5\text{ V}$	$V_I = 0$			5	Ω
			$I_I = 64\text{ mA}$			7	
			$I_I = 30\text{ mA}$			5	
			$V_I = 2.4\text{ V}$,			7	12
			$I_I = 15\text{ mA}$				

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[§] Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{pd}^{\parallel}$	A or B	B or A		0.25	ns
t_{en}	$\overline{OE}$	A or B	1.3	5.9	ns
t_{dis}	$\overline{OE}$	A or B	1	5.3	ns

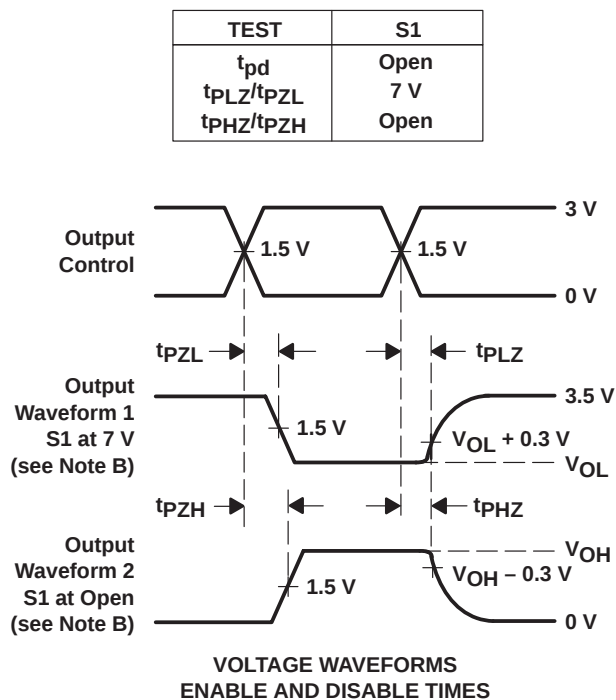
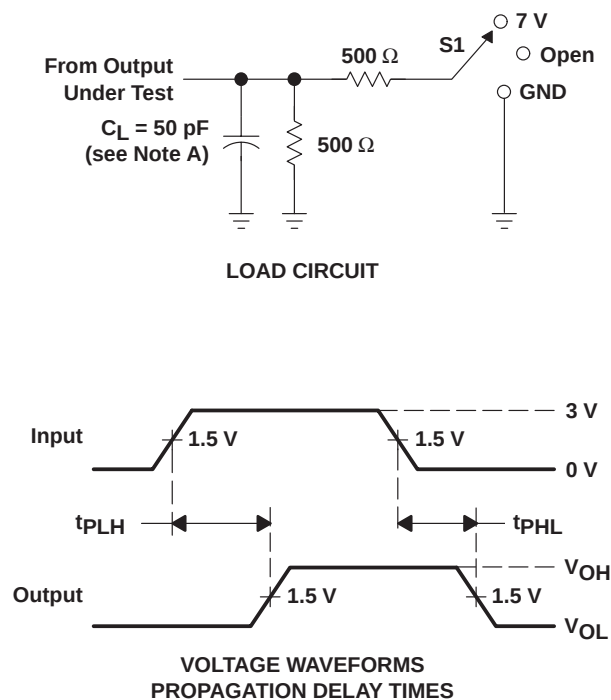
^{||} The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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