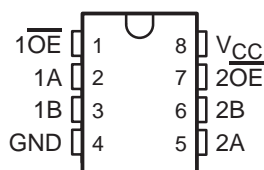


2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

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- Output Voltage Translation Tracks V_{CC}
- Supports Mixed-Mode Signal Operation On All Data I/O Ports
 - 5-V Input Down To 3.3-V Output Level Shift With 3.3-V V_{CC}
 - 5-V/3.3-V Input Down To 2.5-V Output Level Shift With 2.5-V V_{CC}
- 5-V Tolerant I/Os With Device Powered-Up or Powered-Down
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{ON}) Characteristics ($r_{ON} = 5 \Omega$ Typical)
- Low Input/Output Capacitance Minimizes Loading ($C_{iO(OFF)} = 4.5 \text{ pF}$ Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ($I_{CC} = 20 \mu\text{A}$ Max)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
- Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Digital Applications: Level Translation, USB Interface, Bus Isolation
- Ideal for Low-Power Portable Equipment

DCT OR DCU PACKAGE
(TOP VIEW)



description/ordering information

The SN74CB3T3306 is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{ON}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC} . The SN74CB3T3306 supports systems using 5-V TTL, 3.3-V LVTTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 1).

The SN74CB3T3306 is organized as two 1-bit bus switches with separate output-enable ($\overline{1OE}$, $\overline{2OE}$) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When \overline{OE} is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	SSOP – DCT	Tape and reel	SN74CB3T3306DCTR	WA6_ _ _
	VSSOP – DCU	Tape and reel	SN74CB3T3306DCUR	WA6_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.

DCU: The actual top-side marking has one additional character that designates the assembly/test site.

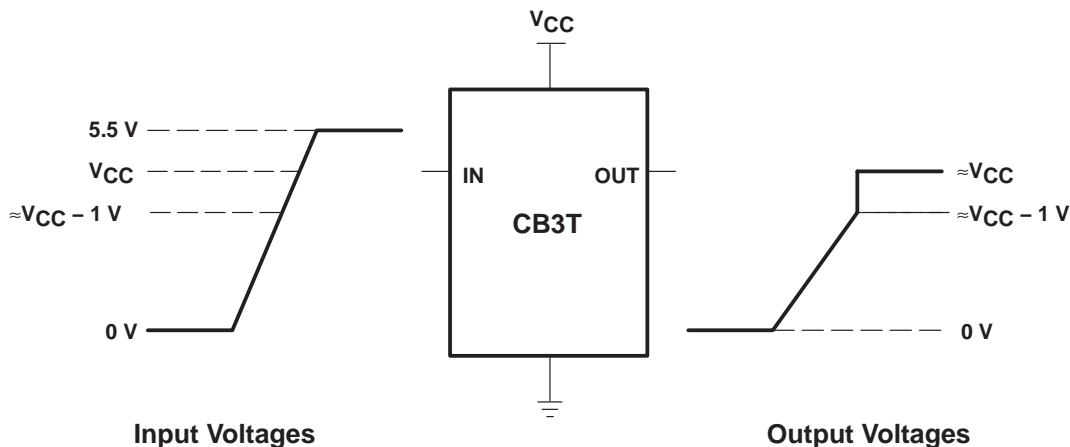


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SN74CB3T3306
DUAL FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

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description/ordering information (continued)



NOTE A: If the input high voltage (V_{IH}) level is greater than or equal to $V_{CC} - 1\text{ V}$, and less than or equal to 5.5 V , then the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage-Translation Characteristics

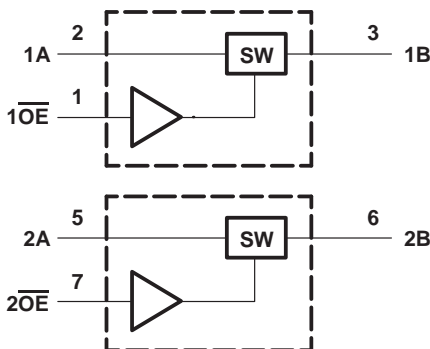
This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each bus switch)

INPUT \overline{OE}	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

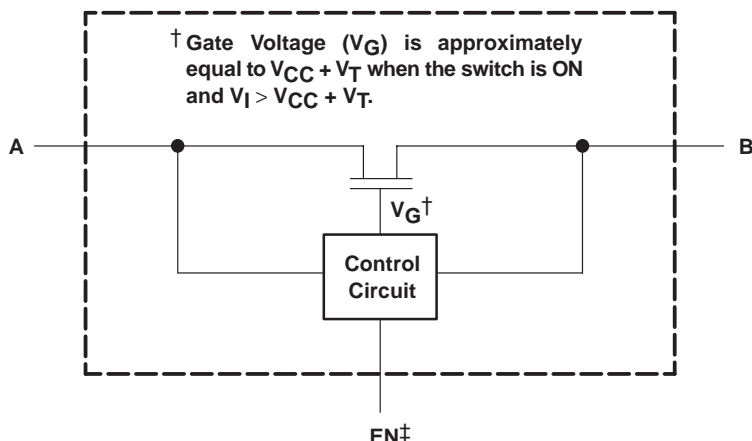
logic diagram (positive logic)



2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

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simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	–0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	–0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	–50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	–50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DCT package	220°C/W
DCU package	227°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- All voltages are with respect to ground unless otherwise specified.
 - The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - V_I and V_O are used to denote specific conditions for $V_{I/O}$.
 - I_I and I_O are used to denote specific conditions for $I_{I/O}$.
 - The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT	
V_{CC}	Supply voltage	2.3	3.6	V	
V_{IH}	High-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	5.5	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	5.5	
V_{IL}	Low-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	0.8	
$V_{I/O}$	Data input/output voltage	0	5.5	V	
T_A	Operating free-air temperature	–40	85	°C	

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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DUAL FET BUS SWITCH

2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT		
V_{IK}		$V_{CC} = 3\text{ V}$, $I_I = -18\text{ mA}$			-1.2	V		
V_{OH}		See Figures 3 and 4						
I_{IN}	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_{IN} = 3.6\text{ V to } 5.5\text{ V or GND}$			± 10	μA		
I_I	Switch ON, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC} - 0.7\text{ V to } 5.5\text{ V}$			± 20	μA		
		$V_I = 0.7\text{ V to } V_{CC} - 0.7\text{ V}$			-40			
		$V_I = 0\text{ to } 0.7\text{ V}$			± 5			
I_{OZ}^\ddagger		$V_{CC} = 3.6\text{ V}$, $V_O = 0\text{ to } 5.5\text{ V}$, $V_I = 0$, Switch OFF, $V_{IN} = V_{CC}$ or GND			± 10	μA		
I_{off}		$V_{CC} = 0$, $V_O = 0\text{ to } 5.5\text{ V}$, $V_I = 0$,			10	μA		
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_{I/O} = 0$, Switch ON or OFF, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC}$ or GND			20	μA	
			$V_I = 5.5\text{ V}$			20		
ΔI_{CC}^\S	Control inputs	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND			300	μA		
C_{in}	Control inputs	$V_{CC} = 3.3\text{ V}$, $V_{IN} = V_{CC}$ or GND			3	pF		
$C_{io(OFF)}$		$V_{CC} = 3.3\text{ V}$, $V_{I/O} = 5.5\text{ V, } 3.3\text{ V, or GND}$, Switch OFF, $V_{IN} = V_{CC}$ or GND			4.5	pF		
$C_{io(ON)}$		$V_{CC} = 3.3\text{ V}$, Switch ON, $V_{IN} = V_{CC}$ or GND	$V_{I/O} = 5.5\text{ V or } 3.3\text{ V}$			4	pF	
			$V_{I/O} = \text{GND}$			15		
r_{on}^\P		$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$, $V_I = 0$	$I_O = 24\text{ mA}$			5	Ω	
			$I_O = 16\text{ mA}$			5		
		$V_{CC} = 3\text{ V}$, $V_I = 0$	$I_O = 64\text{ mA}$			5		7
			$I_O = 32\text{ mA}$			5		7

V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.

† All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



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DUAL FET BUS SWITCH
2.5-V/3.3-V LOW-VOLTAGE BUS SWITCH WITH 5-V TOLERANT LEVEL SHIFTER

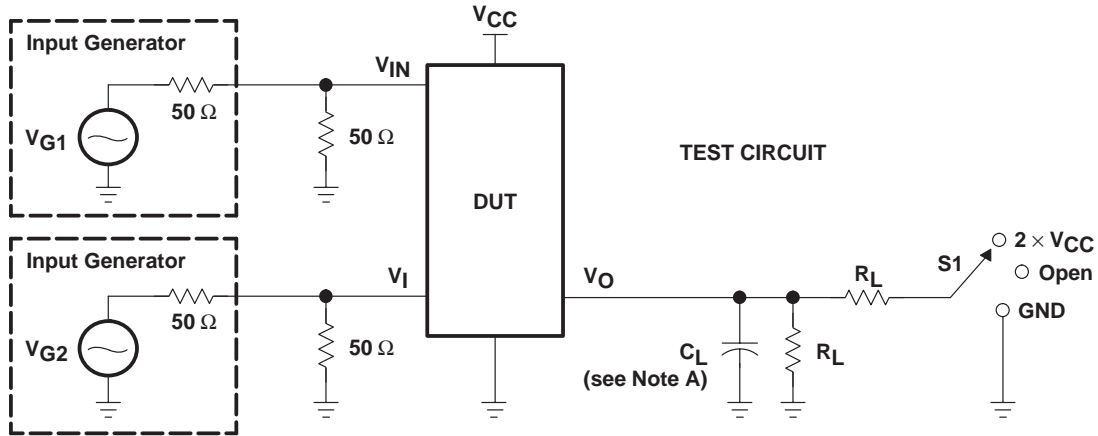
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

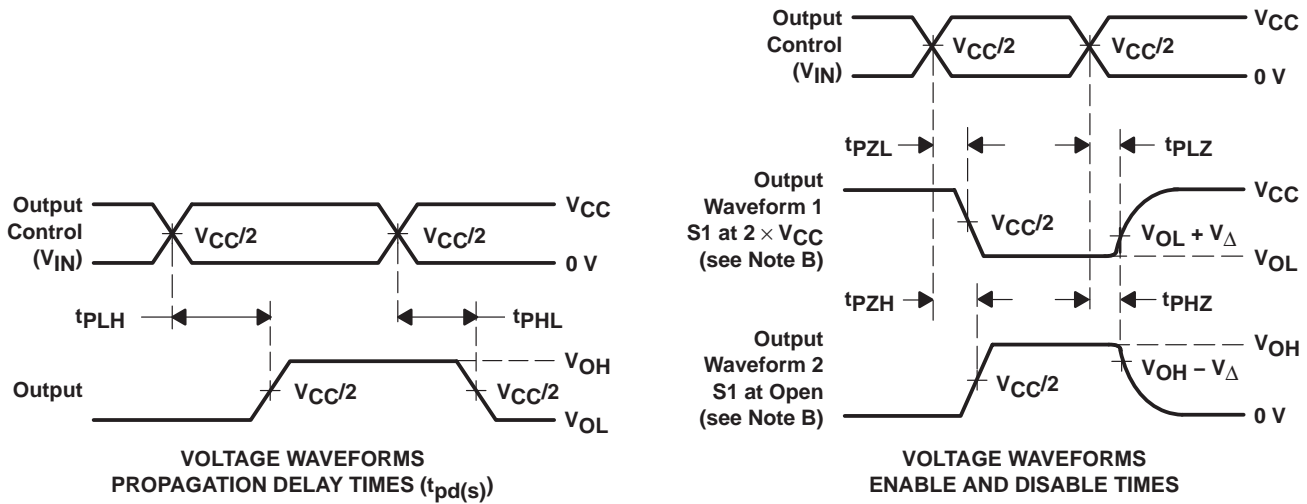
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t _{pd} [†]	A or B	B or A	0.15		0.25		ns
t _{en}	\overline{OE}	A or B	1	8.5	1	6.5	ns
t _{dis}	\overline{OE}	A or B	1	9	1	9	ns

[†] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



TEST	VCC	S1	RL	VI	CL	VΔ
t _{pd} (s)	2.5 V ± 0.2 V	Open	500 Ω	3.6 V or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	5.5 V or GND	50 pF	
t _{PLZ} /t _{PZL}	2.5 V ± 0.2 V	2 × VCC	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × VCC	500 Ω	GND	50 pF	0.3 V
t _{PHZ} /t _{PZH}	2.5 V ± 0.2 V	Open	500 Ω	3.6 V	30 pF	0.15 V
	3.3 V ± 0.3 V	Open	500 Ω	5.5 V	50 pF	0.3 V



- NOTES:
- B. C_L includes probe and jig capacitance.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - E. The outputs are measured one at a time with one transition per measurement.
 - F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - G. t_{PZL} and t_{PZH} are the same as t_{en}.
 - H. t_{PLH} and t_{PHL} are the same as t_{pd}(s). The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 - I. All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

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TYPICAL CHARACTERISTICS

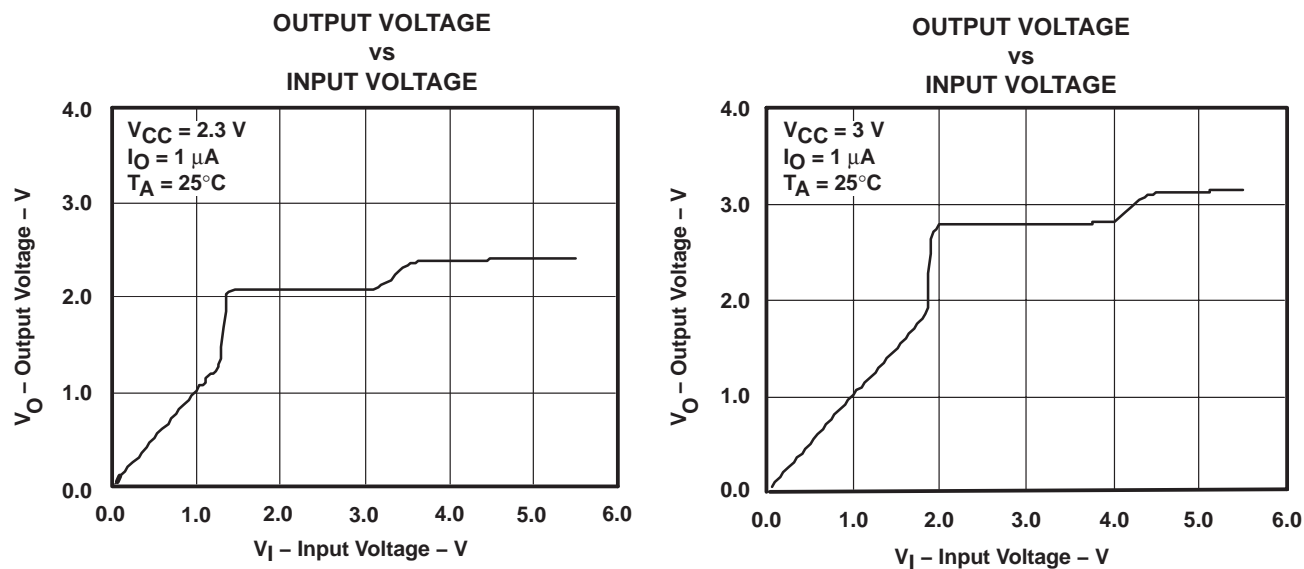


Figure 3. Data Output Voltage vs Data Input Voltage

TYPICAL CHARACTERISTICS (continued)

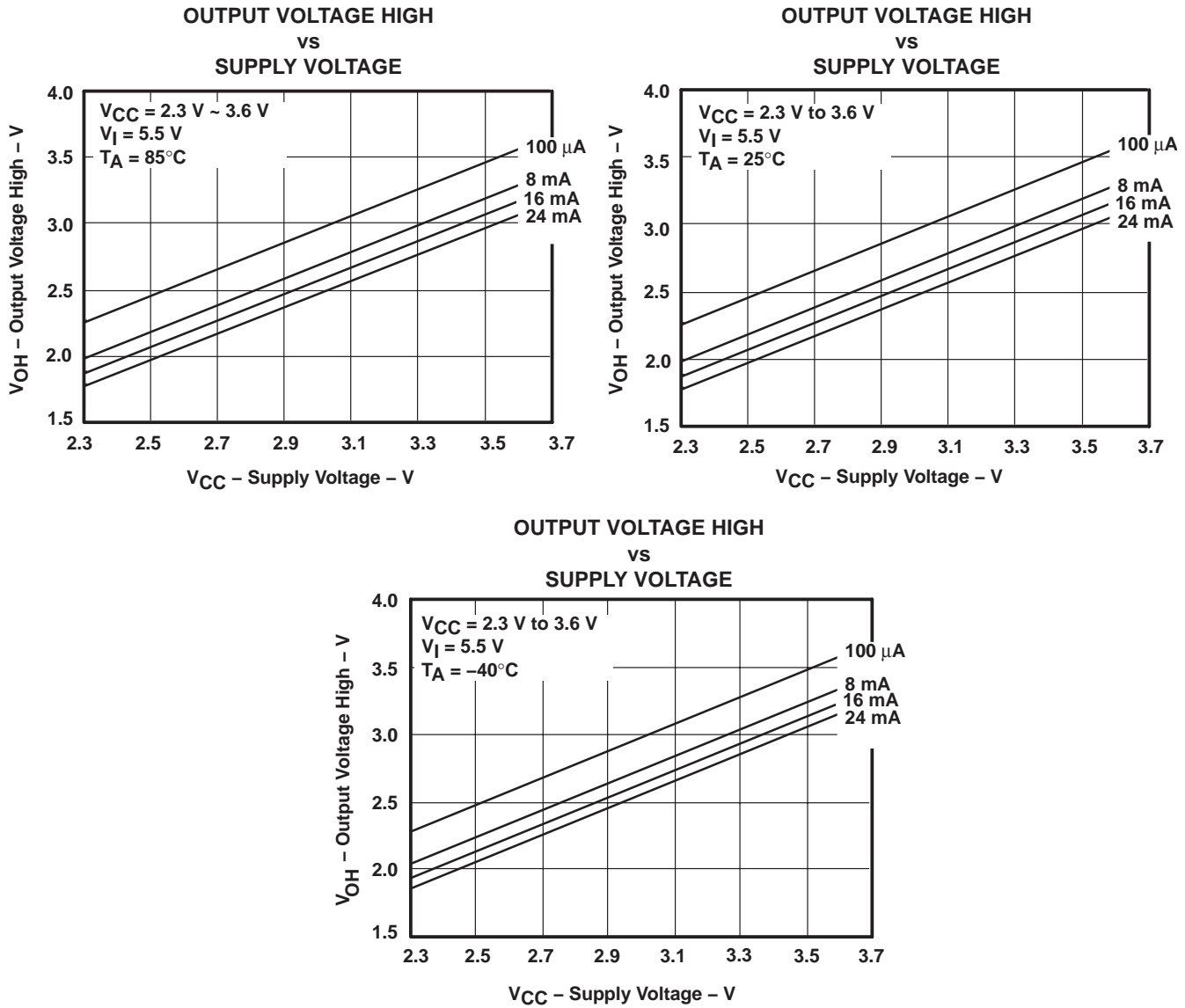
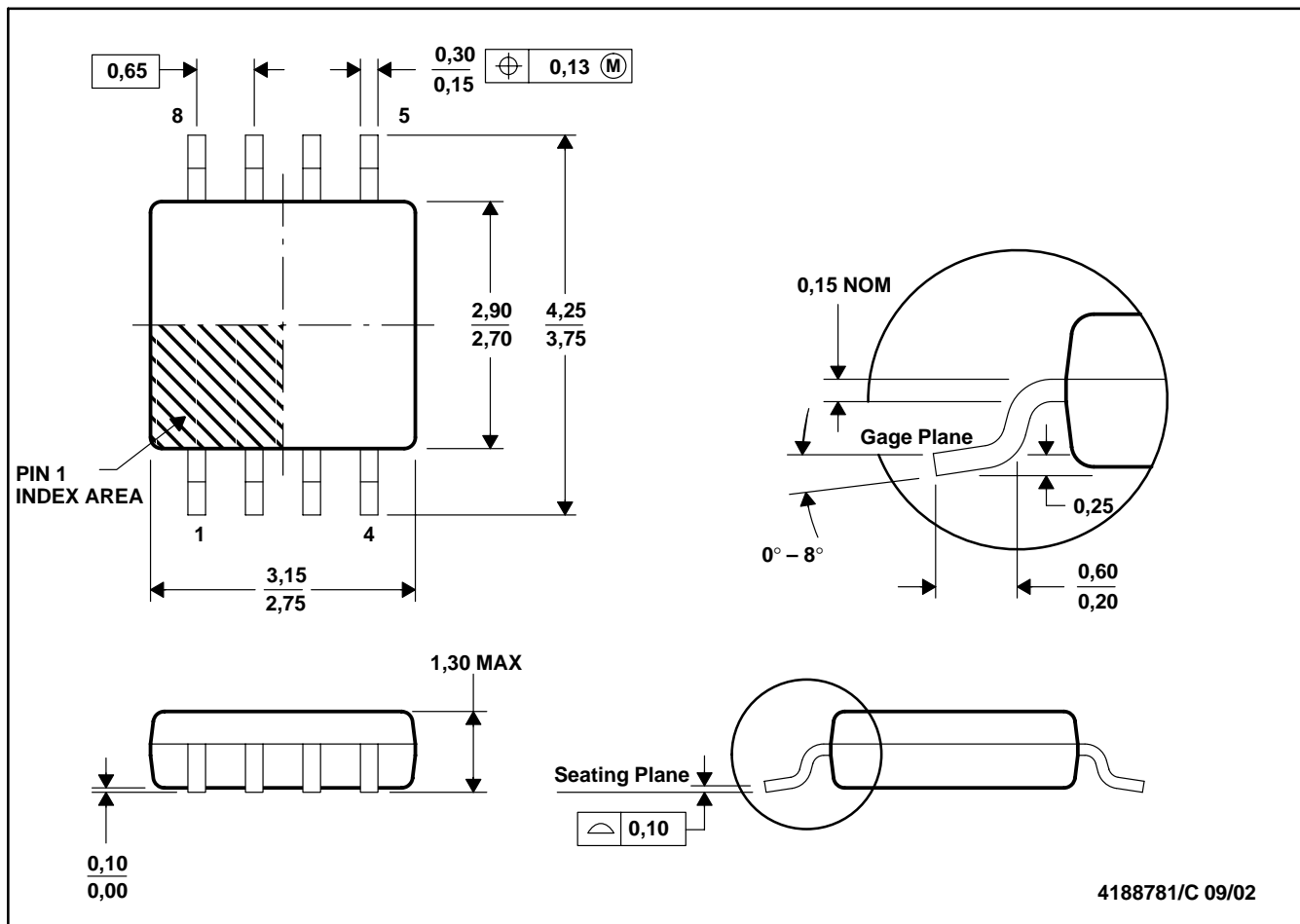


Figure 4. V_{OH} Values

DCT (R-PDSO-G8)

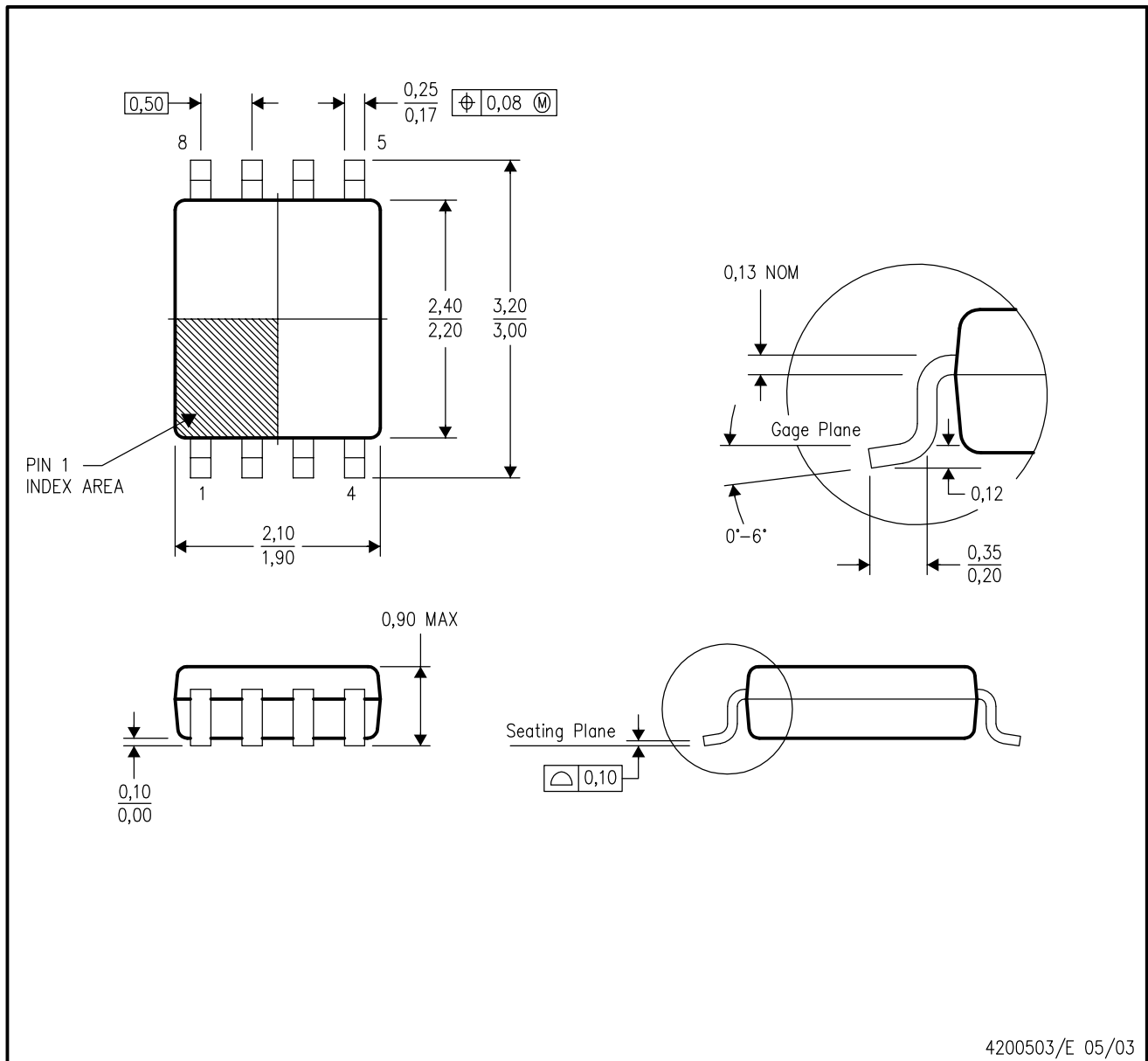
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion
 - D. Falls within JEDEC MO-187 variation DA.

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation CA.

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