

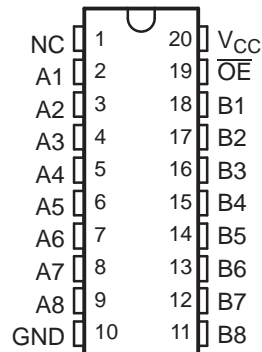
8-BIT FET BUS SWITCH 2.5-V/3.3-V LOW-VOLTAGE WITH 5-V-TOLERANT LEVEL SHIFTER

Check for Samples: [SN74CB3T3245](#)

FEATURES

- Standard '245-Type Pinout
- Output Voltage Translation Tracks V_{CC}
- Supports Mixed-Mode Signal Operation on All Data I/O Ports
 - 5-V Input Down to 3.3-V Output Level Shift With 3.3-V V_{CC}
 - 5-V/3.3-V Input Down to 2.5-V Output Level Shift With 2.5-V V_{CC}
- 5-V-Tolerant I/Os With Device Powered Up or Powered Down
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{on}) Characteristics ($r_{on} = 5 \Omega$ Typ)
- Low Input/Output Capacitance Minimizes Loading ($C_{io(OFF)} = 5 \text{ pF}$ Typ)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ($I_{CC} = 40 \mu\text{A}$ Max)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Digital Applications: Level Translation, PCI Interface, USB Interface, Memory Interleaving, Bus Isolation
- Ideal for Low-Power Portable Equipment

DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

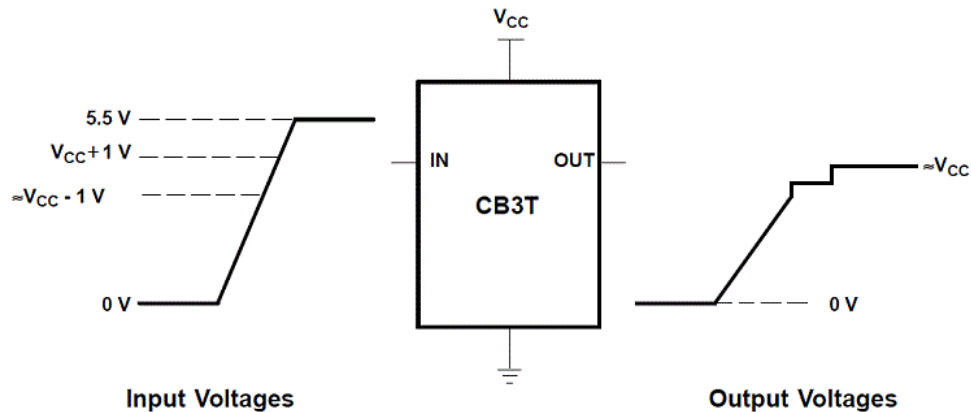
DESCRIPTION/ORDERING INFORMATION

The SN74CB3T3245 is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC} . The SN74CB3T3245 supports systems using 5-V TTL, 3.3-V LVTTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see [Figure 1](#)).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)



If the input high voltage (V_{IH}) level is greater than or equal to $V_{CC} + 1V$, and less than or equal to 5.5 V, the output high voltage (V_{OH}) level will be equal to approximately the V_{CC} voltage level.

Figure 1. Typical DC Voltage Translation Characteristics

The SN74CB3T3245 is an 8-bit bus switch with a single output-enable (\overline{OE}) input and a standard '245 pinout. When \overline{OE} is low, the 8-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the 8-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

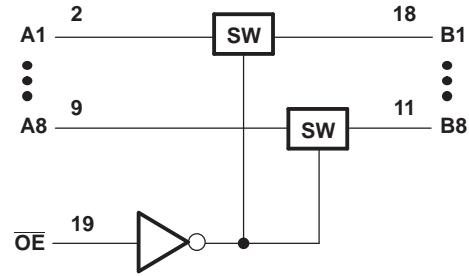
T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SOIC – DW	Tube	SN74CB3T3245DW	CB3T3245
		Tape and reel	SN74CB3T3245DWR	
	SSOP (QSOP) – DBQ	Tape and reel	SN74CB3T3245DBQR	CB3T3245
		Tube	SN74CB3T3245PW	KS245
	TSSOP – PW	Tape and reel	SN74CB3T3245PWR	
		TVSOP – DGV	Tape and reel	SN74CB3T3245DGVR

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

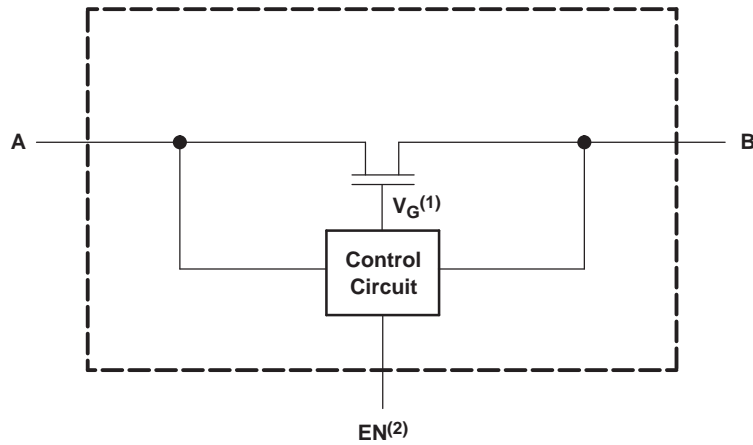
Table 1. FUNCTION TABLE

INPUT \overline{OE}	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

LOGIC DIAGRAM (POSITIVE LOGIC)



SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



- 1) Gate Voltage (V_G) is approximately equal to V_{CC} + V_T when the switch is ON and V_I > (V_{CC} + V_T).
- 2) EN is the internal enable signal applied to the switch.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾	-0.5	7	V
V _{IN}	Control input voltage range ⁽²⁾ ⁽³⁾	-0.5	7	V
V _{I/O}	Switch I/O voltage range ⁽²⁾ ⁽³⁾ ⁽⁴⁾	-0.5	7	V
I _{IK}	Control input clamp current	V _{IN} < 0		-50 mA
I _{I/OK}	I/O port clamp current	V _{I/O} < 0		-50 mA
I _{I/O}	ON-state switch current ⁽⁵⁾			±128 mA
Continuous current through V _{CC} or GND				±100 mA
θ _{JA}	Package thermal impedance ⁽⁶⁾	DBQ package		68
		DGV package		92
		DW package		58
		PW package		83
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for V_{I/O}.
- (5) I_I and I_O are used to denote specific conditions for I_{I/O}.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.3	3.6	V
V _{IH}	High-level control input voltage	V _{CC} = 2.3 V to 2.7 V		1.7
		V _{CC} = 2.7 V to 3.6 V		2
V _{IL}	Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V		0
		V _{CC} = 2.7 V to 3.6 V		0
V _{I/O}	Data input/output voltage	0	5.5	V
T _A	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V_{IK}		$V_{CC} = 3\text{ V}$, $I_I = -18\text{ mA}$			-1.2	V
V_{OH}		See Figure 3 and Figure 4				
I_{IN}	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_{IN} = 3.6\text{ V}$ to 5.5 V or GND			±10	µA
I_I		$V_{CC} = 3.6\text{ V}$, Switch ON, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC} - 0.7\text{ V}$ to 5.5 V		±20	µA
			$V_I = 0.7\text{ V}$ to $V_{CC} - 0.7\text{ V}$		-40	
			$V_I = 0$ to 0.7 V		±5	
I_{OZ} ⁽³⁾		$V_{CC} = 3.6\text{ V}$, $V_O = 0$ to 5.5 V , $V_I = 0$, Switch OFF, $V_{IN} = V_{CC}$ or GND			±10	µA
I_{off}		$V_{CC} = 0$, $V_O = 0$ to 5.5 V , $V_I = 0$,			10	µA
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_{I/O} = 0$, Switch ON or OFF, $V_{IN} = V_{CC}$ or GND	$V_I = V_{CC}$ or GND		40	µA
			$V_I = 5.5\text{ V}$		40	
ΔI_{CC} ⁽⁴⁾	Control inputs	$V_{CC} = 3\text{ V}$ to 3.6 V , One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND			300	µA
C_{in}	Control inputs	$V_{CC} = 3.3\text{ V}$, $V_{IN} = V_{CC}$ or GND		4		pF
$C_{io(OFF)}$		$V_{CC} = 3.3\text{ V}$, $V_{I/O} = 5.5\text{ V}$, 3.3 V , or GND, Switch OFF, $V_{IN} = V_{CC}$ or GND		5		pF
$C_{io(ON)}$		$V_{CC} = 3.3\text{ V}$, Switch ON, $V_{IN} = V_{CC}$ or GND	$V_{I/O} = 5.5\text{ V}$ or 3.3 V		5	pF
			$V_{I/O} = \text{GND}$		13	
r_{on} ⁽⁵⁾		$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$, $V_I = 0$	$I_O = 24\text{ mA}$	5	8.5	Ω
			$I_O = 16\text{ mA}$	5	8.5	
		$V_{CC} = 3\text{ V}$, $V_I = 0$	$I_O = 64\text{ mA}$	5	7	
			$I_O = 32\text{ mA}$	5	7	

(1) V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.

(2) All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

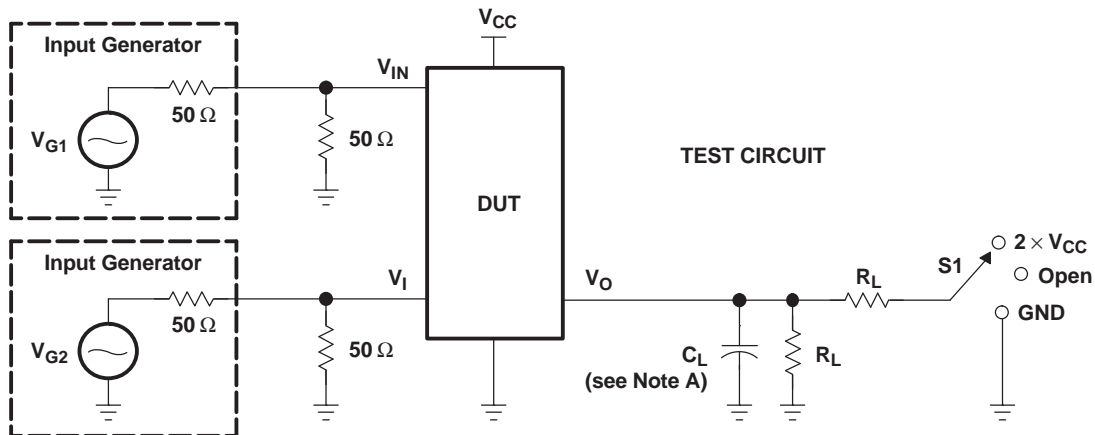
Switching Characteristics

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

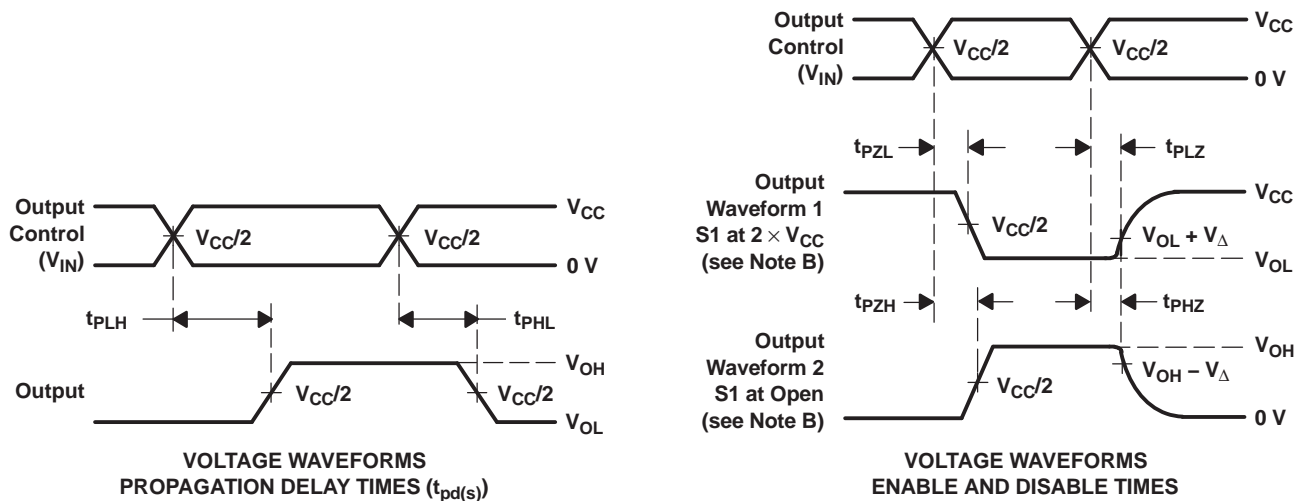
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd} ⁽¹⁾	A or B	B or A	0.15		0.25		ns
t_{en}	\overline{OE}	A or B	1	10.5	1	8	ns
t_{dis}	\overline{OE}	A or B	1	5.5	1	7.5	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION



TEST	V _{CC}	S1	R _L	V _I	C _L	V _Δ
t _{pd(s)}	2.5 V ± 0.2 V	Open	500 Ω	3.6 V or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	5.5 V or GND	50 pF	
t _{PLZ} /t _{PZL}	2.5 V ± 0.2 V	2 × V _{CC}	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V _{CC}	500 Ω	GND	50 pF	0.3 V
t _{PHZ} /t _{PZH}	2.5 V ± 0.2 V	Open	500 Ω	3.6 V	30 pF	0.15 V
	3.3 V ± 0.3 V	Open	500 Ω	5.5 V	50 pF	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - t_{PZL} and t_{PZH} are the same as t_{en}.
 - t_{PLH} and t_{PHL} are the same as t_{pd(s)}. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 - All parameters and waveforms are not applicable to all devices.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

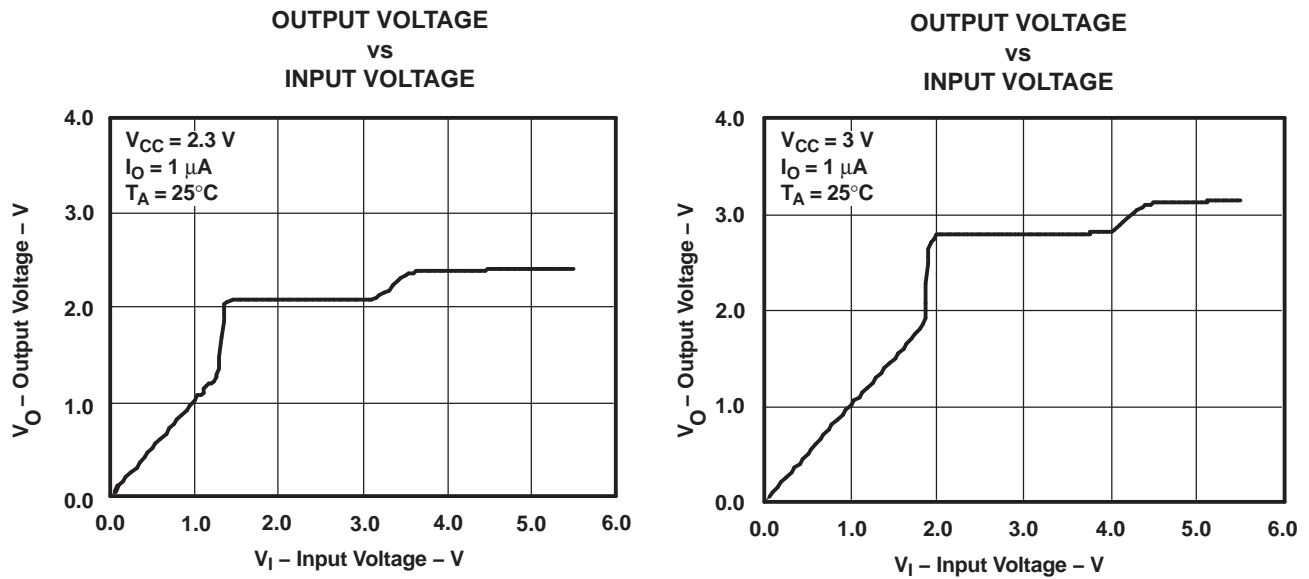
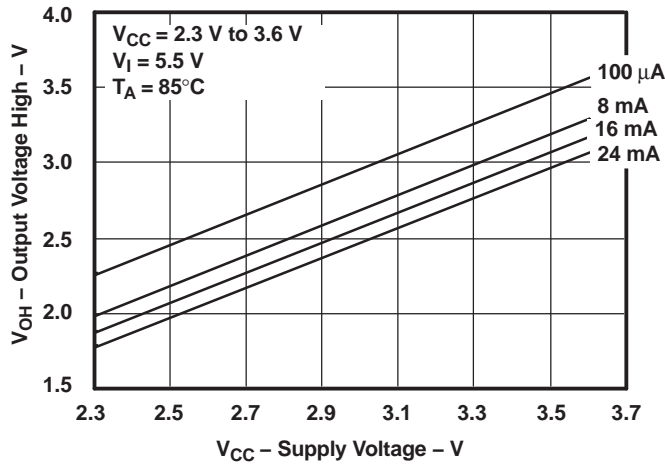


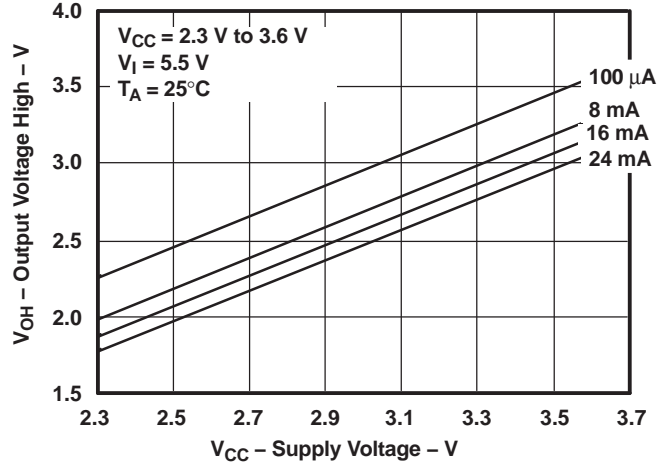
Figure 3. Data Output Voltage vs Data Input Voltage

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE



OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE



OUTPUT VOLTAGE HIGH
vs
SUPPLY VOLTAGE

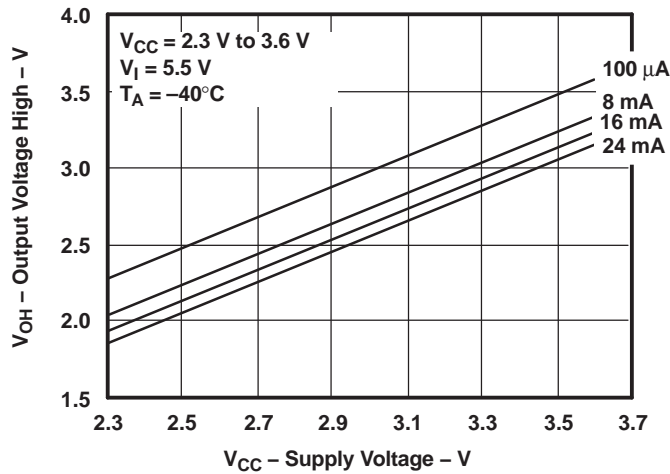


Figure 4. V_{OH} Values

REVISION HISTORY

Changes from Original (March 2005) to Revision A	Page
• Updated graphic note and picture in figure 1.	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74CB3T3245DGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples
SN74CB3T3245DBQR	ACTIVE	SSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3T3245	Samples
SN74CB3T3245DGV	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples
SN74CB3T3245DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245	Samples
SN74CB3T3245DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245	Samples
SN74CB3T3245DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245	Samples
SN74CB3T3245DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245	Samples
SN74CB3T3245PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples
SN74CB3T3245PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples
SN74CB3T3245PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples
SN74CB3T3245PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples
SN74CB3T3245PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples
SN74CB3T3245PWG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T3245DBQR	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CB3T3245DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3T3245DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74CB3T3245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T3245DBQR	SSOP	DBQ	20	2500	367.0	367.0	38.0
SN74CB3T3245DGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74CB3T3245DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74CB3T3245PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

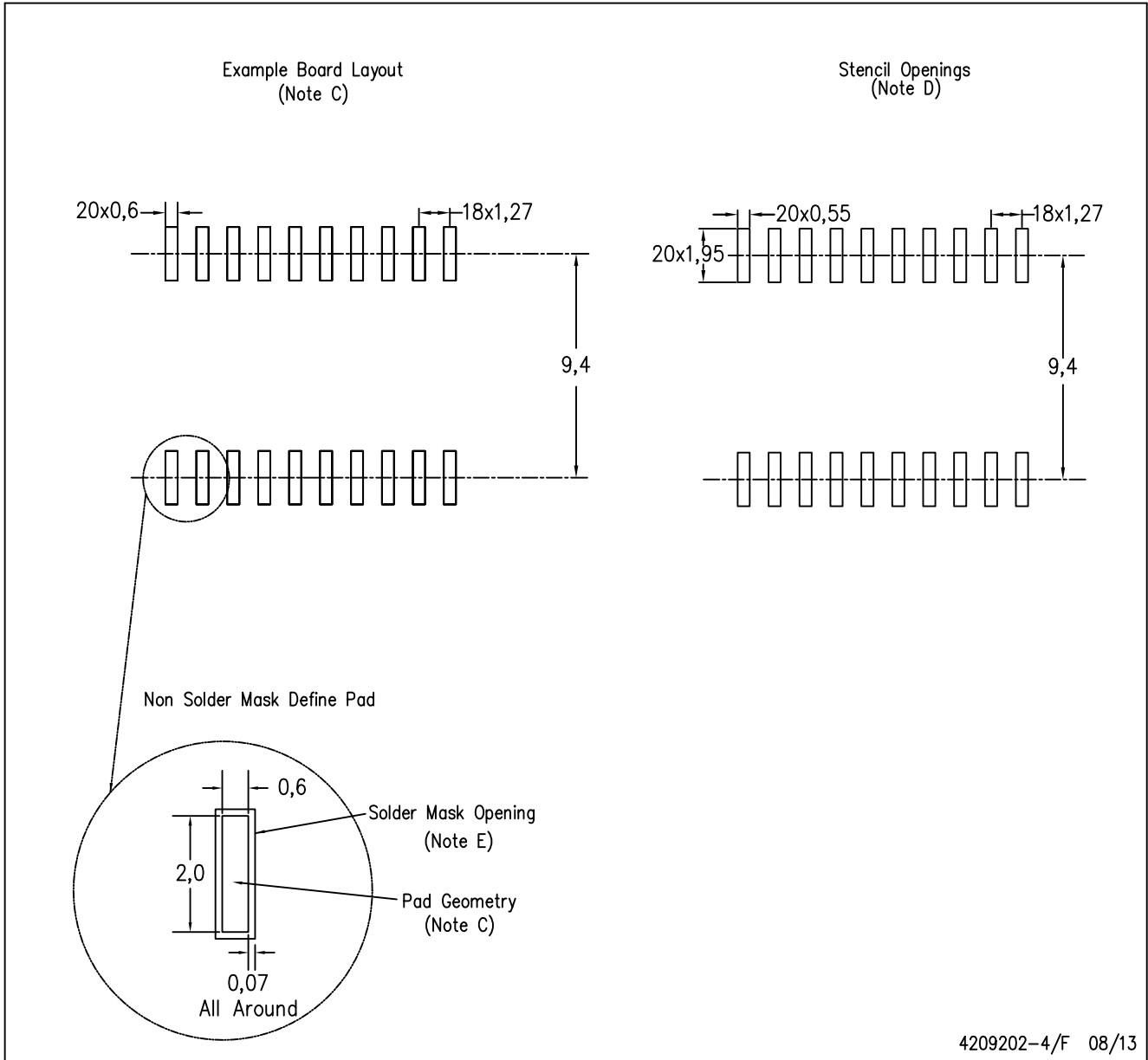
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

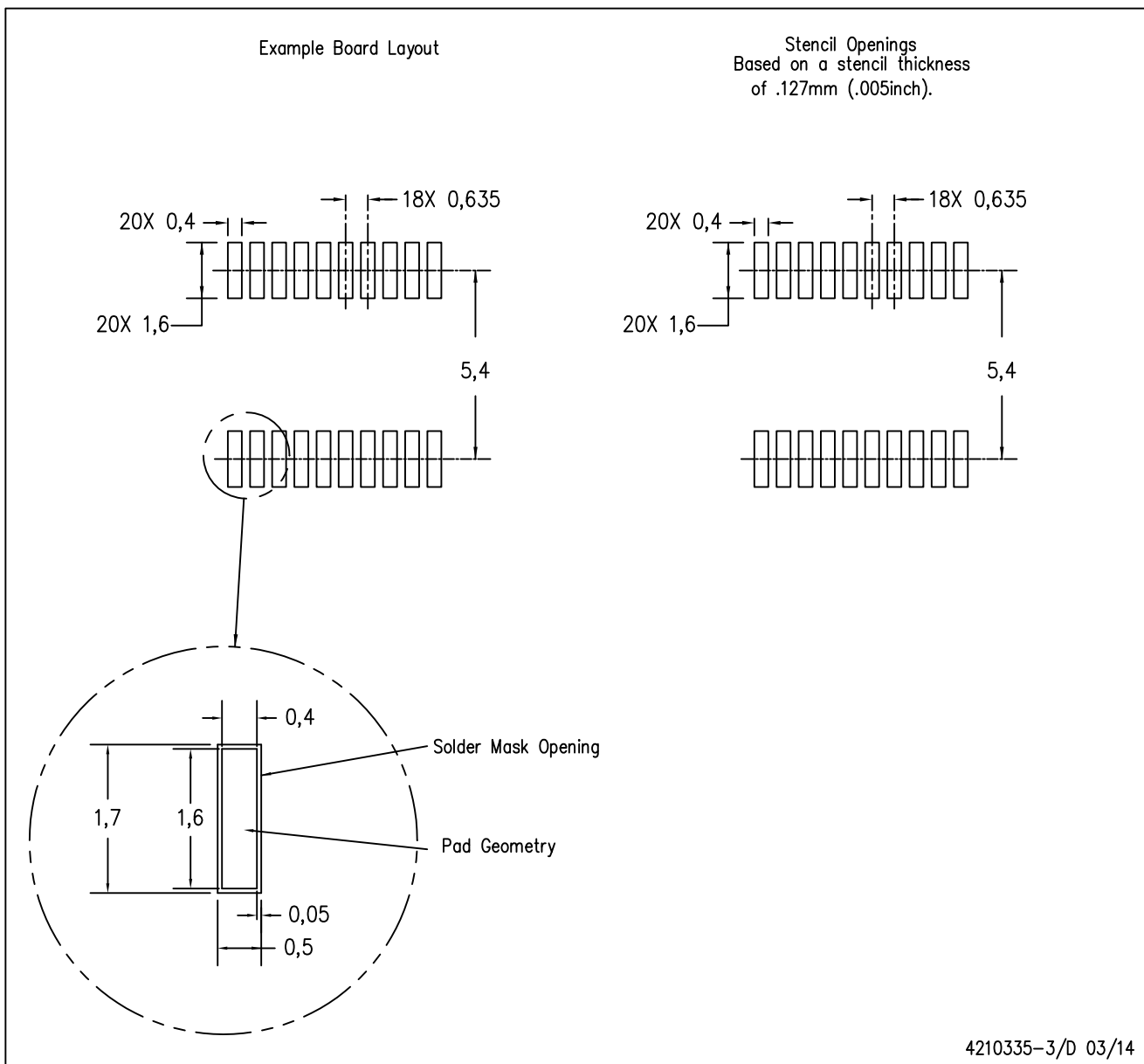


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- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R-PDSO-G20)

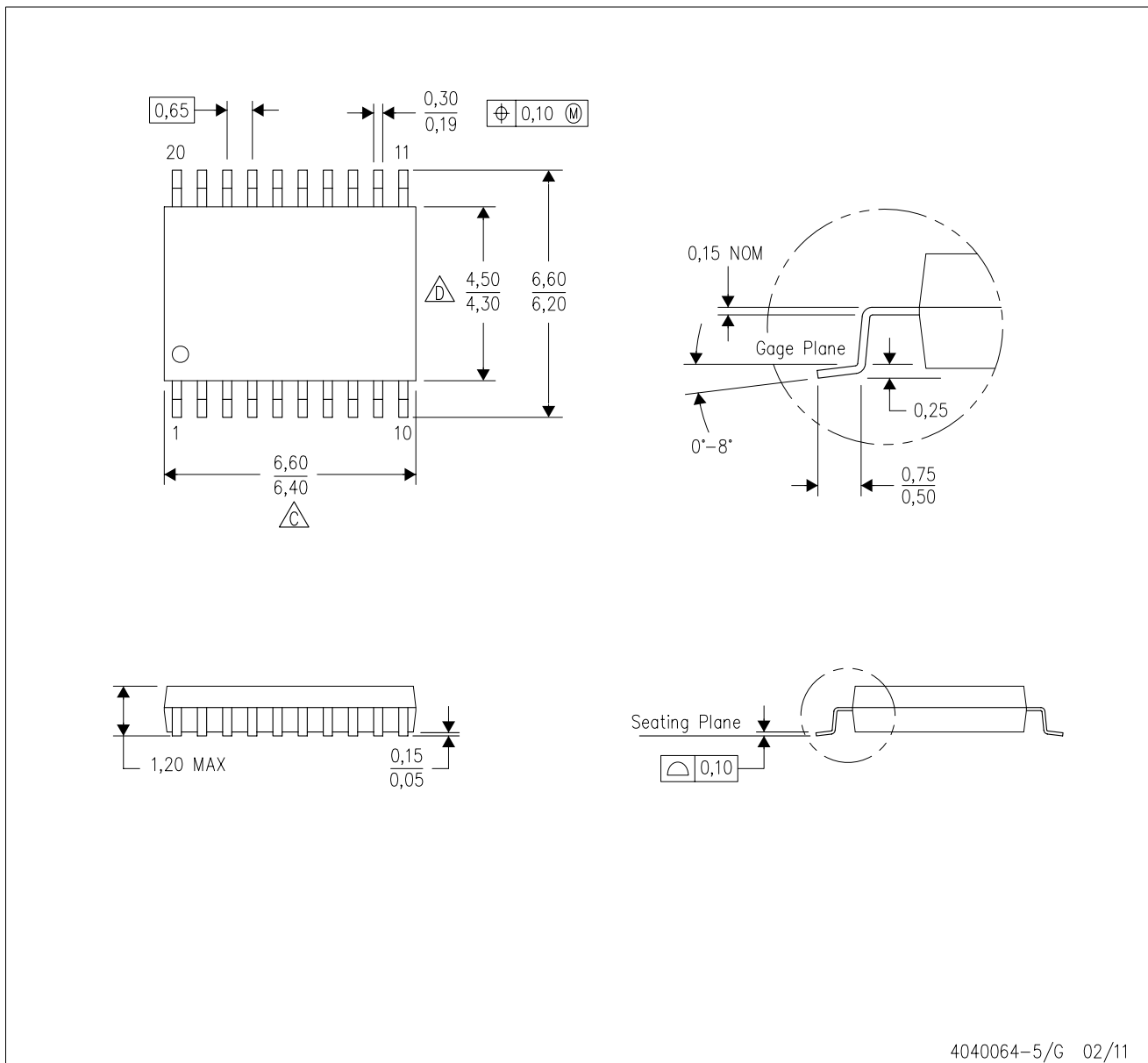
PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

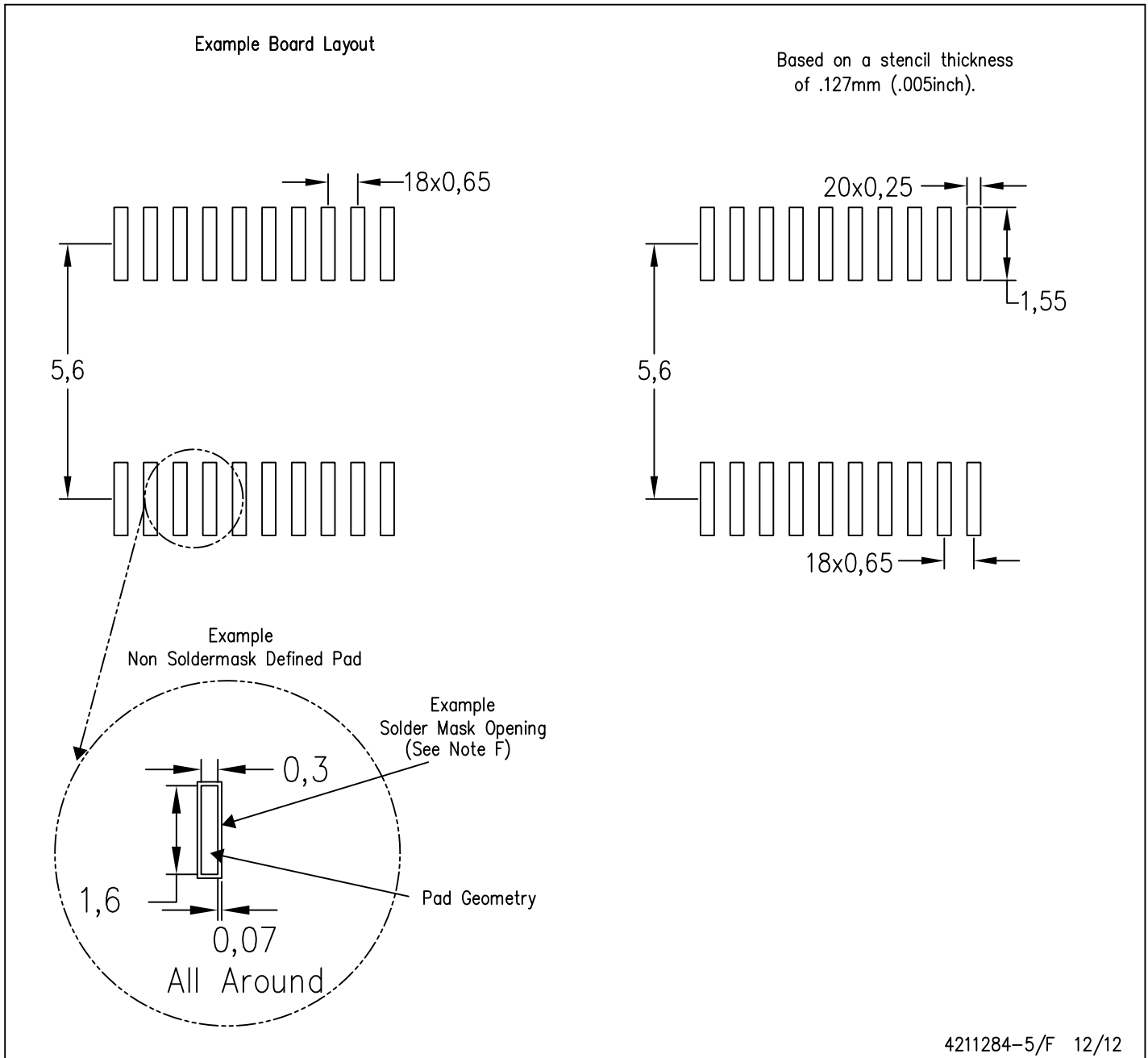


4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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