

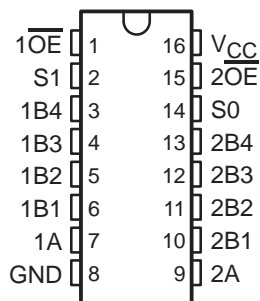
SN74CB3Q3253

DUAL 1-OF-4 FET MULTIPLEXER/DEMULTIPLEXER 2.5-V/3.3-V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH

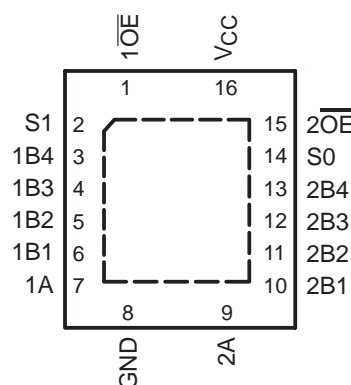
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- High-Bandwidth Data Path (Up To 500 MHz†)
 - 5-V Tolerant I/Os with Device Powered-Up or Powered-Down
 - Low and Flat ON-State Resistance (r_{ON}) Characteristics Over Operating Range ($r_{ON} = 4 \Omega$ Typical)
 - Rail-to-Rail Switching on Data I/O Ports
 - 0- to 5-V Switching With 3.3-V V_{CC}
 - 0- to 3.3-V Switching With 2.5-V V_{CC}
 - Bidirectional Data Flow, With Near-Zero Propagation Delay
 - Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{IO(OFF)} = 3.5 \text{ pF}$ Typical)
 - Fast Switching Frequency ($f_{OE} = 20 \text{ MHz}$ Max)
- † For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C*, *CB3T*, and *CB3Q Signal-Switch Families*, literature number SCDA008.
- Data and Control Inputs Provide Undershoot Clamp Diodes
 - Low Power Consumption ($I_{CC} = 0.6 \text{ mA}$ Typical)
 - V_{CC} Operating Range From 2.3 V to 3.6 V
 - Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
 - Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs
 - I_{off} Supports Partial-Power-Down Mode Operation
 - Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
 - ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
 - Supports Both Digital and Analog Applications: USB Interface, Differential Signal Interface Bus Isolation, Low-Distortion Signal Gating

DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



description/ordering information

The SN74CB3Q3253 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{ON}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3253 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.



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description/ordering information (continued)

The SN74CB3Q3253 is organized as two 1-of-4 multiplexers/demultiplexers with separate output-enable ($\overline{1OE}$, $\overline{2OE}$) inputs. The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. When \overline{OE} is low, the associated multiplexer/demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the associated multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Tape and reel	SN74CB3Q3253RGYR	BU253
	SSOP (QSOP) – DBQ	Tape and reel	SN74CB3Q3253DBQR	BU253
	TSSOP – PW	Tube	SN74CB3Q3253PW	BU253
		Tape and reel	SN74CB3Q3253PWR	
	TVSOP – DGV	Tape and reel	SN74CB3Q3253DGVR	BU253

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
 (each multiplexer/demultiplexer)

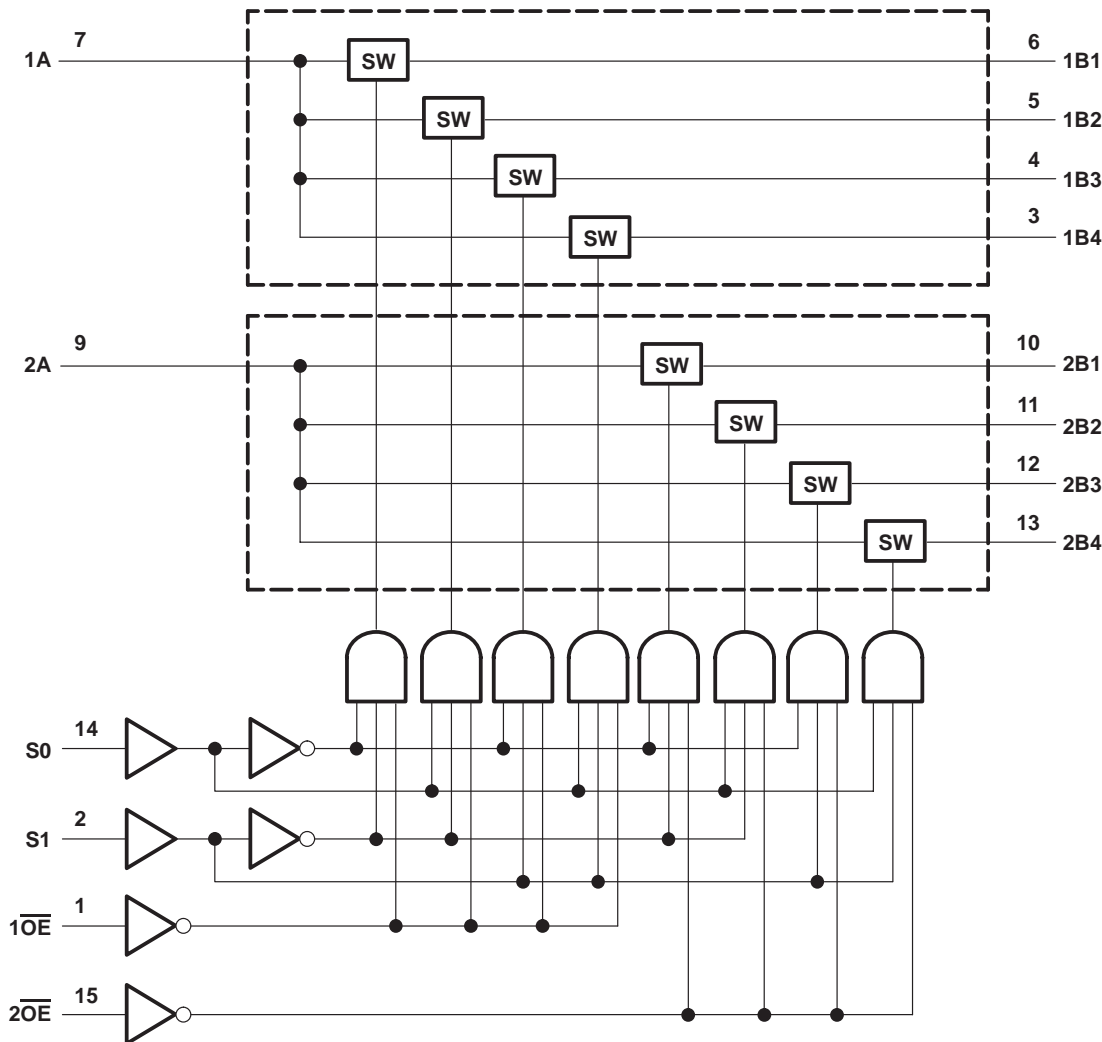
INPUTS			INPUT/OUTPUT A	FUNCTION
\overline{OE}	S1	S0		
L	L	L	B1	A port = B1 port
L	L	H	B2	A port = B2 port
L	H	L	B3	A port = B3 port
L	H	H	B4	A port = B4 port
H	X	X	Z	Disconnect



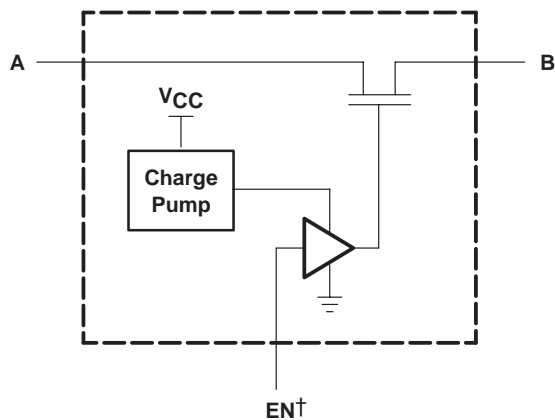
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logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	-0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	-0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	-50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	-50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±64 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DBQ package	90°C/W
(see Note 5): DGV package	120°C/W
(see Note 5): PW package	108°C/W
(see Note 6): RGY package	39°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground unless otherwise specified.
 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
 4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.
 6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

		MIN	MAX	UNIT	
V_{CC}	Supply voltage	2.3	3.6	V	
V_{IH}	High-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	5.5	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2	5.5	
V_{IL}	Low-level control input voltage	$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0	0.8	
$V_{I/O}$	Data input/output voltage	0	5.5	V	
T_A	Operating free-air temperature	-40	85	°C	

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 3.6\text{ V}$,	$I_I = -18\text{ mA}$				-1.8	V
I_{IN}	Control inputs	$V_{CC} = 3.6\text{ V}$,	$V_{IN} = 0\text{ to }5.5\text{ V}$				± 1	μA
I_{OZ}^\ddagger		$V_{CC} = 3.6\text{ V}$,	$V_O = 0\text{ to }5.5\text{ V}$, $V_I = 0$,	Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$			± 1	μA
I_{off}		$V_{CC} = 0$,	$V_O = 0\text{ to }5.5\text{ V}$,	$V_I = 0$			1	μA
I_{CC}		$V_{CC} = 3.6\text{ V}$,	$I_{I/O} = 0$, Switch ON or OFF,	$V_{IN} = V_{CC}\text{ or GND}$		0.6	2	mA
ΔI_{CC}^\S	Control inputs	$V_{CC} = 3.6\text{ V}$,	One input at 3 V,	Other inputs at $V_{CC}\text{ or GND}$			30	μA
I_{CCD}^\parallel	Per control input	$V_{CC} = 3.6\text{ V}$, Control input switching at 50% duty cycle	A and B ports open,	\overline{OE} input		0.15	0.16	mA/
				S input		0.04	0.05	MHz
C_{in}	Control inputs	$V_{CC} = 3.3\text{ V}$,	$V_{IN} = 5.5\text{ V}, 3.3\text{ V},\text{ or }0$			2.5	3.5	pF
$C_{io(OFF)}$	A port	$V_{CC} = 3.3\text{ V}$,	Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$,	$V_{I/O} = 5.5\text{ V}, 3.3\text{ V},\text{ or }0$		8	11	pF
	B port	$V_{CC} = 3.3\text{ V}$,	Switch OFF, $V_{IN} = V_{CC}\text{ or GND}$,	$V_{I/O} = 5.5\text{ V}, 3.3\text{ V},\text{ or }0$		3.5	4.5	pF
$C_{io(ON)}$		$V_{CC} = 3.3\text{ V}$,	Switch ON, $V_{IN} = V_{CC}\text{ or GND}$,	$V_{I/O} = 5.5\text{ V}, 3.3\text{ V},\text{ or }0$		13	17	pF
$r_{on}^\#$		$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$,	$I_O = 30\text{ mA}$		4	10	Ω
			$V_I = 1.7\text{ V}$,	$I_O = -15\text{ mA}$		4.5	11	
		$V_{CC} = 3\text{ V}$	$V_I = 0$,	$I_O = 30\text{ mA}$		3.5	8	
			$V_I = 2.4\text{ V}$,	$I_O = -15\text{ mA}$		4	10	

V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.

† All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

¶ This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$f_{OE}\text{ or }f_{S}^\parallel$	\overline{OE} or S	A or B		10		20	MHz
t_{pd}^*	A or B	B or A		0.12		0.18	ns
$t_{pd(s)}$	S	A	1.5	6.7	1.5	5.9	ns
	S	B	1.5	6.7	1.5	5.9	
t_{en}	\overline{OE}	A or B	1.5	6.7	1.5	5.9	ns
	S	B	1	6.1	1	6.1	
t_{dis}	\overline{OE}	A or B	1	6.1	1	6.1	ns
	S	B	1	6.1	1	6.1	

¶ Maximum switching frequency for control input ($V_O > V_{CC}$, $V_I = 5\text{ V}$, $R_L \geq 1\text{ M}\Omega$, $C_L = 0$).

* The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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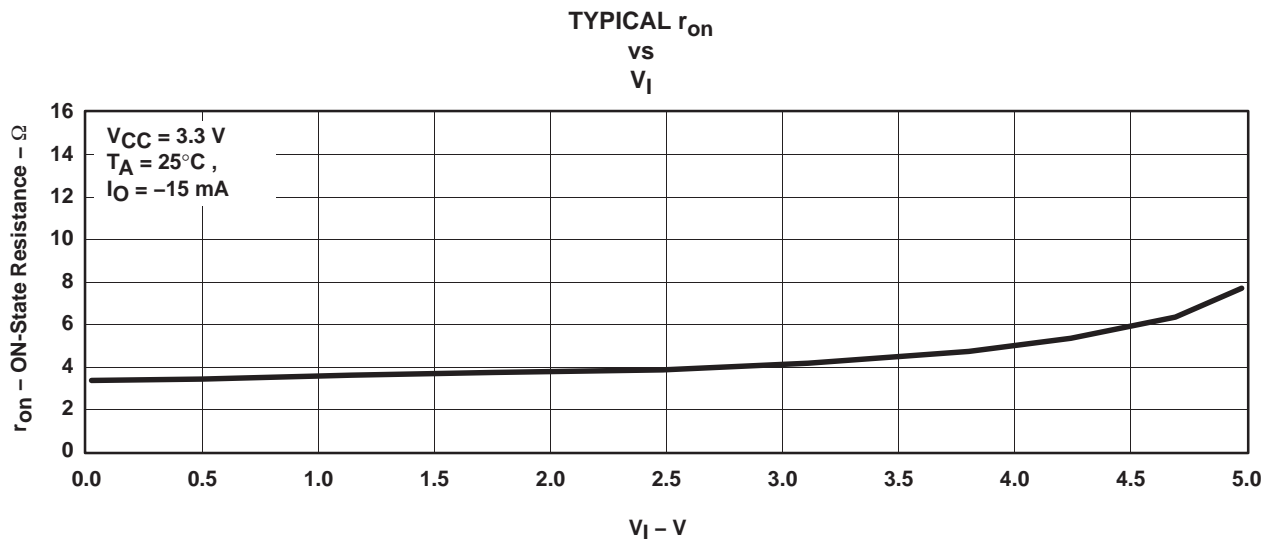


Figure 1. Typical r_{on} vs V_I , $V_{CC} = 3.3$ V and $I_O = -15$ mA

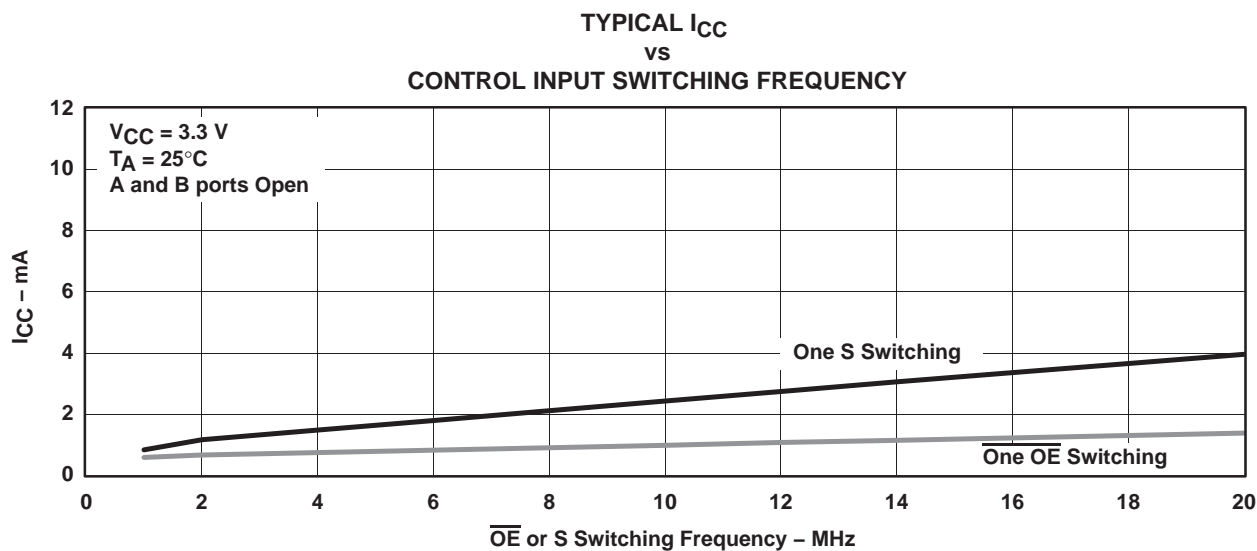
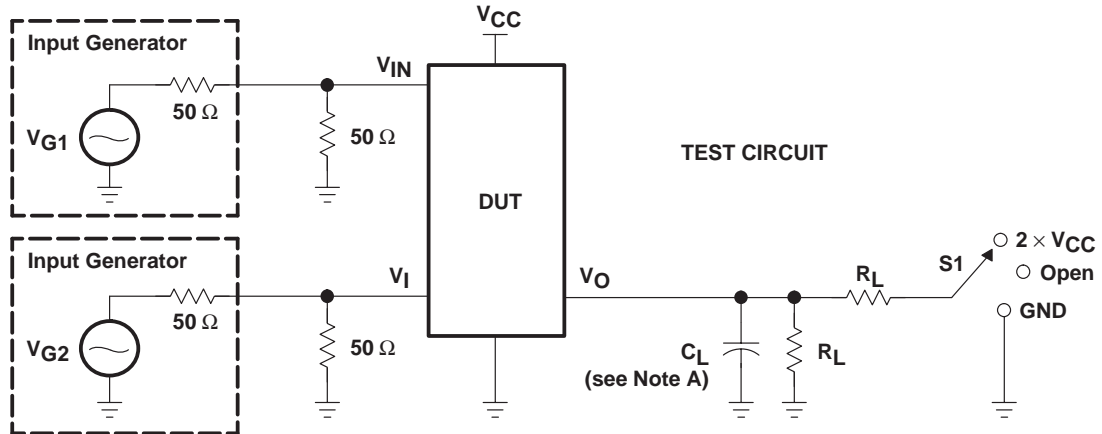


Figure 2. Typical I_{CC} vs \overline{OE} or S Switching Frequency, $V_{CC} = 3.3$ V

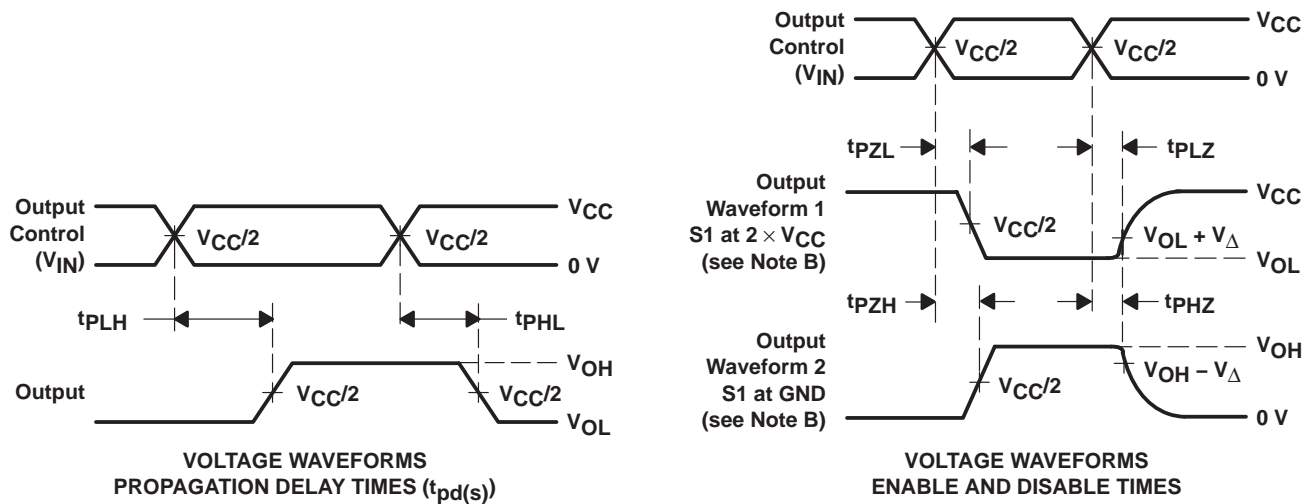
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PARAMETER MEASUREMENT INFORMATION



TEST	V _{CC}	S1	R _L	V _I	C _L	V _Δ
t _{pd} (s)	2.5 V ± 0.2 V	Open	500 Ω	V _{CC} or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	V _{CC} or GND	50 pF	
t _{PLZ} /t _{PZL}	2.5 V ± 0.2 V	2 × V _{CC}	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V _{CC}	500 Ω	GND	50 pF	0.3 V
t _{PHZ} /t _{PZH}	2.5 V ± 0.2 V	GND	500 Ω	V _{CC}	30 pF	0.15 V
	3.3 V ± 0.3 V	GND	500 Ω	V _{CC}	50 pF	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 F. t_{PZL} and t_{PZH} are the same as t_{en}.
 G. t_{PLH} and t_{PHL} are the same as t_{pd}(s). The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

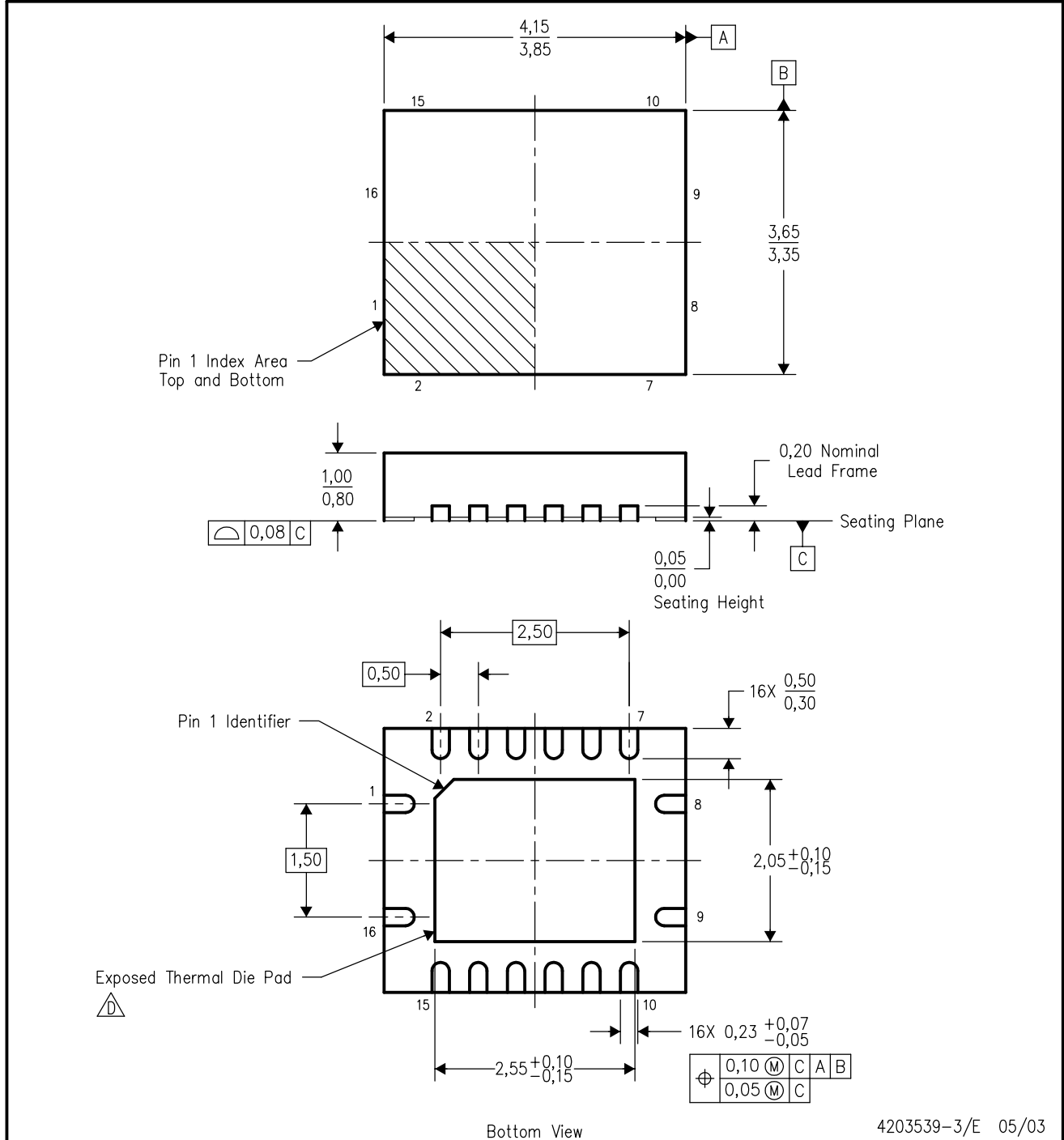



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

RGY (R-PQFP-N16)

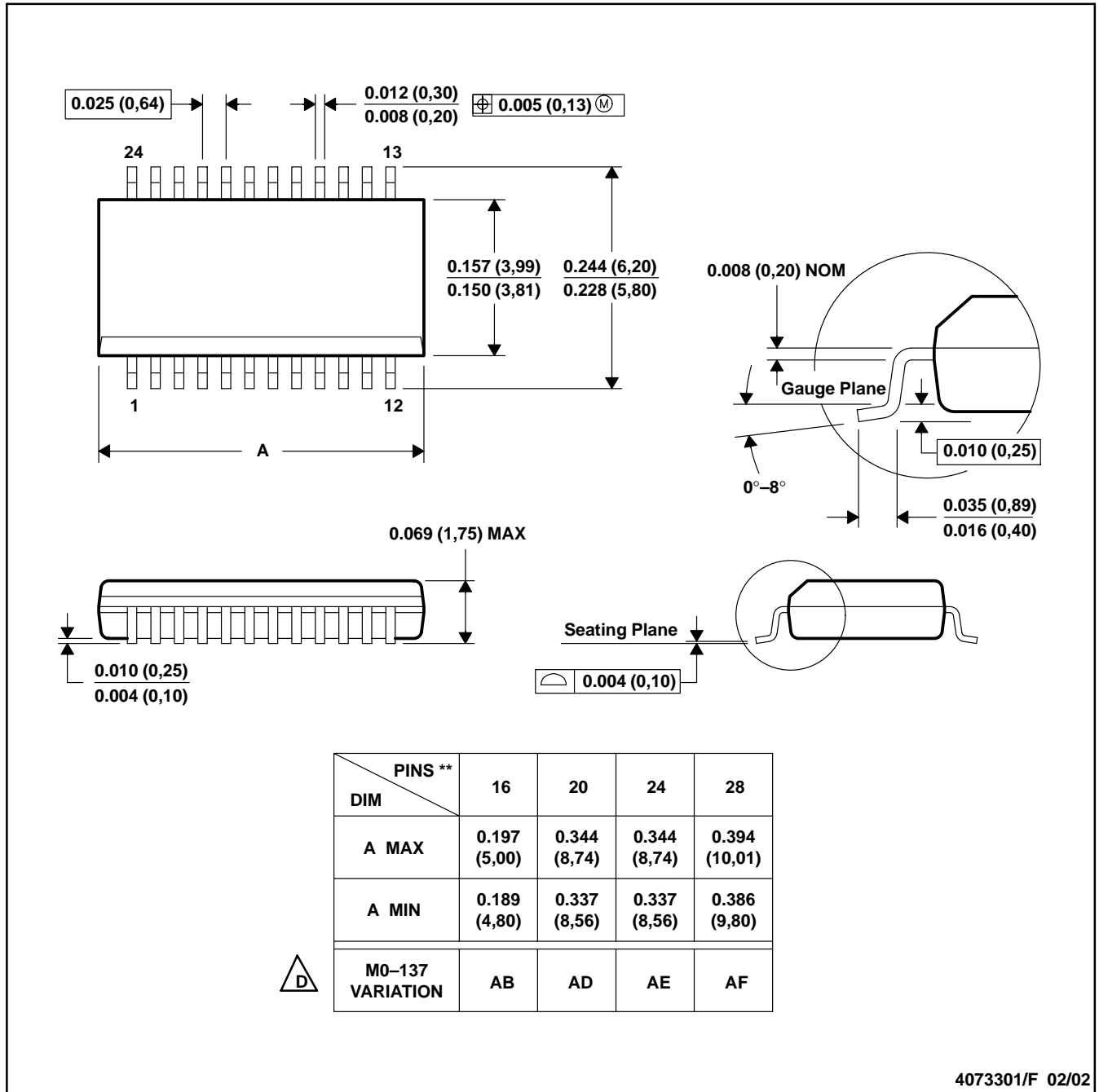
PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 -  The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - E. Package complies to JEDEC MO-241 variation BB.

DBQ (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE



4073301/F 02/02

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-137.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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