

FEATURES

- Member of the Texas Instruments Widebus™ Family
- SN74CB3Q Bus Switches Are Equivalent to IDTQS3VH Bus Switches
- 5-V Tolerant I/Os With Device Powered Up or Powered Down
- Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range ($r_{on} = 5 \Omega$ Typ)
- Rail-to-Rail Switching on Data I/O Ports
 - 0- to 5-V Switching With 3.3-V V_{CC}
 - 0- to 3.3-V Switching With 2.5-V V_{CC}
- B-Port Outputs Are Precharged by Bias Voltage (BIASV) to Minimize Signal Distortion During Live Insertion and Hot Plugging
- Supports PCI Hot Plug
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)} = 4$ pF Typ)
- Fast Switching Frequency ($f_{ON} = 20$ MHz Max)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ($I_{CC} = 0.75$ mA Typ)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: PCI Hot Plug, Hot Docking, Memory Interleaving, Bus Isolation, and Low-Distortion Signal Gating

DESCRIPTION/ORDERING INFORMATION

The SN74CB3Q16811 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q16811 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74CB3Q16811DL	CB3Q16811
		Tape and reel	SN74CB3Q16811DLR	
	TSSOP – DGG	Tape and reel	SN74CB3Q16811DGGR	CB3Q16811
	TVSOP – DGV	Tape and reel	SN74CB3Q16811DGVR	BW811

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74CB3Q16811 is organized as two 12-bit bus switches with separate output-enable ($\overline{1OE}$, $\overline{2OE}$) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When \overline{OE} is low, the associated 12-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the associated 12-bit bus switch is OFF, and a high-impedance state exists between the A and B ports. The B port is precharged to bias voltage (BIASV) through the equivalent of a 10-k Ω resistor when \overline{OE} is high or if the device is powered down ($V_{CC} = 0$ V).



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SN74CB3Q16811
24-BIT SWITCH WITH PRECHARGED OUTPUTS
2.5-V/3.3-V LOW-VOLTAGE FET BUS SWITCH

SCDS153B–OCTOBER 2003–REVISED MARCH 2005

During insertion (or removal) of a card into (or from) an active bus, the card's output voltage may be close to GND. When the connector pins make contact, the card's parasitic capacitance tries to force the bus signal to GND, creating a possible glitch on the active bus. This glitching effect can be reduced by using a bus switch with precharged bias voltage (BIASV) of the bus switch equal to the input threshold voltage level of the receivers on the active bus. This method ensures that any glitch produced by insertion (or removal) of the card does not cross the input threshold region of the receivers on the active bus, minimizing the effects of live-insertion noise.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry prevents damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DGG, DGV, OR DL PACKAGE
(TOP VIEW)

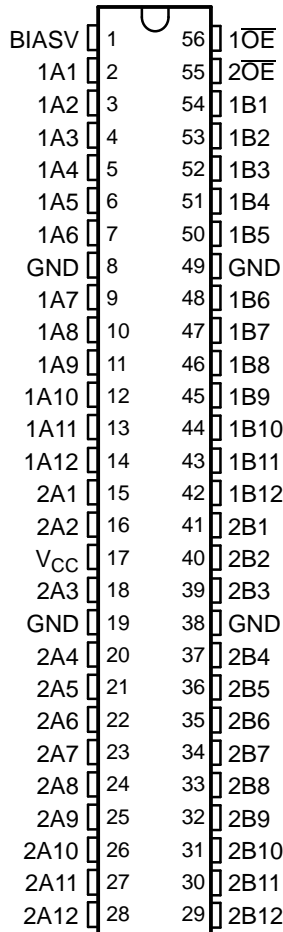
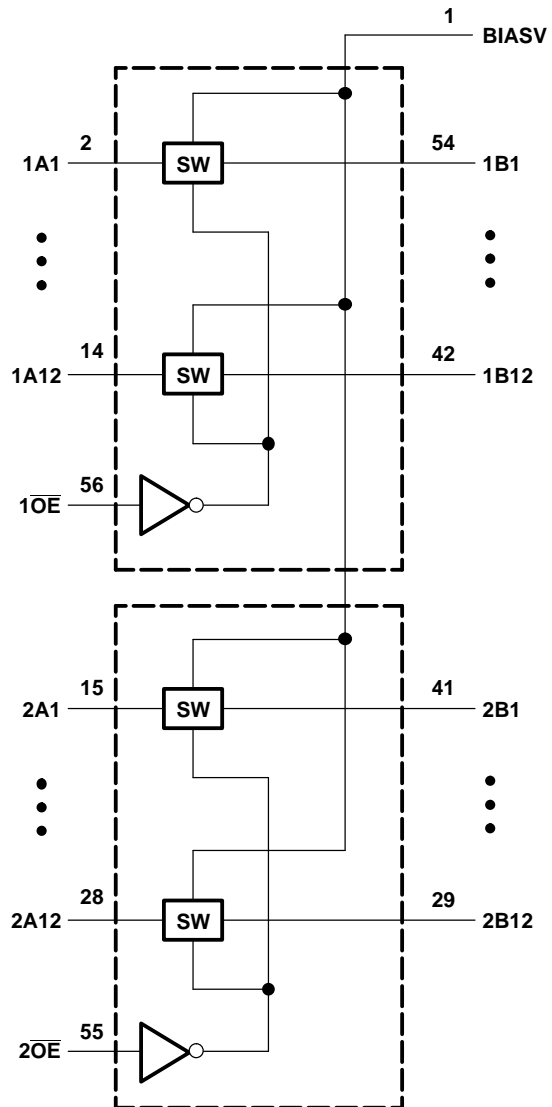


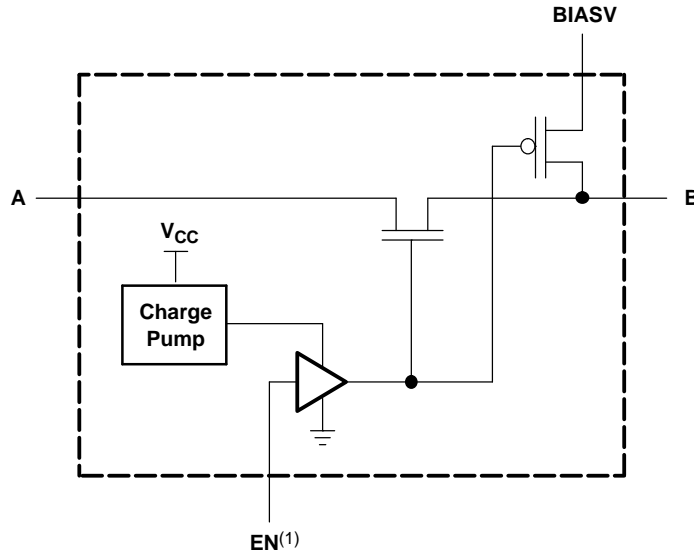
Table 1. FUNCTION TABLE
(EACH 12-BIT BUS SWITCH)

INPUT \overline{OE}	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect B port = BIASV

LOGIC DIAGRAM (POSITIVE LOGIC)



SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	4.6	V
BIASV	BIAS supply voltage range	-0.5	7	V
V _{IN}	Control input voltage range ⁽²⁾⁽³⁾	-0.5	7	V
V _{I/O}	Switch I/O voltage range ⁽²⁾⁽³⁾⁽⁴⁾	-0.5	7	V
I _{IK}	Control input clamp current		-50	mA
I _{I/OK}	I/O port clamp current		-50	mA
I _{I/O}	ON-state switch current ⁽⁵⁾		±64	mA
	Continuous current through V _{CC} or GND		±100	mA
θ _{JA}	Package thermal impedance ⁽⁶⁾	DGG package		64
		DGV package		48
		DL package		56
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for V_{I/O}.
- (5) I_I and I_O are used to denote specific conditions for I_{I/O}.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	2.3	3.6	V	
BIASV	Bias voltage	0	5	V	
V _{IH}	High-level control input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V _{CC} = 2.7 V to 3.6 V	2	5.5	
V _{IL}	Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V	0	0.7	V
		V _{CC} = 2.7 V to 3.6 V	0	0.8	
V _{I/O}	Data input/output voltage	0	5.5	V	
T _A	Operating free-air temperature	-40	85	°C	

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽²⁾	MAX	UNIT	
V _{IK}		V _{CC} = 3.6 V,	I _I = -18 mA				-1.8	V	
I _{IN}	Control inputs	V _{CC} = 3.6 V,	V _{IN} = 0 to 5.5 V				±1	µA	
I _O	B port	V _{CC} = 3.3 V,	BIASV = 2.4 V, V _O = 0,	Switch OFF, V _{IN} = V _{CC} or GND			0.2	mA	
I _{OZ} ⁽³⁾		V _{CC} = 3.6 V,	V _O = 0 to 5.5 V, V _I = 0,	Switch OFF, V _{IN} = V _{CC} or GND			±1	µA	
I _{off}		V _{CC} = 0,	V _O = 0 to 5.5 V, V _I = 0				1	µA	
I _{CC}		V _{CC} = 3.6 V,	I _{I/O} = 0, Switch ON or OFF,	V _{IN} = V _{CC} or GND			1	3	mA
ΔI _{CC} ⁽⁴⁾	Control inputs	V _{CC} = 3.6 V,	One input at 3 V,	Other inputs at V _{CC} or GND			30	µA	
I _{CCD} ⁽⁵⁾	Per control input	V _{CC} = 3.6 V,	A and B ports open, Control input switching at 50% duty cycle				0.38	0.45	mA/ MHz
C _{in}	Control inputs	V _{CC} = 3.3 V,	V _{IN} = 5.5 V, 3.3 V, or 0				3.5	5	pF
C _{io(OFF)}	A port	V _{CC} = 3.3 V,	Switch OFF, V _{IN} = V _{CC} or GND,	V _{I/O} = 5.5 V, 3.3 V, or 0			4	5	pF
C _{io(ON)}		V _{CC} = 3.3 V,	Switch ON, V _{IN} = V _{CC} or GND,	V _{I/O} = 5.5 V, 3.3 V, or 0			10	12.5	pF
r _{on} ⁽⁶⁾		V _{CC} = 2.3 V, TYP at V _{CC} = 2.5 V	V _I = 0,	I _O = 30 mA			5	8	Ω
			V _I = 1.7 V,	I _O = -15 mA			5	9	
		V _{CC} = 3 V	V _I = 0,	I _O = 30 mA			5	6.5	
			V _I = 2.4 V,	I _O = -15 mA			5	8	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.

(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	
f _{OE} ⁽¹⁾		\overline{OE}	A or B		10		20	MHz
t _{pd} ⁽²⁾		A or B	B or A		0.09		0.15	ns
t _{PZH}	BIASV = GND	\overline{OE}	A or B	1.5	8	1.5	8	ns
t _{PZL}	BIASV = 3 V			1.5	8	1.5	8	
t _{PHZ}	BIASV = GND	\overline{OE}	A or B	1	7.5	1	7.5	ns
t _{PLZ}	BIASV = 3 V			1	7.5	1	7.5	

- (1) Maximum switching frequency for control input (V_O > V_{CC}, V_I = 5 V, R_L ≥ 1 MΩ, C_L = 0)
 (2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

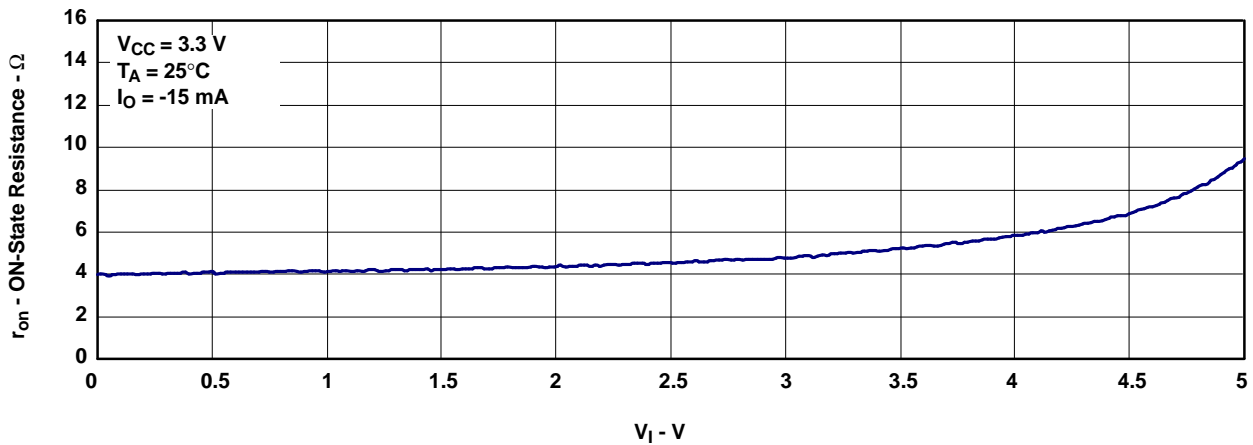


Figure 1. Typical r_{on} vs V_I

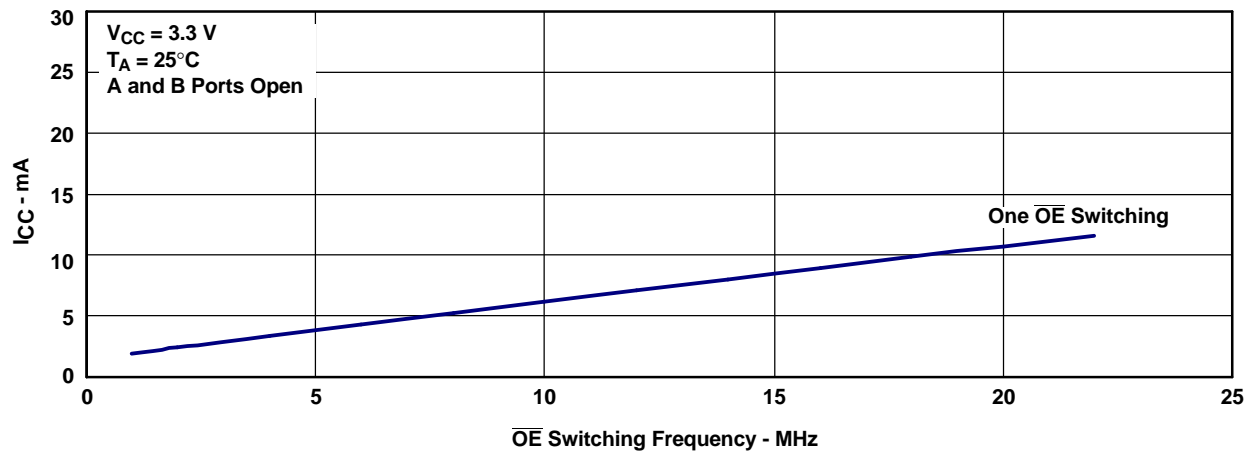
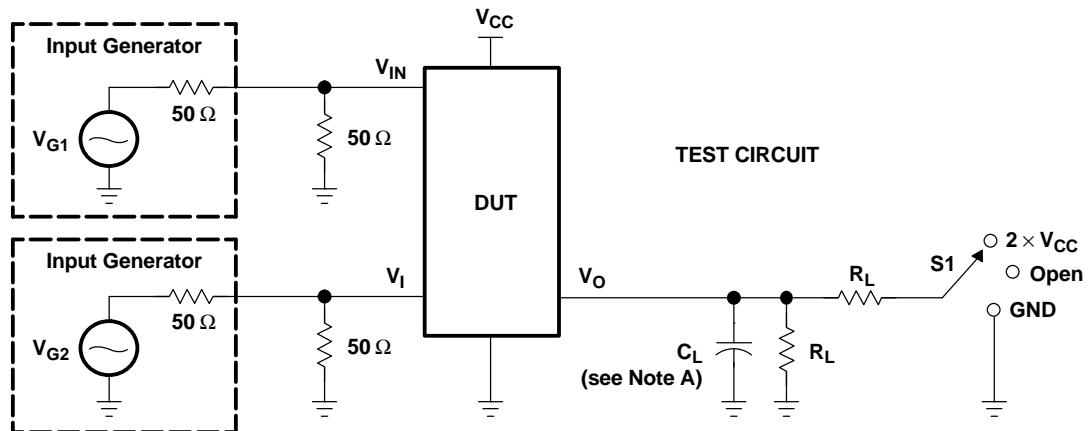
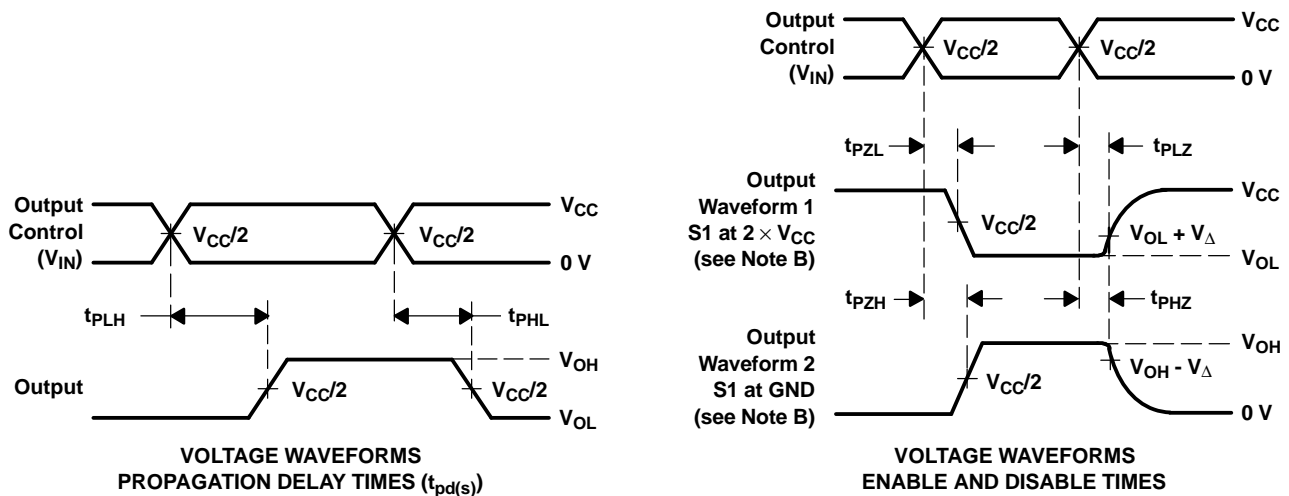


Figure 2. Typical I_{CC} vs \overline{OE} Switching Frequency

PARAMETER MEASUREMENT INFORMATION



TEST	V _{CC}	S1	R _L	V _I	C _L	V _Δ
t _{pd(s)}	2.5 V ± 0.2 V	Open	500 Ω	V _{CC} or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	V _{CC} or GND	50 pF	
t _{PLZ} /t _{PZL}	2.5 V ± 0.2 V	2 × V _{CC}	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V _{CC}	500 Ω	GND	50 pF	0.3 V
t _{PHZ} /t _{PZH}	2.5 V ± 0.2 V	GND	500 Ω	V _{CC}	30 pF	0.15 V
	3.3 V ± 0.3 V	GND	500 Ω	V _{CC}	50 pF	0.3 V



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd(s)}. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74CB3Q16811DGGRE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CB3Q16811DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CB3Q16811DGVRE4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CB3Q16811DGVRG4	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CB3Q16811DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q16811DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q16811DGVR	ACTIVE	TVSOP	DGV	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q16811DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q16811DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CB3Q16811DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

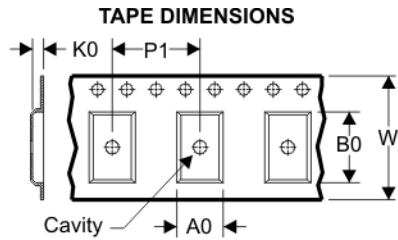
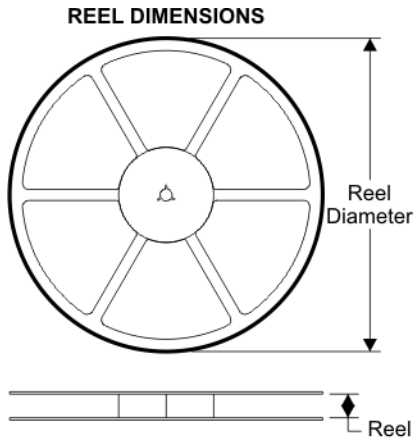
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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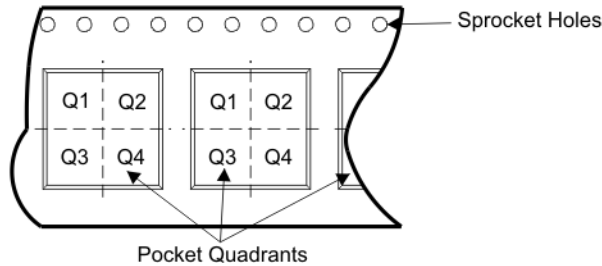
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TAPE AND REEL BOX INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3Q16811DGGR	DGG	56	SITE 41	330	24	8.6	15.6	1.8	12	24	Q1
SN74CB3Q16811DGVR	DGV	56	SITE 41	330	24	6.8	10.1	1.6	12	24	Q1
SN74CB3Q16811DLR	DL	56	SITE 41	330	32	11.35	18.67	3.1	16	32	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74CB3Q16811DGGR	DGG	56	SITE 41	346.0	346.0	41.0
SN74CB3Q16811DGVR	DGV	56	SITE 41	346.0	346.0	41.0
SN74CB3Q16811DLR	DL	56	SITE 41	346.0	346.0	49.0

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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