

# SN74CB3Q16811

## 24-BIT SWITCH WITH PRECHARGED OUTPUTS

### 2.5-V/3.3-V LOW-VOLTAGE FET BUS SWITCH

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- Member of the Texas Instruments Widebus™ Family
- SN74CB3Q Bus Switches Are Equivalent to IDTQS3VH Bus Switches
- 5-V Tolerant I/Os With Device Powered Up or Powered Down
- Low and Flat ON-State Resistance ( $r_{ON}$ ) Characteristics Over Operating Range ( $r_{ON} = 5 \Omega$  Typ)
- Rail-to-Rail Switching on Data I/O Ports
  - 0- to 5-V Switching With 3.3-V  $V_{CC}$
  - 0- to 3.3-V Switching With 2.5-V  $V_{CC}$
- B-Port Outputs Are Precharged by Bias Voltage (BIASV) to Minimize Signal Distortion During Live Insertion and Hot Plugging
- Supports PCI Hot Plug
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{iO(OFF)} = 4 \text{ pF Typ}$ )
- Fast Switching Frequency ( $f_{ON} = 20 \text{ MHz Max}$ )
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 0.75 \text{ mA Typ}$ )
- $V_{CC}$  Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: PCI Hot Plug, Hot Docking, Memory Interleaving, Bus Isolation, and Low-Distortion Signal Gating

† For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C*, *CB3T*, and *CB3Q Signal-Switch Families*, literature number SCDA008.

## description/ordering information

The SN74CB3Q16811 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance ( $r_{ON}$ ). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q16811 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74CB3Q16811DL	CB3Q16811
		Tape and reel	SN74CB3Q16811DLR	
	TSSOP – DGG	Tape and reel	SN74CB3Q16811DGGR	CB3Q16811
	TVSOP – DGV	Tape and reel	SN74CB3Q16811DGVR	BW811

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**description/ordering information (continued)**

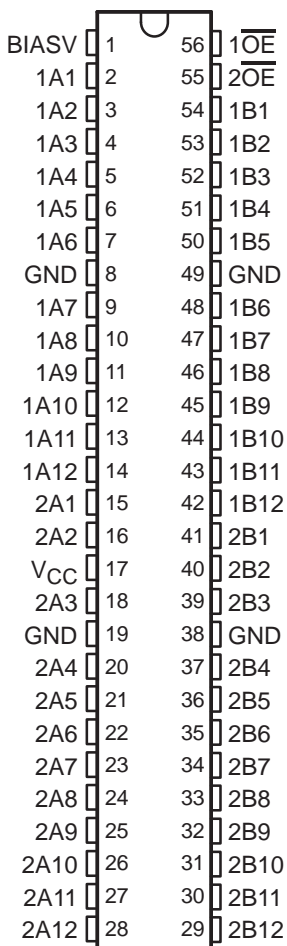
The SN74CB3Q16811 is organized as two 12-bit bus switches with separate output-enable ( $\overline{1OE}$ ,  $\overline{2OE}$ ) inputs. It can be used as two 12-bit bus switches or as one 24-bit bus switch. When  $\overline{OE}$  is low, the associated 12-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 12-bit bus switch is OFF, and a high-impedance state exists between the A and B ports. The B port is precharged to bias voltage (BIASV) through the equivalent of a 10-k $\Omega$  resistor when  $\overline{OE}$  is high or if the device is powered down ( $V_{CC} = 0$  V).

During insertion (or removal) of a card into (or from) an active bus, the card's output voltage may be close to GND. When the connector pins make contact, the card's parasitic capacitance tries to force the bus signal to GND, creating a possible glitch on the active bus. This glitching effect can be reduced by using a bus switch with precharged bias voltage (BIASV) of the bus switch equal to the input threshold voltage level of the receivers on the active bus. This method ensures that any glitch produced by insertion (or removal) of the card does not cross the input threshold region of the receivers on the active bus, minimizing the effects of live-insertion noise.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry prevents damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**DGG, DGV, OR DL PACKAGE**  
**(TOP VIEW)**



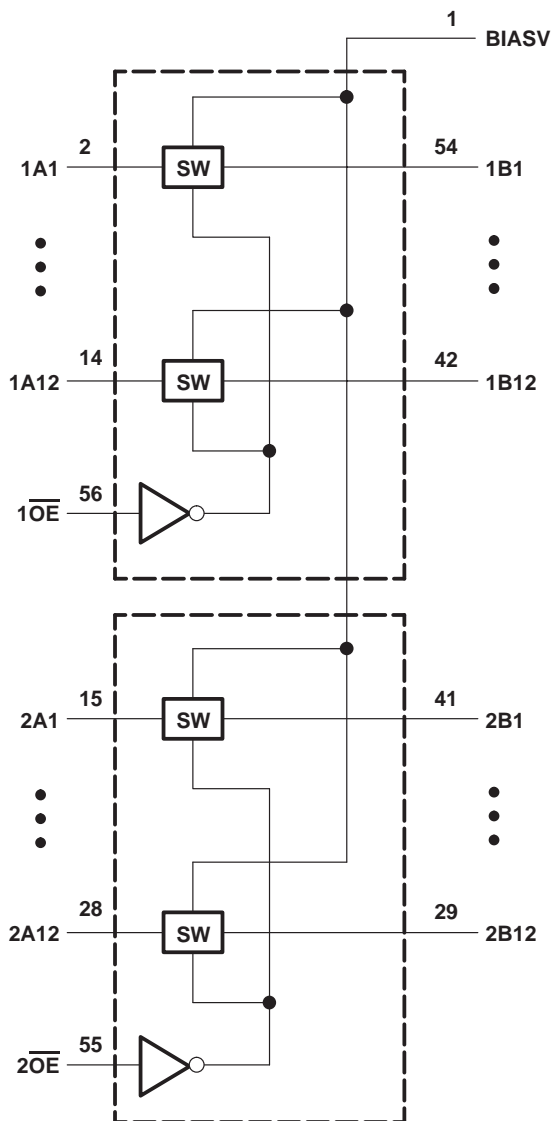
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**FUNCTION TABLE**  
(each 12-bit bus switch)

INPUT $\overline{\text{OE}}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect B port = BIASV

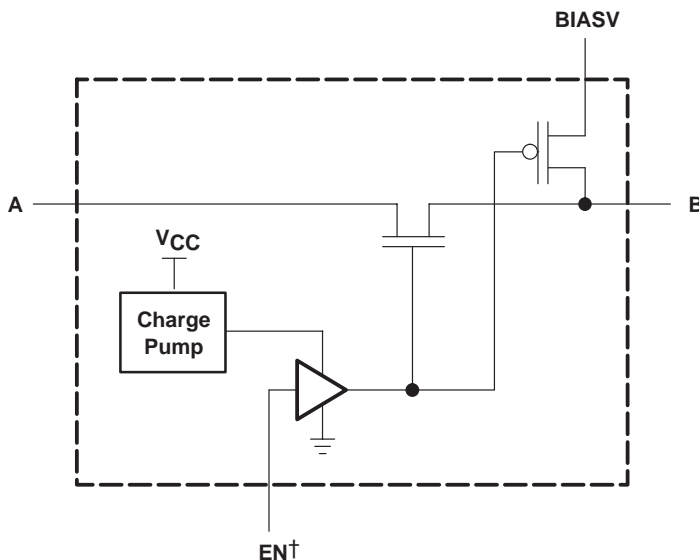
logic diagram (positive logic)



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simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range, $V_{CC}$	-0.5 V to 4.6 V
BIAS supply voltage range, BIASV	-0.5 V to 7 V
Control input voltage range, $V_{IN}$ (see Notes 1 and 2)	-0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	-0.5 V to 7 V
Control input clamp current, $I_{IK}$ ( $V_{IN} < 0$ )	-50 mA
I/O port clamp current, $I_{I/O}$ ( $V_{I/O} < 0$ )	-50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	$\pm 64$ mA
Continuous current through $V_{CC}$ or GND terminals	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 5):	
DGG package	64°C/W
DGV package	48°C/W
DL package	56°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground, unless otherwise specified.
  2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  3.  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
  4.  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
  5. The package thermal impedance is calculated in accordance with JESD 51-7.

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**recommended operating conditions (see Note 6)**

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	2.3	3.6	V	
BIASV	Bias voltage	0	5	V	
V <sub>IH</sub>	High-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	5.5	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2	5.5	
V <sub>IL</sub>	Low-level control input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	0	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	0.8	
V <sub>I/O</sub>	Data input/output voltage	0	5.5	V	
T <sub>A</sub>	Operating free-air temperature	-40	85	°C	

NOTE 6: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 3.6 V,	I <sub>I</sub> = -18 mA			-1.8	V
I <sub>IN</sub>	Control inputs	V <sub>CC</sub> = 3.6 V,	V <sub>IN</sub> = 0 to 5.5 V			±1	μA
I <sub>O</sub>	B port	V <sub>CC</sub> = 3.0 V,	BIASV = 2.4 V, V <sub>O</sub> = 0, Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND			0.2	mA
I <sub>OZ</sub> ‡		V <sub>CC</sub> = 3.6 V,	V <sub>O</sub> = 0 to 5.5 V, V <sub>I</sub> = 0, Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND			±1	μA
I <sub>off</sub>		V <sub>CC</sub> = 0,	V <sub>O</sub> = 0 to 5.5 V, V <sub>I</sub> = 0			1	μA
I <sub>CC</sub>		V <sub>CC</sub> = 3.6 V,	I <sub>I/O</sub> = 0, Switch ON or OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND			1 3	mA
ΔI <sub>CC</sub> §	Control inputs	V <sub>CC</sub> = 3.6 V,	One input at 3 V, Other inputs at V <sub>CC</sub> or GND			30	μA
I <sub>CCD</sub> ¶	Per control input	V <sub>CC</sub> = 3.6 V,	A and B ports open, Control input switching at 50% duty cycle			0.38 0.45	mA/ MHz
C <sub>in</sub>	Control inputs	V <sub>CC</sub> = 3.3 V,	V <sub>IN</sub> = 5.5 V, 3.3 V, or 0			3.5 5	pF
C <sub>io(OFF)</sub>	A port	V <sub>CC</sub> = 3.3 V,	Switch OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>I/O</sub> = 5.5 V, 3.3 V, or 0			4 5	pF
C <sub>io(ON)</sub>		V <sub>CC</sub> = 3.3 V,	Switch ON, V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>I/O</sub> = 5.5 V, 3.3 V, or 0			10 12.5	pF
r <sub>on</sub> #		V <sub>CC</sub> = 2.3 V, TYP at V <sub>CC</sub> = 2.5 V	V <sub>I</sub> = 0, I <sub>O</sub> = 30 mA			5 8	Ω
			V <sub>I</sub> = 1.7 V, I <sub>O</sub> = -15 mA			5 9	
		V <sub>CC</sub> = 3 V	V <sub>I</sub> = 0, I <sub>O</sub> = 30 mA			5 6.5	
			V <sub>I</sub> = 2.4 V, I <sub>O</sub> = -15 mA			5 8	

V<sub>IN</sub> and I<sub>IN</sub> refer to control inputs. V<sub>I</sub>, V<sub>O</sub>, I<sub>I</sub>, and I<sub>O</sub> refer to data pins.

† All typical values are at V<sub>CC</sub> = 3.3 V (unless otherwise noted), T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.

¶ This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).

# Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)**

PARAMETER	FROM (INPUT)	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	
f <sub>OE</sub>		$\overline{OE}$	A or B		10		20	MHz
t <sub>pd</sub> *		A or B	B or A		0.09		0.15	ns
t <sub>PZH</sub>	BIASV = GND	$\overline{OE}$	A or B	1.5	8	1.5	8	ns
t <sub>PZL</sub>	BIASV = 3 V			1.5	8	1.5	8	
t <sub>PHZ</sub>	BIASV = GND	$\overline{OE}$	A or B	1	7.5	1	7.5	ns
t <sub>PLZ</sub>	BIASV = 3 V			1	7.5	1	7.5	

|| Maximum switching frequency for control input (V<sub>O</sub> > V<sub>CC</sub>, V<sub>I</sub> = 5 V, R<sub>L</sub> ≥ 1 MΩ, C<sub>L</sub> = 0)

\* The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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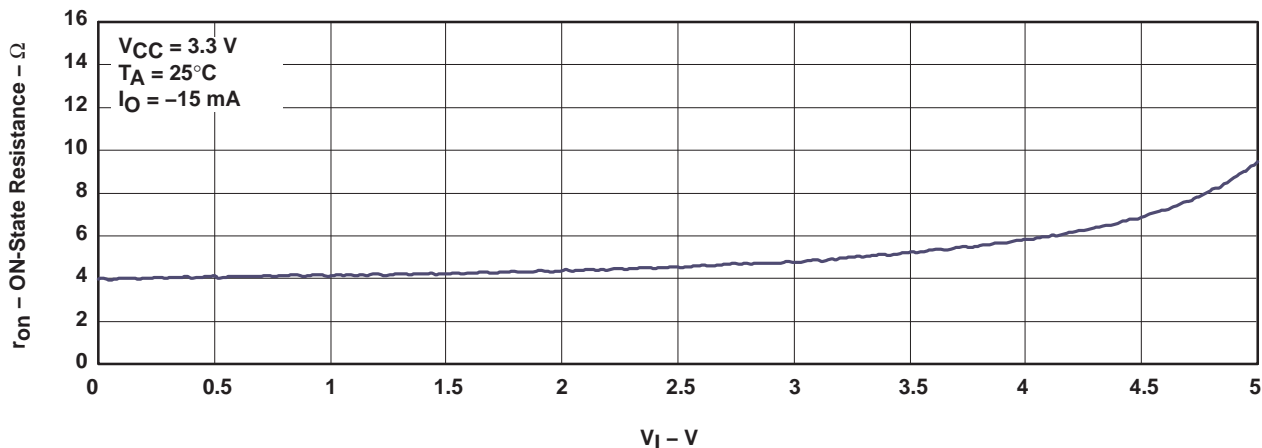


Figure 1. Typical  $r_{on}$  vs  $V_I$ ,  $V_{CC} = 3.3$  V,  $I_O = -15$  mA

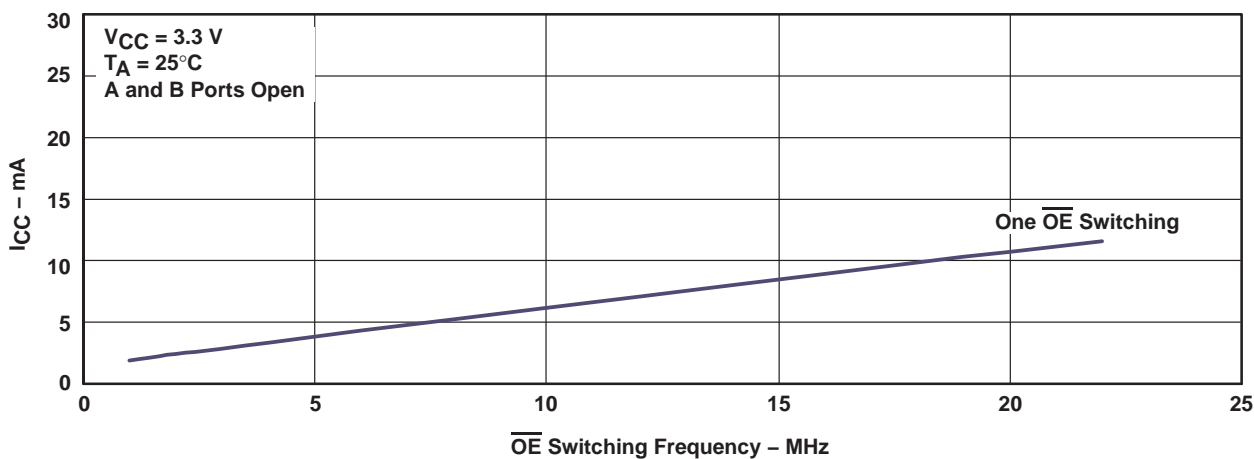
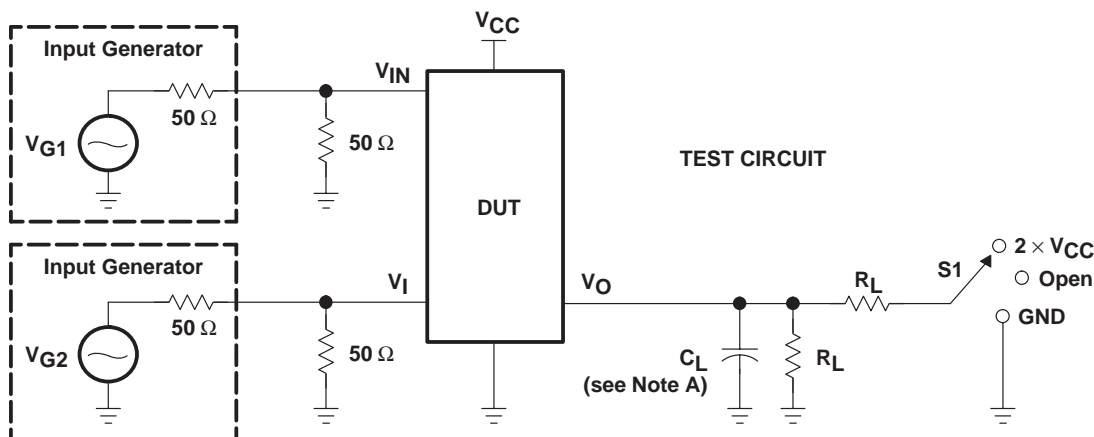


Figure 2. Typical  $I_{CC}$  vs  $\overline{OE}$  Switching Frequency,  $V_{CC} = 3.3$  V

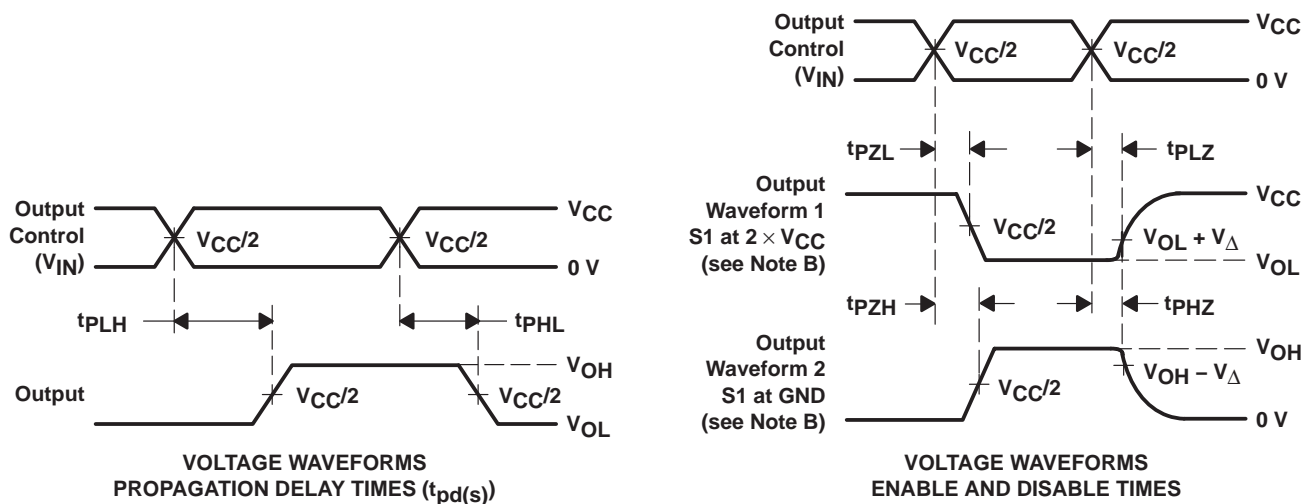
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**PARAMETER MEASUREMENT INFORMATION**



TEST	VCC	S1	RL	VI	CL	VΔ
t <sub>pd</sub> (s)	2.5 V ± 0.2 V	Open	500 Ω	VCC or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	VCC or GND	50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	2.5 V ± 0.2 V	2 × VCC	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × VCC	500 Ω	GND	50 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	2.5 V ± 0.2 V	GND	500 Ω	VCC	30 pF	0.15 V
	3.3 V ± 0.3 V	GND	500 Ω	VCC	50 pF	0.3 V



- NOTES:
- A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>(s). The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Test Circuit and Voltage Waveforms**



DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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