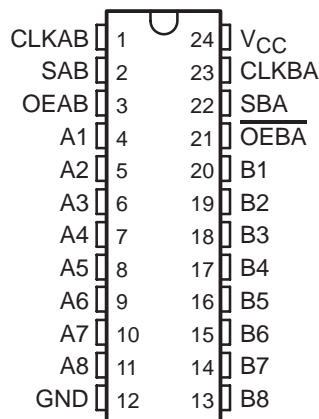


SN74BCT651 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

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- State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- Power-Up High-Impedance Mode
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (NT)

DW OR NT PACKAGE
(TOP VIEW)



description

This SN74BCT651 consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and \overline{OEBA}) inputs are provided to control the transceiver functions. The select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74BCT651.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and \overline{OEBA} . In this configuration, each output reinforces its input. Thus, when all the other data sources to the two sets of bus lines are at high impedance, each set will remain at its last state.

The SN74BCT651 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
OEAB	\overline{OEBA}	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified [†]	Store A, hold B
H	H	↑	↑	X [‡]	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified [†]	Input	Hold A, store B
L	L	↑	↑	X	X [‡]	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time \overline{B} data to A bus
L	L	X	H or L	X	H	Output	Input	Stored \overline{B} data to A bus
H	H	X	X	L	X	Input	Output	Real-time \overline{A} data to B bus
H	H	H or L	X	H	X	Input	Output	Stored \overline{A} data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored \overline{A} data to B bus and stored B data to A bus

[†] The data output functions may be enabled or disabled by various signals at the OEAB or \overline{OEBA} inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

[‡] When select control is low, clocks can occur simultaneously so long as allowances are made for propagation delays from A to B (B to A) plus setup and hold times. When select control is high, clocks must be staggered in order to load both registers.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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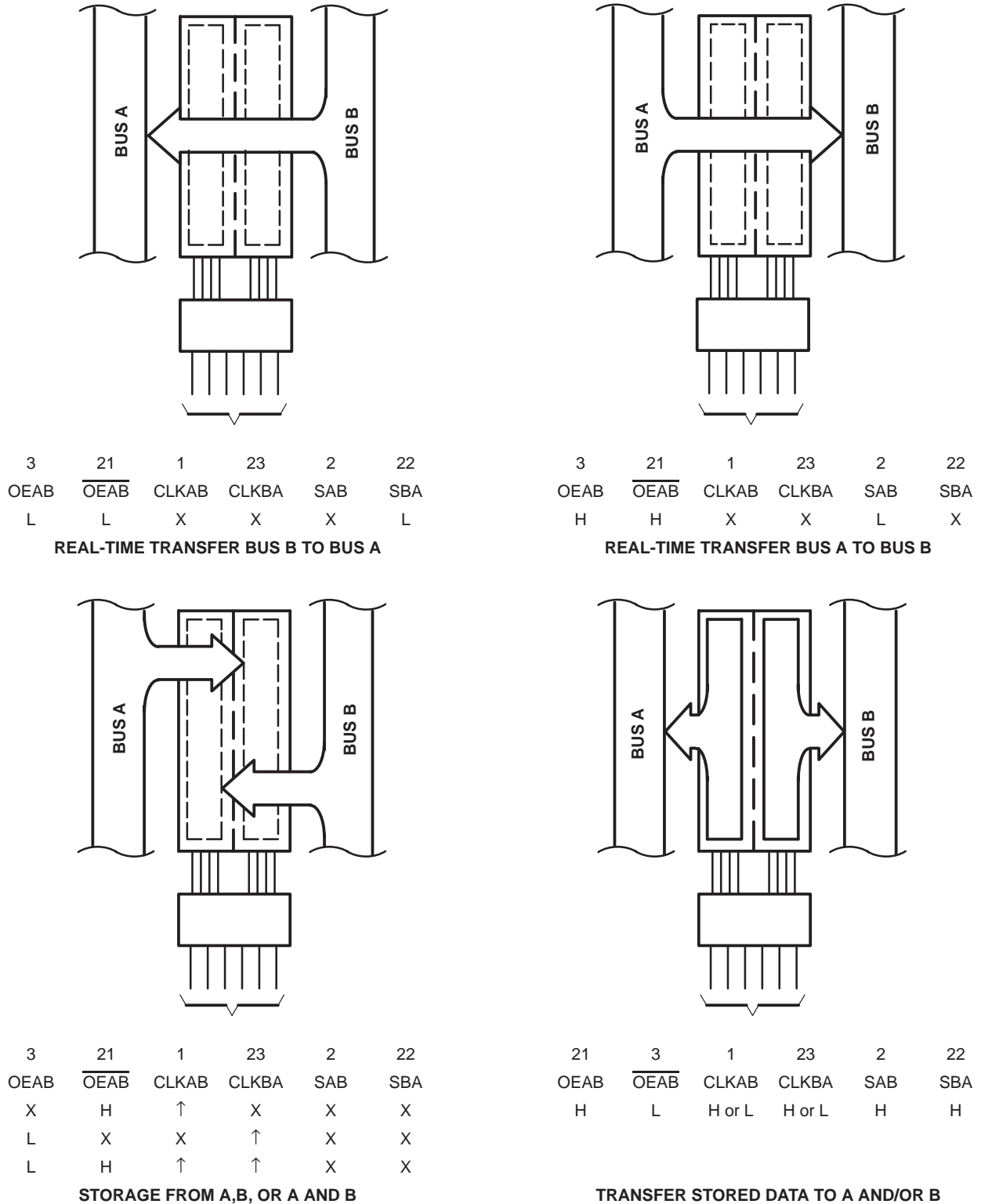
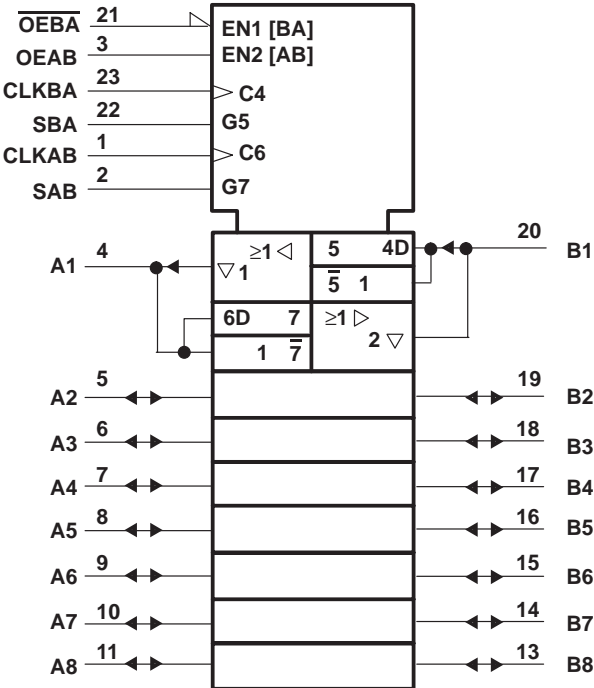


Figure 1. Bus-Management Functions

SN74BCT651
OCTAL BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS

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logic symbol†



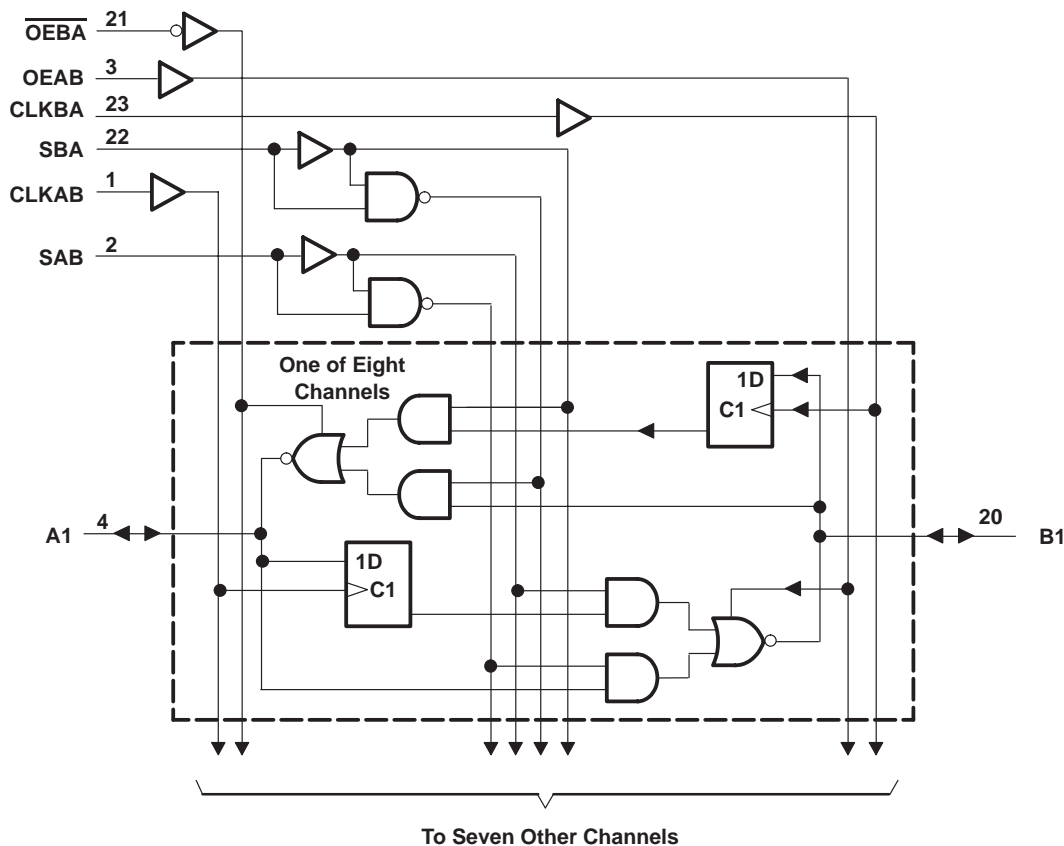
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



SN74BCT651 OCTAL BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

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logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	- 0.5 V to 7 V
Input voltage range: Control inputs (see Note 1)	- 0.5 V to 7 V
I/O ports (see Note 1)	- 0.5 V to 5.5 V
Voltage range applied to any output in the disabled or power-off state, V_O	- 0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O	- 0.5 V to V_{CC}
Current into any output in the low state	128 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	- 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
V_{OH}		$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.3		V
			$I_{OH} = -15\text{ mA}$	2	3.1		
		$V_{CC} = 4.75\text{ V}$,	$I_{OH} = -3\text{ mA}$	2.7			
V_{OL}		$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 64\text{ mA}$		0.42	0.55	V
I_I	A or B port	$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V}$			1	mA
	Control inputs					1	
$I_{IH}‡$	A or B port	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			70	µA
	Control inputs					20	
$I_{IL}‡$	A or B port	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.5\text{ V}$			-0.7	mA
	Control inputs					-0.7	
$I_{OS}§$		$V_{CC} = 5.5\text{ V}$,	$V_O = 0$	-100		-225	mA
I_{CCL}	A or B port	$V_{CC} = 5.5\text{ V}$,	$V_I = \text{GND}$		39	62	mA
I_{CCH}	A or B port	$V_{CC} = 5.5\text{ V}$,	$V_I = 4.5\text{ V}$		8	13	mA
I_{CCZ}	A or B port	$V_{CC} = 5.5\text{ V}$,	$V_I = \text{GND}$		10	16	mA
C_i	Control inputs	$V_{CC} = 5\text{ V}$,	$V_I = 2.5\text{ V or }0.5\text{ V}$		5.5		pF
C_{iO}	A or B port	$V_{CC} = 5\text{ V}$,	$V_O = 2.5\text{ V or }0.5\text{ V}$		11		pF

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
		MIN	MAX			
f_{clock}	Clock frequency	0	85	0	85	MHz
t_w	Pulse duration	CLK high	4.8	4.8		ns
		CLK low	7	7		
t_{su}	Setup time, A or B before CLK↑	6		6		ns
t_h	Hold time, A or B after CLK↑	1		1		ns



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			85			85		MHz
t_{PLH}	CLKBA or CLKAB	A or B	3.2	7	10	3.2	11.7	ns
t_{PHL}			3.9	7.3	10.2	3.9	11.8	
t_{PLH}	A or B	B or A	3.2	7.3	10.4	3.2	12.6	ns
t_{PHL}			2.7	5.9	8.5	2.7	9.8	
t_{PLH}	SAB or SBA \dagger (with A or B high)	A or B	2.8	6	8.6	2.8	9.8	ns
t_{PHL}			4.8	9.4	12.8	4.8	15.5	
t_{PLH}	SBA or SAB \dagger (with A or B low)	A or B	3.9	8.6	12.1	3.9	14.6	ns
t_{PHL}			4.4	8.1	11.1	4.4	12.8	
t_{PZH}	\overline{OEBA} or OEAB	A or B	3.3	7.1	9.8	3.3	12	ns
t_{PZL}			3.8	7.8	10.8	3.8	13.1	
t_{PHZ}	\overline{OEBA} or OEAB	A or B	3.6	6.6	9	3.6	10.2	ns
t_{PLZ}			2.8	5.8	8.4	2.8	9.6	
t_{PZH}	DIR	A or B	2.2	5.1	7.3	2.2	8.3	ns
t_{PZL}			2.8	5.9	8.5	2.8	9.7	
t_{PHZ}	DIR	A or B	4.2	8	12.8	4.2	15	ns
t_{PLZ}			3.8	7.4	10.2	3.8	12.3	

\dagger These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74BCT651DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN74BCT651DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN74BCT651NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

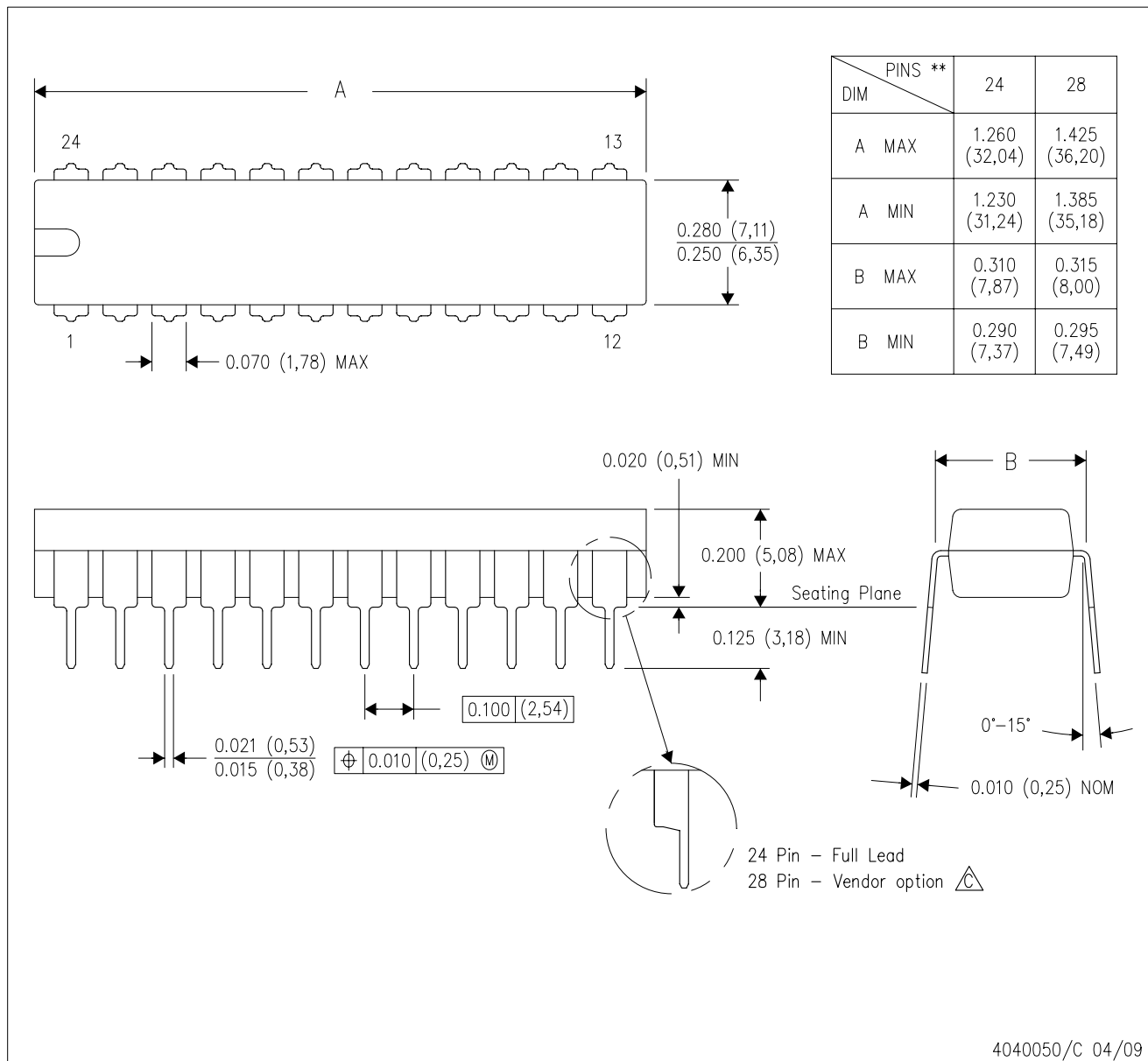
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MECHANICAL DATA

NT (R-PDIP-T**) 24 PINS SHOWN

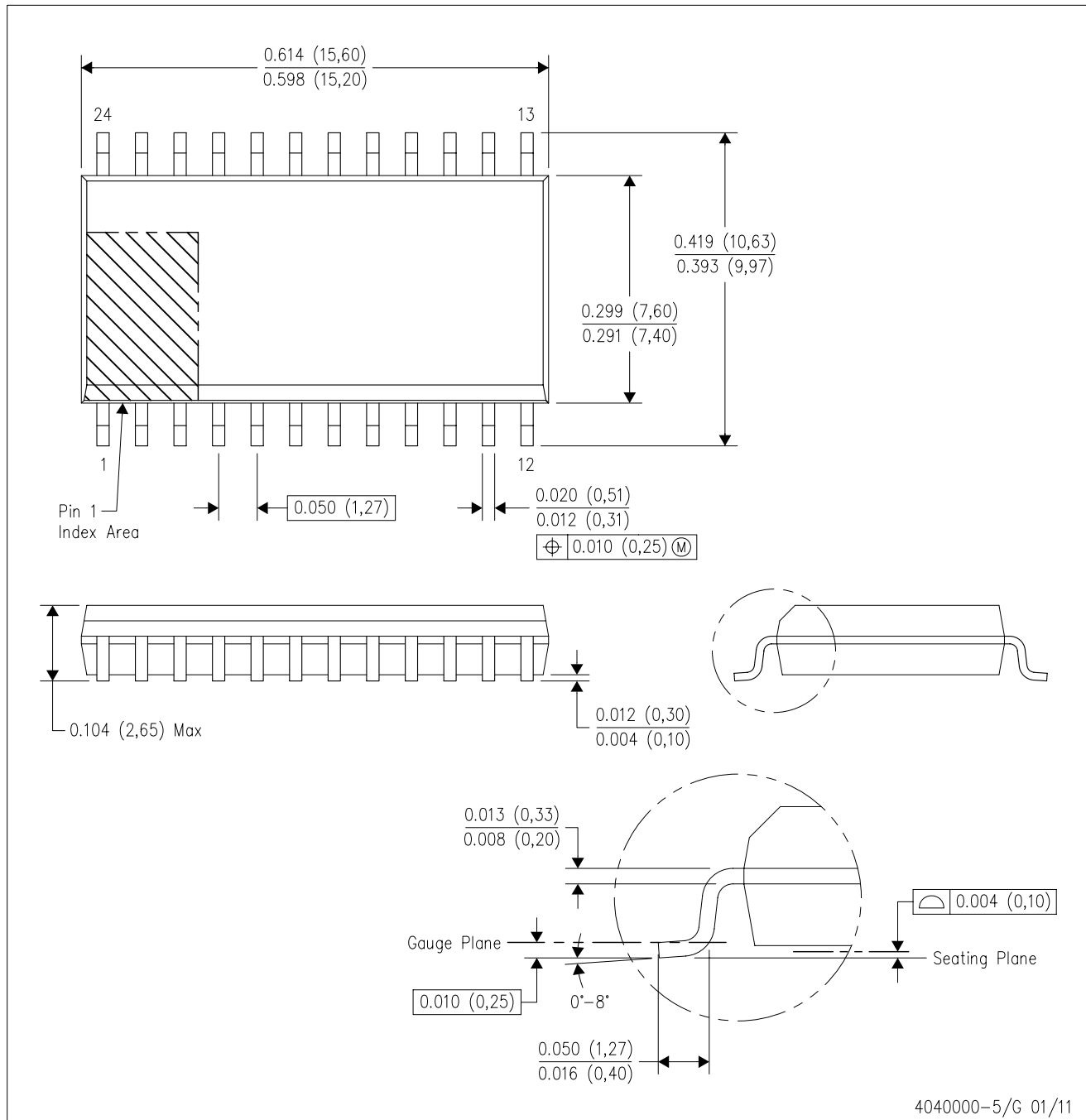
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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