

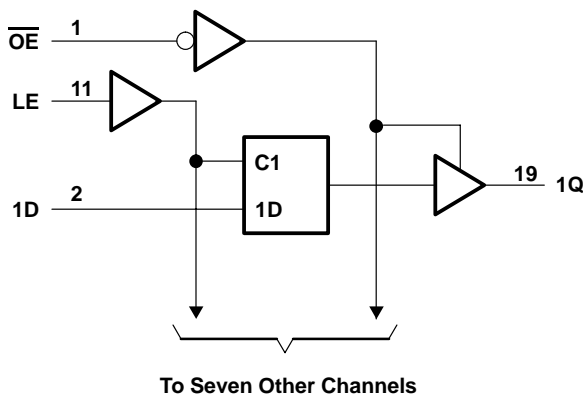
SN54BCT573, SN74BCT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS071B – AUGUST 1990 – REVISED MARCH 2003

FUNCTION TABLE
(each latch)

| INPUTS | | | OUTPUT |
|-----------------|----|---|--------|
| \overline{OE} | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|--------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Voltage range applied to any output in the disabled or power-off state, V_O | –0.5 V to 5.5 V |
| Voltage range applied to any output in the high state, V_O | –0.5 V to V_{CC} |
| Input clamp current, I_{IK} ($V_I < 0$) | –30 mA |
| Current into any output in the low state: SN54BCT573 | 96 mA |
| SN74BCT573 | 128 mA |
| Package thermal impedance, θ_{JA} (see Note 2): DW package | 58°C/W |
| N package | 69°C/W |
| NS package | 60°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

| | | SN54BCT573 | | | SN74BCT573 | | | UNIT |
|----------|--------------------------------|------------|-----|-----|------------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I_{IK} | Input clamp current | | | -18 | | | -18 | mA |
| I_{OH} | High-level output current | | | -12 | | | -15 | mA |
| I_{OL} | Low-level output current | | | 48 | | | 64 | mA |
| T_A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54BCT573 | | SN74BCT573 | | UNIT | |
|-----------|---------------------------|--|------------|------|------------|------|------|------|
| | | | MIN | TYP† | MAX | MIN | | TYP† |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, | $I_I = -18\text{ mA}$ | | | -1.2 | | -1.2 | V |
| V_{OH} | $V_{CC} = 4.5\text{ V}$ | $I_{OH} = -3\text{ mA}$ | 2.4 | 3.3 | 2.4 | 3.3 | | V |
| | | $I_{OH} = -12\text{ mA}$ | 2 | 3.2 | | | | |
| | | $I_{OH} = -15\text{ mA}$ | | | 2 | 3.1 | | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 48\text{ mA}$ | | 0.38 | 0.55 | | | V |
| | | $I_{OL} = 64\text{ mA}$ | | | | 0.42 | 0.55 | |
| I_I | $V_{CC} = 5.5\text{ V}$, | $V_I = 5.5\text{ V}$ | | | 0.4 | | 0.4 | mA |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, | $V_I = 2.7\text{ V}$ | | | 20 | | 20 | μA |
| I_{IL} | $V_{CC} = 5.5\text{ V}$, | $V_I = 0.5\text{ V}$ | | | -0.6 | | -0.6 | mA |
| $I_{OS}‡$ | $V_{CC} = 5.5\text{ V}$, | $V_O = 0$ | -100 | | -225 | -100 | -225 | mA |
| I_{OZH} | $V_{CC} = 5.5\text{ V}$, | $V_O = 2.7\text{ V}$ | | | 50 | | 50 | μA |
| I_{OZL} | $V_{CC} = 5.5\text{ V}$, | $V_O = 0.5\text{ V}$ | | | -50 | | -50 | μA |
| I_{CCL} | $V_{CC} = 5.5\text{ V}$, | Outputs open | | | 62 | | 62 | mA |
| I_{CCH} | $V_{CC} = 5.5\text{ V}$, | Outputs open | | | 8 | | 8 | mA |
| I_{CCZ} | $V_{CC} = 5.5\text{ V}$, | Outputs open | | | 8 | | 8 | mA |
| C_i | $V_{CC} = 5\text{ V}$, | $V_I = 2.5\text{ V}$ or 0.5 V | | 5.5 | | 5.5 | | pF |
| C_o | $V_{CC} = 5\text{ V}$, | $V_O = 2.5\text{ V}$ or 0.5 V | | 7.5 | | 7.5 | | pF |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ | | SN54BCT573 | | SN74BCT573 | | UNIT |
|----------|-----------------------------|---|-----|------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration, LE high | 4 | | 4 | | 4 | | ns |
| t_{su} | Setup time, data before LE↓ | 1 | | 2.5 | | 1 | | ns |
| t_h | Hold time, data after LE↓ | 4 | | 4 | | 4 | | ns |



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WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

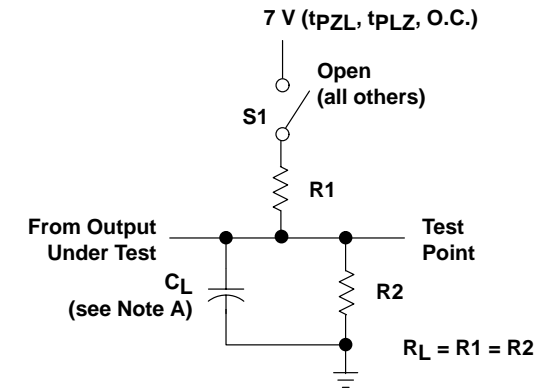
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5$ V, $T_A = 25^\circ$ C | | | SN54BCT573 | | SN74BCT573 | | UNIT |
|-----------|-----------------|-------------|---------------------------------------|-----|-----|------------|------|------------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | D | Q | 2 | 5 | 7.2 | 1 | 9.8 | 2 | 8.4 | ns |
| t_{PHL} | | | 2.8 | 5.9 | 8.2 | 1.5 | 10.3 | 2.8 | 9.6 | |
| t_{PLH} | LE | Q | 2.4 | 6.1 | 7.2 | 2 | 9.7 | 2.4 | 8.1 | ns |
| t_{PHL} | | | 2.9 | 5.2 | 7.1 | 2 | 8.8 | 2.9 | 7.8 | |
| t_{PZH} | \overline{OE} | Q | 3 | 6.2 | 8.5 | 2.5 | 11 | 3 | 10.4 | ns |
| t_{PZL} | | | 4.3 | 7.1 | 9.3 | 3.5 | 11.5 | 4.3 | 11 | |
| t_{PHZ} | \overline{OE} | Q | 2.2 | 3.9 | 5.6 | 1.5 | 7.2 | 2.2 | 6 | ns |
| t_{PLZ} | | | 1.7 | 3.6 | 5.2 | 1 | 7 | 1.7 | 6 | |



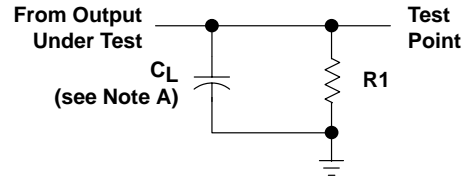
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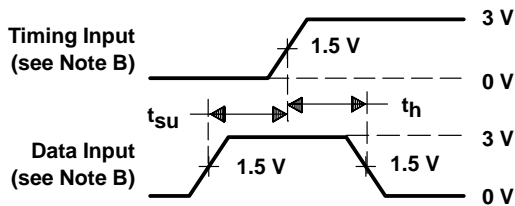
PARAMETER MEASUREMENT INFORMATION



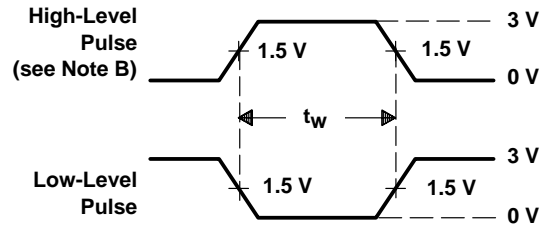
LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS



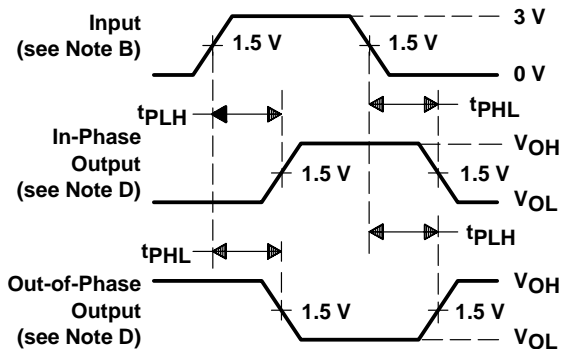
LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



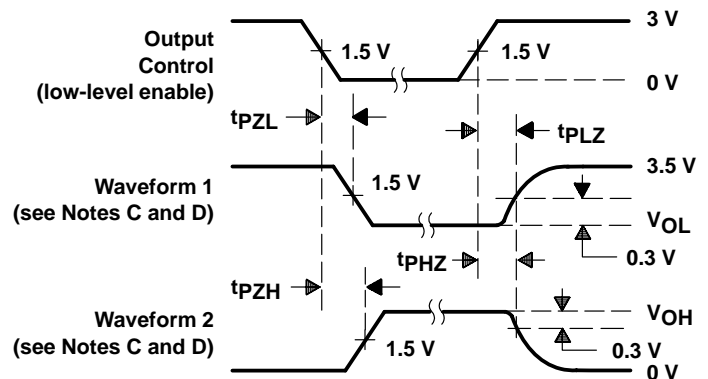
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES:
- C_L includes probe and jig capacitance.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - The outputs are measured one at a time with one transition per measurement.
 - When measuring propagation delay times of 3-state outputs, switch S1 is open.
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

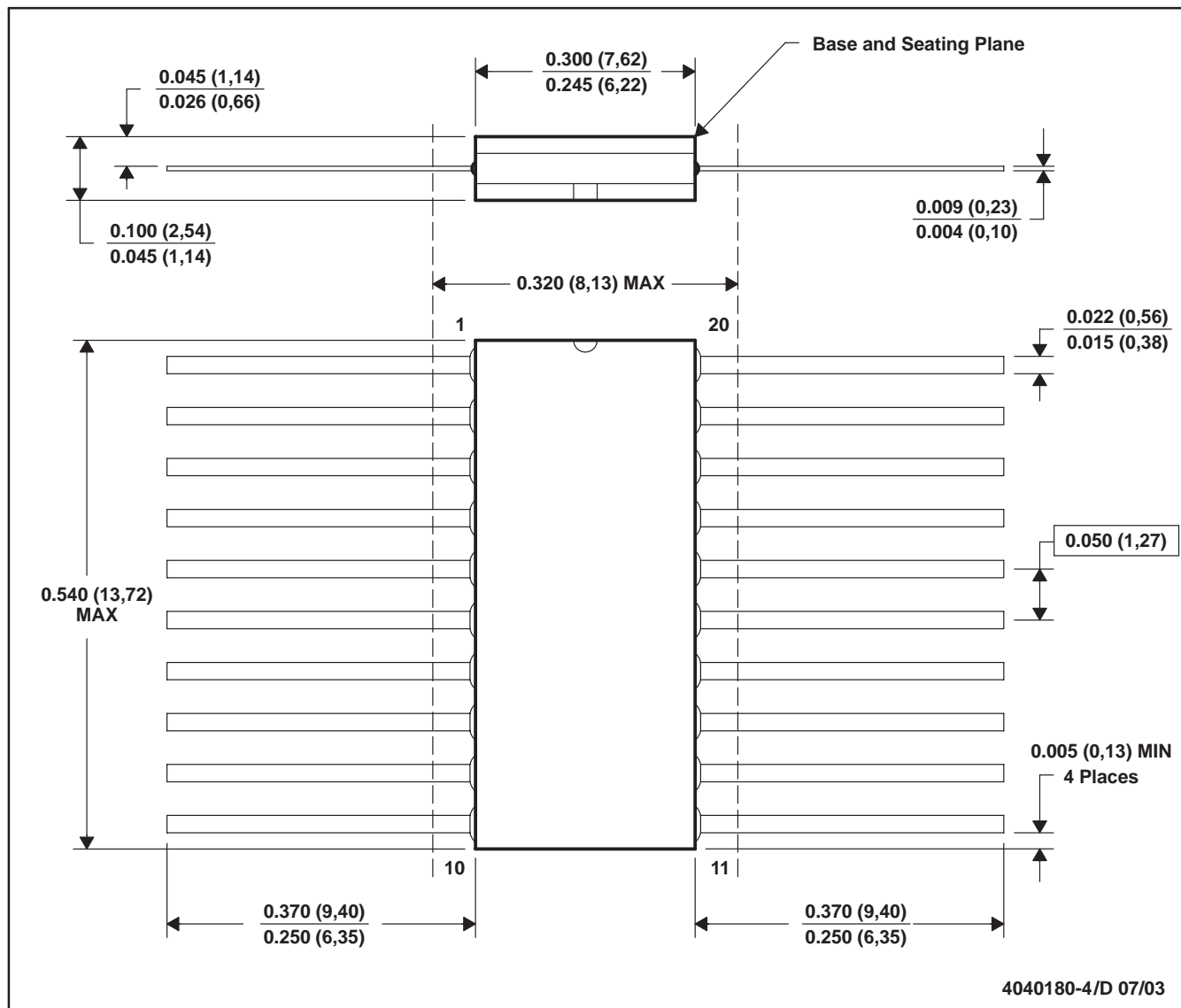


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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