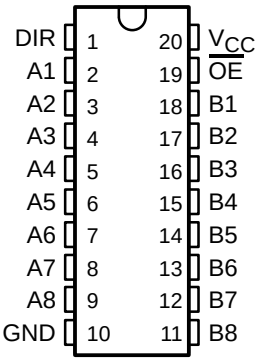
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds JESD 22**
  – 2000-V Human-Body Model (A114-A)

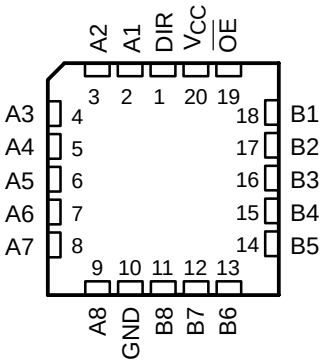
description

These octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

SN54BCT245 . . . J OR W PACKAGE
SN74BCT245 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54BCT245 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

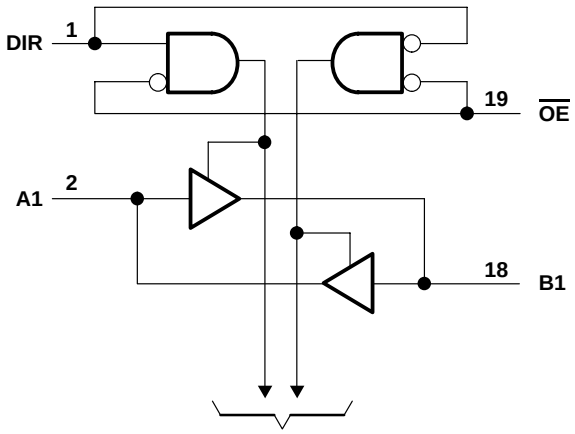
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74BCT245N	SN74BCT245N
	SOIC – DW	Tube	SN74BCT245DW	BCT245
		Tape and reel	SN74BVT245DWR	
	SOP – NS	Tape and reel	SN74BCT245NSR	BCT245
	SSOP – DB	Tape and reel	SN74BCT245DBR	BT245
	TSSOP – PW	Tape and reel	SN74BCT245PWR	BT245
–55°C to 125°C	CDIP – J	Tube	SNJ54BCT245J	SNJ54BCT245J
	CFP – W	Tube	SNJ54BCT245W	SNJ54BCT245W
	LCCC – FK	Tube	SNJ54BCT245FK	SNJ54BCT245FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I: Control inputs (see Note 1) . . . . . –0.5 V to 7 V
I/O ports (see Note 1) . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state, V_O . . . . . –0.5 V to V_{CC}
Current into any output in the low state, I_O: SN54BCT245 . . . . . 96 mA
SN74BCT245 . . . . . 128 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 70°C/W
DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
PW package . . . . . 83°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54BCT245			SN74BCT245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				–18			–18	mA
I_{OH}	High-level output current	A port			–3			–3	mA
		B port			–12			–15	
I_{OL}	Low-level output current	A port			20			24	mA
		B port			48			64	
T_A	Operating free-air temperature		–55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT245			SN74BCT245			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	A port	V_{CC} = 4.5 V	I_{OH} = –1 mA	2.5	3.4		2.5	3.4		V
			I_{OH} = –3 mA	2.4	3.3		2.4	3.3		
	B port	V_{CC} = 4.5 V	I_{OH} = –3 mA	2.4	3.3		2.4	3.3		
			I_{OH} = –12 mA	2	3.2					
			I_{OH} = –15 mA				2	3.1		
V_{OL}	A port	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5				V
			I_{OL} = 24 mA					0.35	0.5	
	B port	V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I	A or B port	V_{CC} = 5.5 V,	V_I = 5.5 V			1			1	mA
	Control input					0.1			0.1	
I_{IH}‡	A or B port	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	µA
	Control input					20			20	
I_{IL}‡	A or B port	V_{CC} = 5.5 V,	V_I = 0.5 V			–0.65			–0.65	mA
	Control input					–1.2			–1.2	
I_{OS}§	A port	V_{CC} = 5.5 V,	V_O = 0	–60		–150	–60		–150	mA
	B port			–100		–225	–100		–225	
I_{CCL}	A to B	V_{CC} = 5.5 V			57	90		57	90	mA
I_{CCH}	A to B	V_{CC} = 5.5 V			36	57		36	57	mA
I_{CCZ}		V_{CC} = 5.5 V			10	15		10	15	mA
C_i	Control input	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		7			7		pF
C_{io}	A to B	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		9			9		pF
	B to A				12			12		

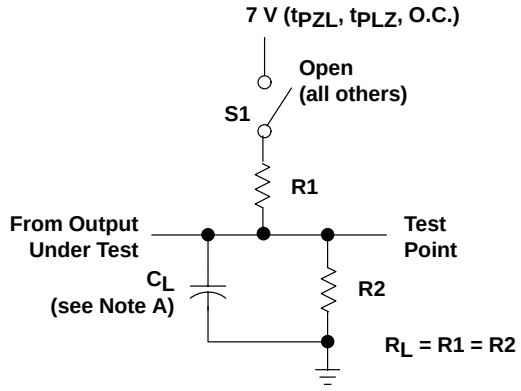
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics (see Figure 1)

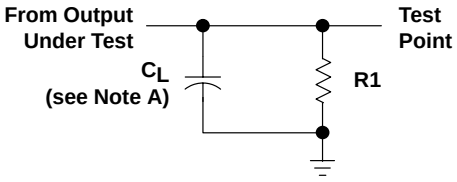
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			′BCT245			SN54BCT245		SN74BCT245		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	4.4	6	1	7.2	1	7	ns
t_{PHL}			1.5	4.8	6.6	1.5	7.6	1.5	7	
t_{PZH}	$\overline{OE}$	A or B	1.5	8	9.4	1.5	11.2	1.5	10.9	ns
t_{PZL}			1.5	8	10.2	1.5	11.8	1.5	11.6	
t_{PHZ}	$\overline{OE}$	A or B	1.5	5.8	8.3	1.5	9.7	1.5	9.3	ns
t_{PLZ}			1.5	5.1	7.8	1.5	9.6	1.5	9.1	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

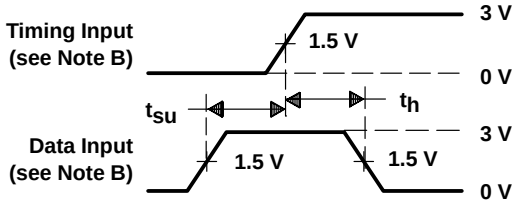
PARAMETER MEASUREMENT INFORMATION



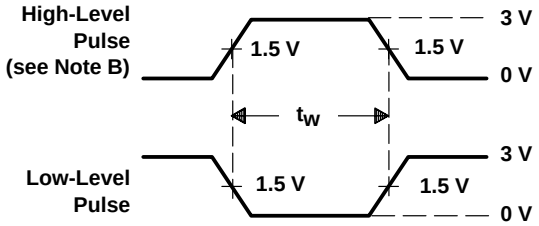
LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS



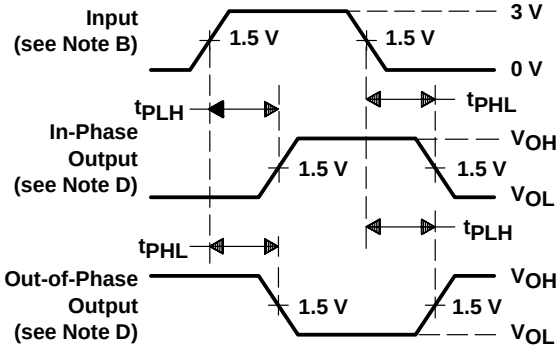
LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



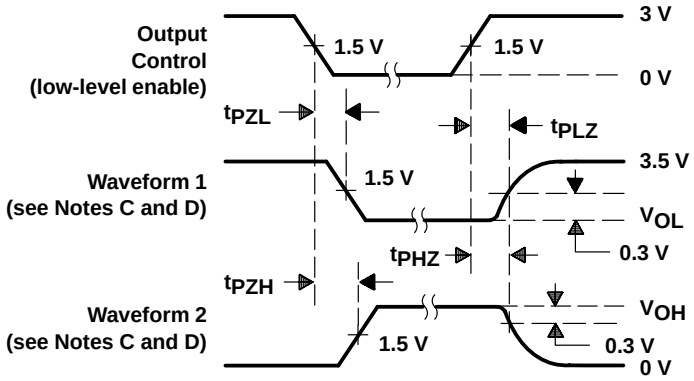
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. When measuring propagation delay times of 3-state outputs, switch S1 is open.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

Figures 2 through 5 show the typical power dissipation for an SN74BCT245 over variations in outputs switching, output frequency, and capacitive load.

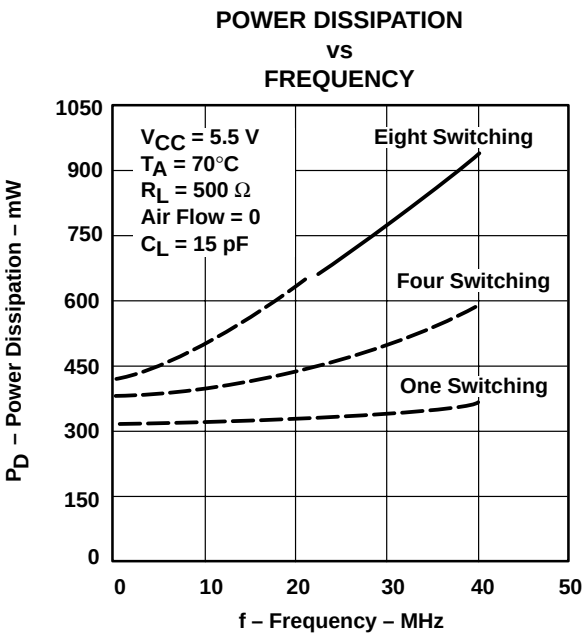


Figure 2

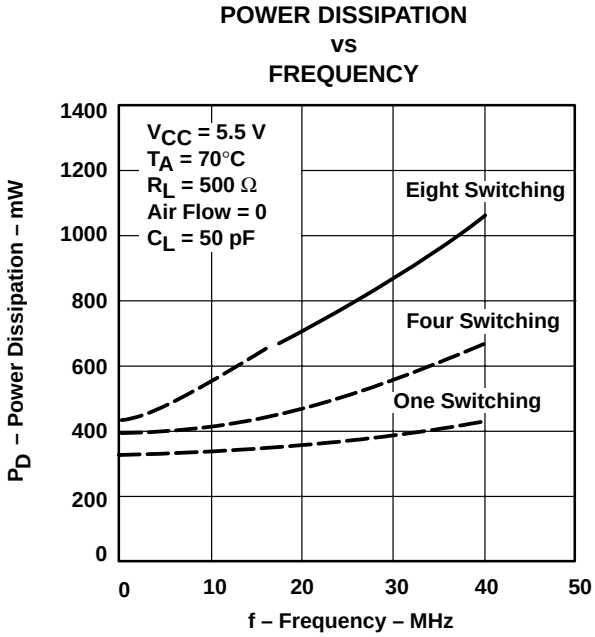


Figure 3

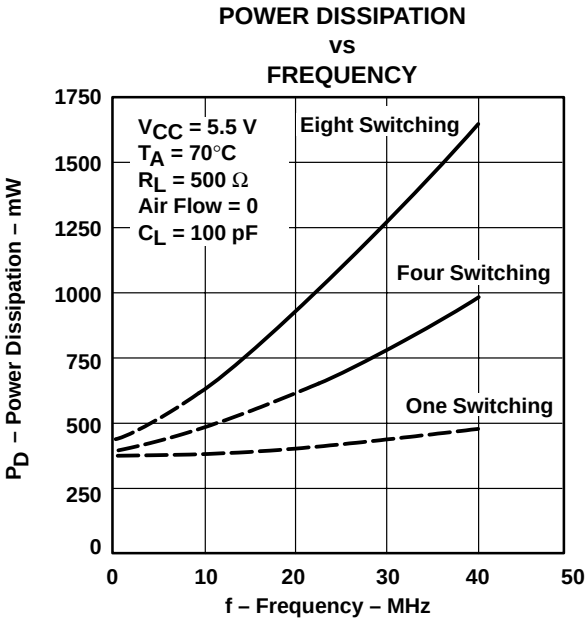


Figure 4

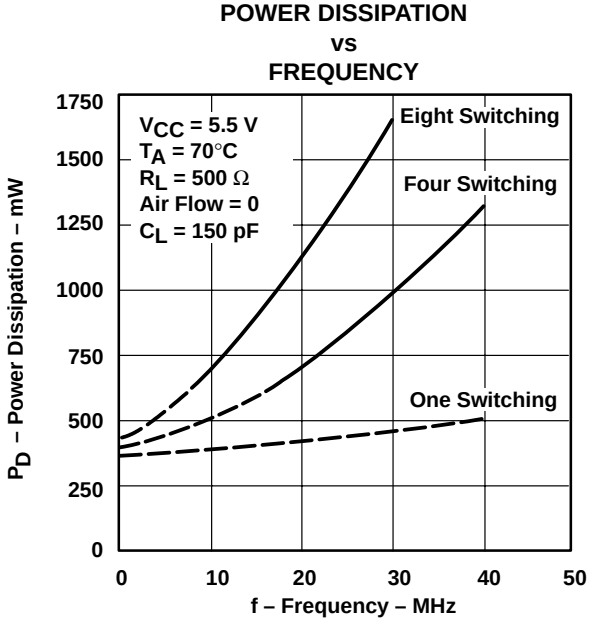


Figure 5

† The dashed lines are for the DB package only.

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