

# SN74BCT2420

## NuBus™ ADDRESS/DATA TRANSCEIVERS AND REGISTERS

SDIS007A – D3159, NOVEMBER 1988 – REVISED JANUARY 1989

- **Designed for NuBus™ Interface Applications**
- **Conforms to ANSI/IEEE Std 1196-1987**
- **On-Chip Comparator Provides I/D Slot Identification**
- **Multiplexed Real-Time and Latched Address/Data**
- **Designed to Operate With SN74ACT2440 NuBus™ Controller**
- **BiCMOS Design Substantially Reduces Standby Current**
- **Dependable Texas instruments Quality and Reliability**

### description

The 'BCT2420 consists of bus transceiver circuits, D-type flip-flops, latches, and control circuitry arranged for multiplexed transmission of address and data information in NuBus™ applications. An on-chip comparator has been included to detect when a NuBus™ transfer cycle is requesting the local board. The device conforms to ANSI/IEEE Std 1196-1987 and operates with Texas instruments SN74ACT2440 NuBus™ Controller. In addition, the device is easily configured around ASIC or other PAL® -based controllers.

The 'BCT2420 was designed using Texas Instruments BiCMOS process, which features bipolar drive characteristics and greatly reduces the standby power of the device when disabled. This feature is especially valuable when the device is not performing a NuBus™ transaction.

The  $\overline{\text{AEN}}$ ,  $\overline{\text{DEN}}$  and  $\overline{\text{ADEN}}$  inputs control the transceiver functions. Three 16-bit I/O ports, A15–A0, D15–D0, and  $\overline{\text{AD15}}-\overline{\text{AD0}}$ , provide for address and data transfer. When the NuBus™ performs a write cycle to the local board, address information is saved on the rising edge of  $\overline{\text{ACLK}}$ . During the last portion of the NuBus™ write cycle, data information is saved on the rising edge of  $\overline{\text{DCLK}}$ .

When the local board is performing a write to the NuBus™, address and data is multiplexed onto the NuBus™ via the  $\overline{\text{A/D}}$  line. Address and data can be latched by using the  $\overline{\text{ALE}}$  and  $\overline{\text{DLE}}$  input lines respectively.

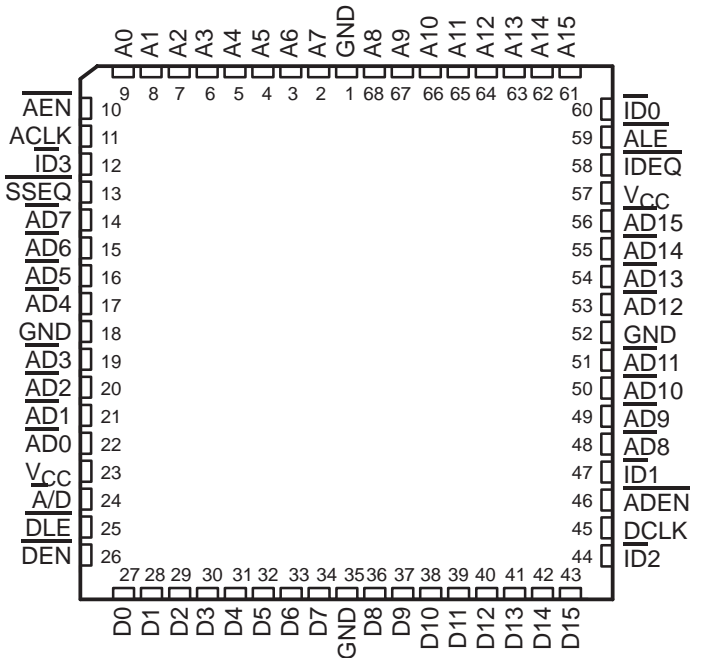
The  $\overline{\text{IDEQ}}$  output is used to signal that the local board is being requested by the NuBus™. This output is typically fed to the NuBus™ controller.  $\overline{\text{IDEQ}}$  goes active (low) when  $\overline{\text{AD15}}-\overline{\text{AD12}}$  are low and  $\overline{\text{AD11}}-\overline{\text{AD8}}$  match  $\overline{\text{ID3}}-\overline{\text{ID0}}$ .  $\overline{\text{IDEQ}}$  stays valid until the next address clock ( $\overline{\text{ACLK}}$ ) occurs. Internal 10-kΩ pullup resistors are included on the  $\overline{\text{ID3}}-\overline{\text{ID0}}$  inputs.

The  $\overline{\text{SSEQ}}$  output is used to signal the local board that super-slot addresses are being requested. This output is active (low) whenever  $\overline{\text{AD15}}-\overline{\text{AD12}}$  are equal to  $\overline{\text{ID3}}-\overline{\text{AD0}}$ , except when  $\overline{\text{ID3}}-\overline{\text{ID0}}$  are all low.

In typical NuBus™ applications, two devices are required to provide the full 32-bit address/data path. Refer to the typical NuBus™ interface diagram on page 9 for additional information.

The SN74BCT2420 is characterized for operation from 0°C to 70°C.

**FN PACKAGE  
(TOP VIEW)**



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Function Tables

INPUTS						OUTPUTS
A15–A0	D15–D0	ALE	DLE	A/D	ADEN	AD15–AD0
H	X	L	X	L	L	L
L	X	L	X	L	L	H
X	X	H	X	L	L	Q <sub>O</sub>
X	H	X	L	H	L	L
X	L	X	L	H	L	H
X	X	X	H	H	L	Q <sub>O</sub>
X	X	X	X	X	H	Z

INPUTS			OUTPUTS
AD15–AD0	ACLK, DCLK	AEN, DEN	A15–A0, D15–D0
H	↑	L	L
L	↑	L	H
X	L	L	Q <sub>O</sub>
X	X	H	L

AD15–AD12	ID3–ID0	SSEQ
EQ $\overline{\text{ID3-ID0}}$	NE 0	L
NE $\overline{\text{ID3-ID0}}$	X	H
X	EQ 0	H

AD15–AD12	AD11–AD8	IDEQ
EQ 0	EQ $\overline{\text{ID3-ID0}}$	L
X	NE $\overline{\text{ID3-ID0}}$	H
NE 0	X	H

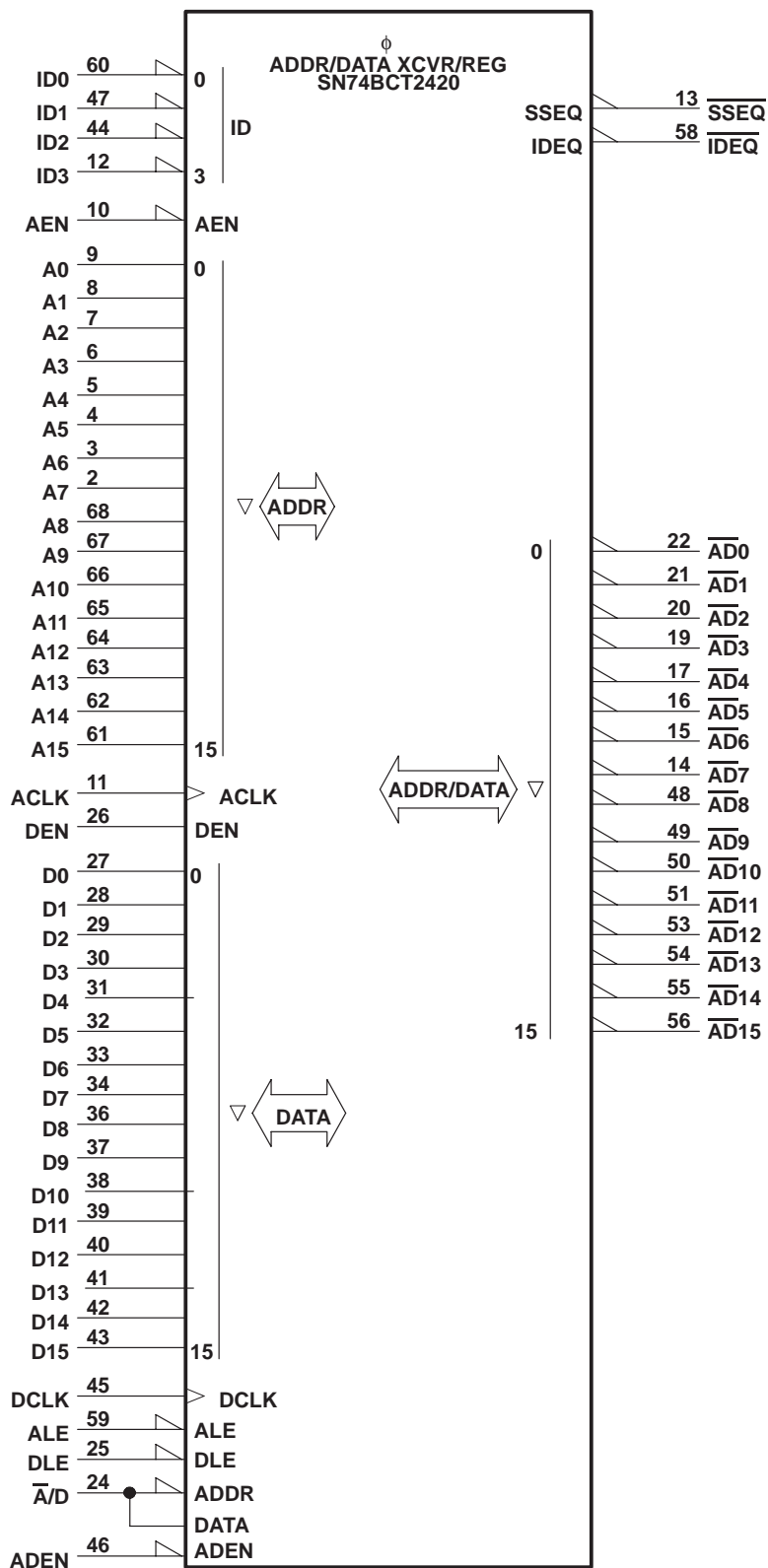
NOTE: Symbol 'Q<sub>O</sub>' denotes previous logic state preserved. Symbol 'Z' denotes high-impedance state.

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## NuBus™ ADDRESS/DATA TRANSCEIVERS AND REGISTERS

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logic symbol†



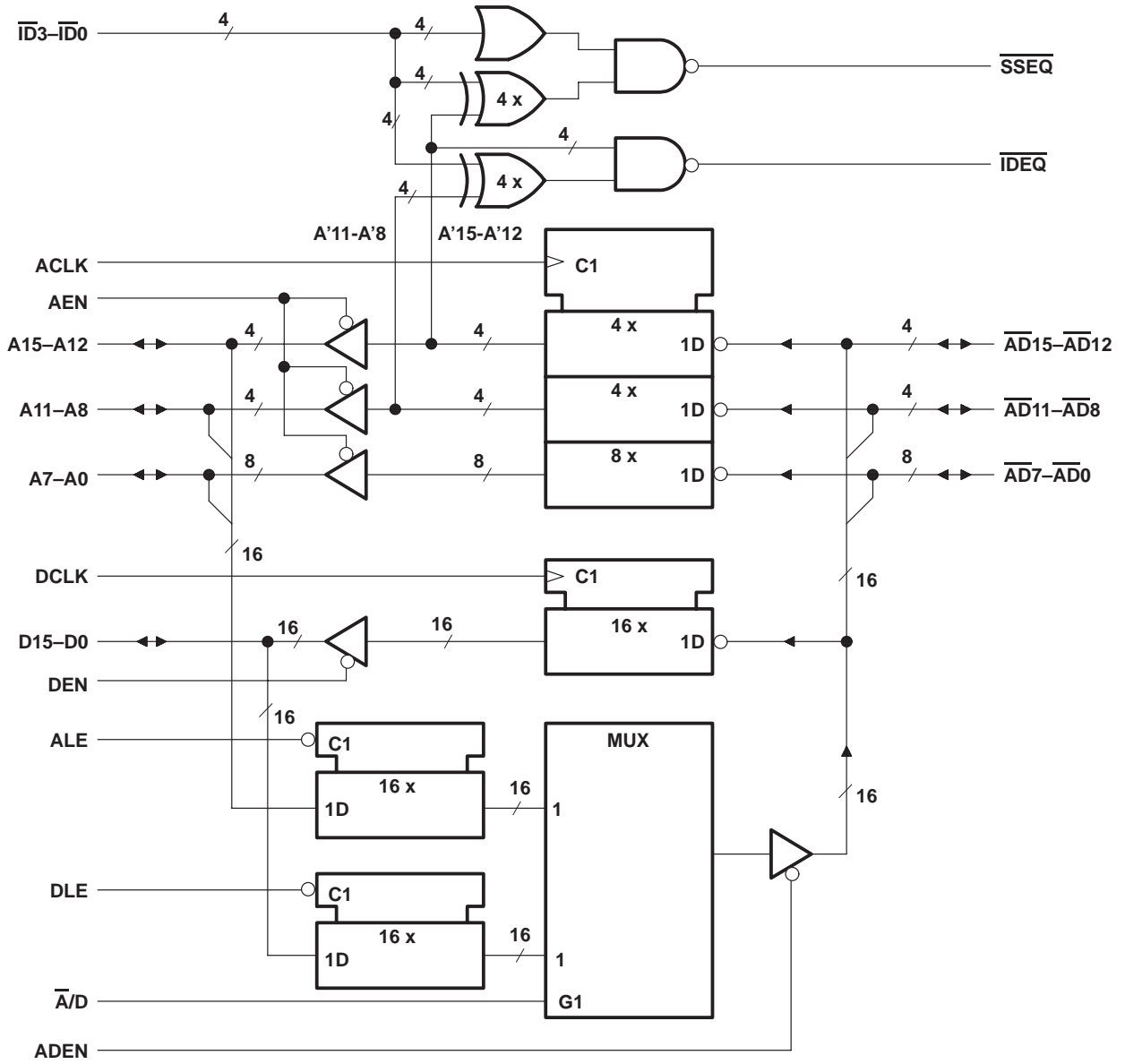
† This symbol is in accordance with ANSI/IEEE Std. 91-1984.



# SN74BCT2420 NuBus™ ADDRESS/DATA TRANSCEIVERS AND REGISTERS

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## logic diagram



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## NuBus™ ADDRESS/DATA TRANSCEIVERS AND REGISTERS

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### Terminal Functions

PIN NAME	DESCRIPTION
A15–A0	Address bus. This 16-bit I/O port is connected to the local board's address bus. When information is transferred between this port and the NuBus™ port ( $\overline{AD15}$ – $\overline{AD0}$ ), the data is inverted to conform to NuBus™ specifications.
ACLK	Address clock. This input saves the address portion of NuBus™ read or write cycles. Data present at the $\overline{AD15}$ – $\overline{AD0}$ inputs is clocked into the address register on the low-to-high transition of ACLK.
$\overline{A/D}$	Address/data select. This input controls the address/data multiplexer. When $\overline{A/D}$ is driven low, the local address port, A15–A0, is selected as input to the $\overline{AD15}$ – $\overline{AD0}$ outputs. When $\overline{A/D}$ is taken high, the local data port, D15–D0, is selected as input to the $\overline{AD15}$ – $\overline{AD0}$ outputs.
$\overline{AD15}$ – $\overline{AD0}$	Address/data port. This 16-bit active-low I/O port directly interfaces to the NuBus™ address/data lines. These lines are multiplexed to carry address information at the beginning of a NuBus™ cycle and data information later in the cycle.
$\overline{ADEN}$	Address/data output enable. This active-low input enables the $\overline{AD15}$ – $\overline{AD0}$ outputs. When $\overline{ADEN}$ is taken high, the $\overline{AD15}$ – $\overline{AD0}$ outputs are in the high impedance state, allowing input from the NuBus™.
$\overline{AEN}$	Address enable. This active-low input enables the local address outputs, A15–A0, to place data onto the local board. When $\overline{AEN}$ is taken high, the A15–A0 outputs are in the high-impedance state, allowing input from the local address bus.
$\overline{ALE}$	Address latch enable. This active-low input controls the latch that holds the address received from the local address bus, A15–A0. When $\overline{ALE}$ is low, the latch is transparent. When $\overline{ALE}$ is taken high, the address present at the A15–A0 inputs is latched and remains latched while $\overline{ALE}$ is held high.
D15–D0	Data bus. This 16-bit I/O port is connected to the local board's data bus. When information is transferred between this port and the NuBus™ port ( $\overline{AD15}$ – $\overline{AD0}$ ), the data is inverted to conform to NuBus™ specifications.
DCLK	Data clock. This input saves the data portion of NuBus™ write cycles. Data present at the $\overline{AD15}$ – $\overline{AD0}$ inputs is clocked into the data register on the low-to-high transition of DCLK.
$\overline{DEN}$	Data enable. This active-low input enables the local data port outputs, D15–D0, to place data onto the local board. When $\overline{DEN}$ is taken high, the D15–D0 outputs are in the high-impedance state, allowing input from the local board.
$\overline{DLE}$	Data latch enable. This active-low input controls the latch that holds the data received from the local data bus, D15–D0. When $\overline{DLE}$ is low, the latch is transparent. When $\overline{DLE}$ is taken high, the data present at the D15–D0 inputs is latched and remains latched while $\overline{DLE}$ is held high.
$\overline{ID3}$ – $\overline{ID0}$	Card-slot identification. These four inputs accept binary-coded location information for each NuBus™ slot position on the backplane. These four lines are typically hard wired logic levels unique to each NuBus™ slot connector. For convenient implementation, the inputs have internal 10-k $\Omega$ pull up resistors that ensure the logic high level when the inputs are left open circuited. The internal comparator uses these inputs to identify when the local hardware card is being accessed.
$\overline{IDEQ}$	Identification equal. This active-low output is used to signal that the board is being accessed by the NuBus™. $\overline{IDEQ}$ goes low whenever $\overline{AD15}$ – $\overline{AD12}$ are low and $\overline{AD11}$ – $\overline{AD8}$ match $\overline{ID3}$ – $\overline{ID0}$ . Since the internal comparator uses data from the address register, the address register must be clocked before the local board samples $\overline{IDEQ}$ . $\overline{IDEQ}$ is valid for the entire NuBus™ cycle after ACLK.
SSEQ	Super-slot equal. This active-low output is used to signal the local board that super-slot addresses are being requested in the super-slot mode. SSEQ goes low when $\overline{AD15}$ – $\overline{AD12}$ match $\overline{ID3}$ – $\overline{ID0}$ and $\overline{ID3}$ – $\overline{ID0}$ are not all low. Since the internal comparator uses data from the address register, the address register must be clocked before the local board samples SSEQ. SSEQ is valid for the entire NuBus™ cycle after ACLK.

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## NuBus™ ADDRESS/DATA TRANSCEIVERS AND REGISTERS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage (all inputs and I/O ports)	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

### recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level input current	Ax, Dx, $\overline{ADx}$ outputs		-15	mA
		$\overline{SSEQ}$ , $\overline{IDEQ}$ outputs		2.6	
$I_{OL}$	Low-level input current	Ax, Dx, $\overline{ADx}$ outputs		24	mA
		$\overline{SSEQ}$ , $\overline{IDEQ}$ outputs		16	
$f_{clock}$	Clock frequency	0		40	MHz
$t_w$	Pulse duration	ACLK, DCLK high		12.5	ns
		ACLK, DCLK low		12.5	
		$\overline{ALE}$ , $\overline{DLE}$ low		12.5	
$t_{su}$	Setup time	$\overline{ADx}$ before ACLK $\uparrow$ , DCLK $\uparrow$		5	ns
		Ax before $\overline{ALE}\uparrow$		5	
		Dx before $\overline{DLE}\uparrow$		5	
$t_h$	Hold time	$\overline{ADx}$ after ACLK $\uparrow$ , DCLK $\uparrow$		2	ns
		Ax after $\overline{ALE}\uparrow$		2	
		Dx after $\overline{DLE}\uparrow$		2	
$T_A$	Operating free-air temperature	0		70°	°C

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## NuBus™ ADDRESS/DATA TRANSCEIVERS AND REGISTERS

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### electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 4.5 \text{ V}$ , $I_I = -18 \text{ mA}$			-1.2	V
$V_{OH}$	Ax, Dx, $\overline{ADx}$	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $I_{OH} = -400 \mu\text{A}$	$V_{CC} - 1.5$			V
		$V_{CC} = 4.5 \text{ V}$ , $I_{OH} = -3 \text{ mA}$	2.8	3.6		
		$V_{CC} = 4.5 \text{ V}$ , $I_{OH} = -15 \text{ mA}$	2			
	$\overline{SSEQ}$ , $\overline{IDEQ}$	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ , $I_{OH} = -400 \mu\text{A}$	$V_{CC} - 2$			
$V_{CC} = 4.5 \text{ V}$ , $I_{OH} = -2.6 \text{ mA}$		2.4	3.2			
$V_{OL}$	Ax, Dx, $\overline{ADx}$	$V_{CC} = 4.5 \text{ V}$ , $I_{OL} = 12 \text{ mA}$	0.25	0.4		V
		$V_{CC} = 4.5 \text{ V}$ , $I_{OL} = 24 \text{ mA}$	0.35	0.5		
	$\overline{SSEQ}$ , $\overline{IDEQ}$	$V_{CC} = 4.5 \text{ V}$ , $I_{OL} = 8 \text{ mA}$	0.25	0.4		
		$V_{CC} = 4.5 \text{ V}$ , $I_{OL} = 16 \text{ mA}$	0.35	0.5		
$I_I$		$V_{CC} = 5.5 \text{ V}$ , $V_I = 5.5 \text{ V}$			100	$\mu\text{A}$
$I_{IH}^\ddagger$	$\overline{AEN}$ , $\overline{DEN}$ , $\overline{ADEN}$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 2.7 \text{ V}$			20	$\mu\text{A}$
	$\overline{ID3-ID0}$				-400	
	All other inputs				-100	
$I_{IL}^\ddagger$	$\overline{ID3-ID0}$	$V_{CC} = 5.5 \text{ V}$ , $V_I = 0.4 \text{ V}$			-750	$\mu\text{A}$
	All other inputs				-200	
$I_{OS}^\S$		$V_{CC} = 5.5 \text{ V}$ , $V_O = 0 \text{ V}$	-60		-225	mA
$I_{CC}$	Enabled	$V_{CC} = 5.5 \text{ V}$ , $V_{IL} = 0.5 \text{ V}$ , $V_{IH} = 3 \text{ V}$ , Outputs open		110	160	mA
	Disabled			30	40	

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

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## NuBus™ ADDRESS/DATA TRANSCEIVERS AND REGISTERS

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**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER	LOAD CONDITIONS			MIN	TYP†	MAX	UNIT
	R1, R2, and R <sub>L</sub>	C <sub>L</sub>	LOAD CIRCUIT				
f <sub>max</sub> Maximum clock frequency				40			MHz
t <sub>pd</sub> Propagation time, ACLK↑ to Ax ( $\overline{AEN} = L$ )	R1 = 500 Ω, R2 = 500 Ω	50 pF	S1 Open‡		9	16	ns
t <sub>pd</sub> Propagation time, DCLK↑ to Dx ( $\overline{DEN} = L$ )	R1 = 500 Ω, R2 = 500 Ω	50 pF	S1 Open‡		9	16	ns
t <sub>pd</sub> Propagation time, Ax to $\overline{ADx}$ ( $\overline{ALE} = L, \overline{A/D} = L$ )	R1 = 270 Ω, R2 = 470 Ω	300 pF	S1 Closed§		10	18	ns
t <sub>pd</sub> Propagation time, Dx to $\overline{ADx}$ ( $\overline{DLE} = L, \overline{A/D} = H$ )	R1 = 270 Ω, R2 = 470 Ω	300 pF	S1 Closed§		11	18	ns
t <sub>pd</sub> Propagation time, $\overline{ALE}$ low to $\overline{ADx}$ (A/D = L)	R1 = 270 Ω, R2 = 470 Ω	300 pF	S1 Closed§		10	18	ns
t <sub>pd</sub> Propagation time, $\overline{DLE}$ low to $\overline{ADx}$ ( $\overline{A/D} = H$ )	R1 = 270 Ω, R2 = 470 Ω	300 pF	S1 Closed§		11	18	ns
t <sub>pd</sub> Propagation time, $\overline{A/D}$ to $\overline{ADx}$	R1 = 270 Ω, R2 = 470 Ω	300 pF	S1 Closed§		10	16	ns
t <sub>pd</sub> Propagation time, ACLK to IDEQ	R <sub>L</sub> = 500 Ω	50 pF	¶		12	20	ns
t <sub>pd</sub> Propagation time, ACLK to SSEQ	R <sub>L</sub> = 500 Ω	50 pF	¶		12	18	ns
t <sub>pd</sub> Propagation time, IDx to IDEQ	R <sub>L</sub> = 500 Ω	50 pF	¶		12	22	ns
t <sub>pd</sub> Propagation time, IDx to SSEQ	R <sub>L</sub> = 500 Ω	50 pF	¶		12	22	ns
t <sub>en</sub> Enable time, $\overline{AEN}$ to Ax	R1 = 500 Ω, R2 = 500 Ω	50 pF	‡		10	16	ns
t <sub>en</sub> Enable time, $\overline{DEN}$ to Dx	R1 = 500 Ω, R2 = 500 Ω	50 pF	‡		10	16	ns
t <sub>en</sub> Enable time, $\overline{ADEN}$ to $\overline{ADx}$	R1 = 270 Ω, R2 = 470 Ω	300 pF	§		10	18	ns
t <sub>dis</sub> Disable time, $\overline{AEN}$ to Ax	R1 = 500 Ω, R2 = 500 Ω	50 pF	‡		6	10	ns
t <sub>dis</sub> Disable time, $\overline{DEN}$ to Dx	R1 = 500 Ω, R2 = 500 Ω	50 pF	‡		6	10	ns
t <sub>dis</sub> Disable time, $\overline{ADEN}$ to $\overline{ADx}$	R1 = 270 Ω, R2 = 470 Ω	50 pF	§		6	10	ns

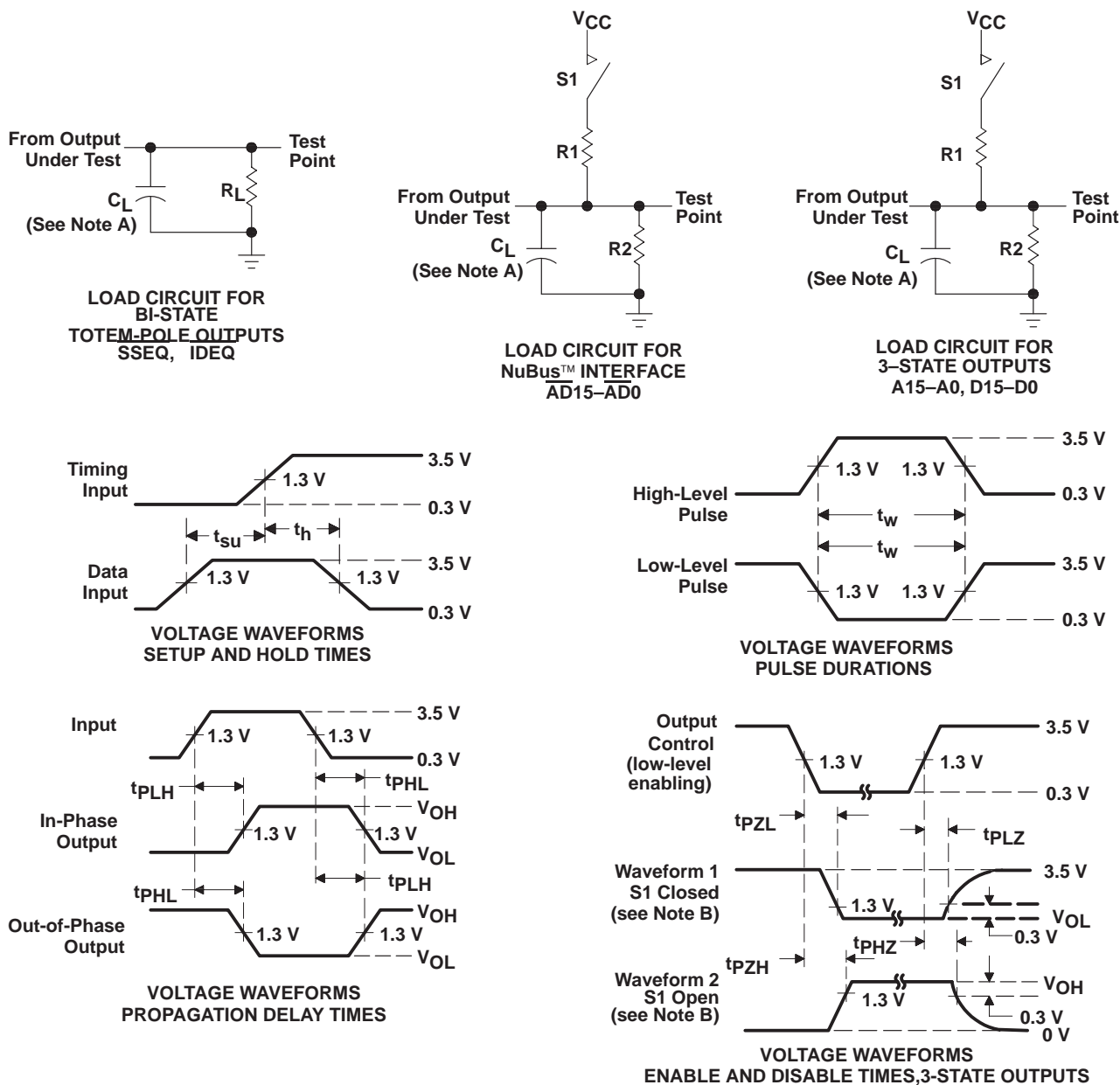
† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ See Parameter Measurement Information for load circuit (3-state outputs, A15–A0, D15–D0) and voltage waveforms.

§ See Parameter Measurement Information for load circuit (NuBus™ Interface,  $\overline{AD15}$ – $\overline{AD0}$ ) and voltage waveforms.

¶ See Parameter Measurement Information for load circuit (bi-state totem-pole outputs, SSEQ, IDEQ) and voltage waveforms.

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal condition such that the output is high except when disabled by the output control.  
 C. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1

# SN74BCT2420 NuBus™ ADDRESS/DATA TRANSCEIVERS AND REGISTERS

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## APPLICATION INFORMATION

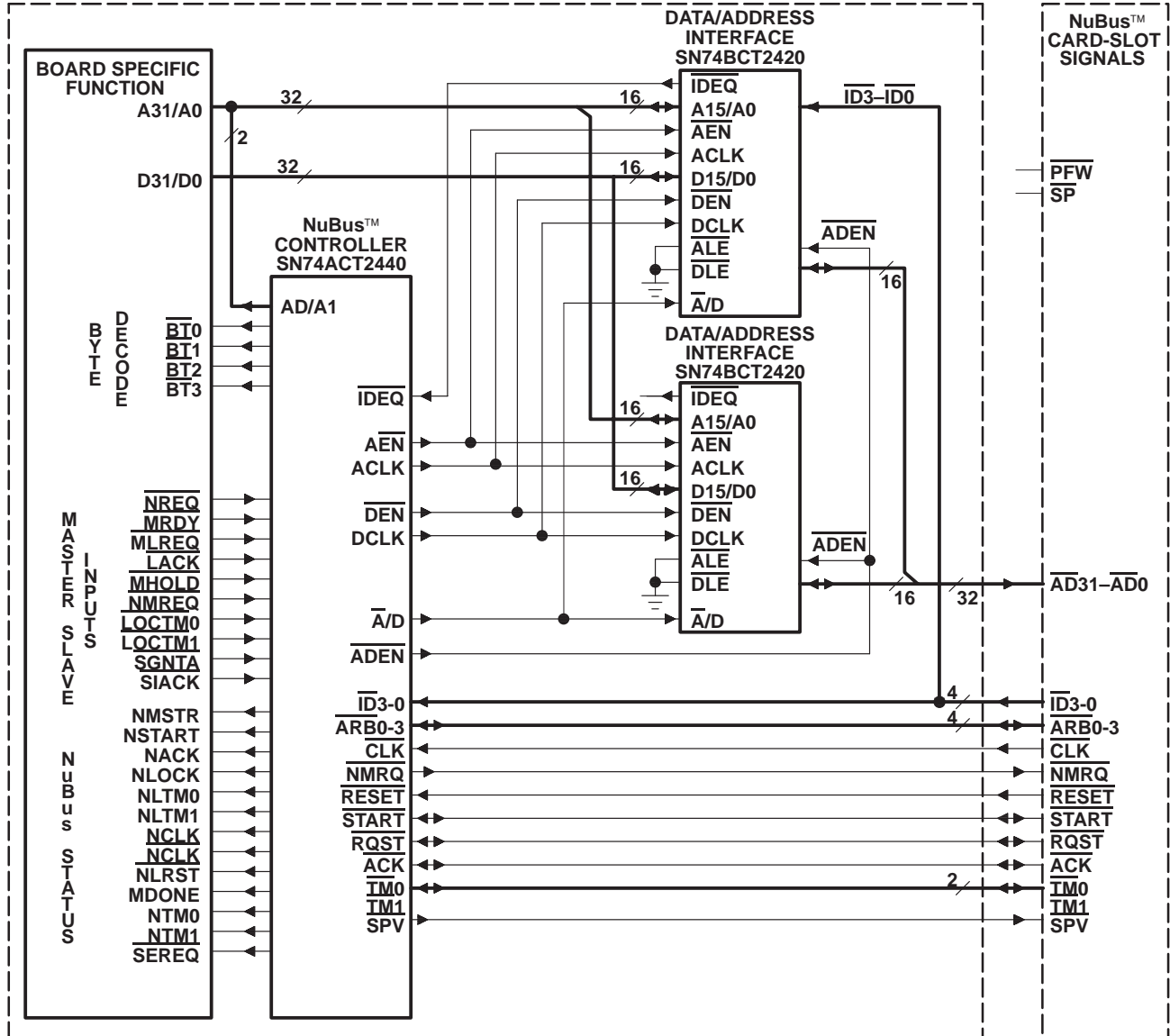


Figure 2. Typical NuBus™ Interface

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