

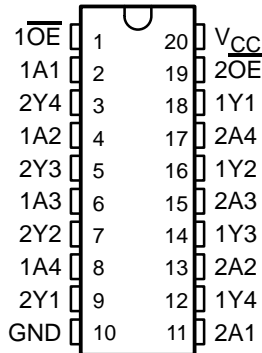
# SN54BCT240, SN74BCT240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS004F – OCTOBER 1987 – REVISED MARCH 2003

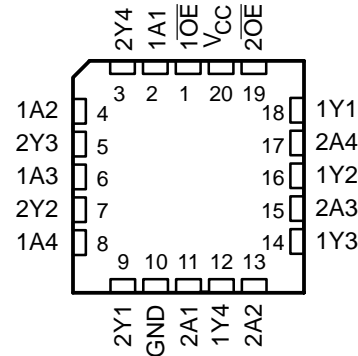
- Operating Voltage Range of 4.5 V to 5.5 V
- State-of-the-Art BiCMOS Design Significantly Reduces  $I_{CCZ}$

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- ESD Protection Exceeds JESD 22 – 2000-V Human-Body Model (A114-A)

SN54BCT240 . . . J OR W PACKAGE  
SN74BCT240 . . . DB, DW, N, OR NS PACKAGE  
(TOP VIEW)



SN54BCT240 . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the 'BCT241 and 'BCT244 devices, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical  $\overline{OE}$  (active-low output-enable) inputs, and complementary OE and  $\overline{OE}$  inputs. These devices feature high fan-out and improved fan-in.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74BCT240N	SN74BCT240N
	SOIC – DW	Tube	SN74BCT240DW	BCT240
		Tape and reel	SN74BCT240DWR	
	SOP – NS	Tape and reel	SN74BCT240NSR	BCT240
	SSOP – DB	Tape and reel	SN74BCT240DBR	BT240
–55°C to 125°C	CDIP – J	Tube	SNJ54BCT240J	SNJ54BCT240J
	CFP – W	Tube	SNJ54BCT240W	SNJ54BCT240W
	LCCC – FK	Tube	SNJ54BCT240FK	SNJ54BCT240FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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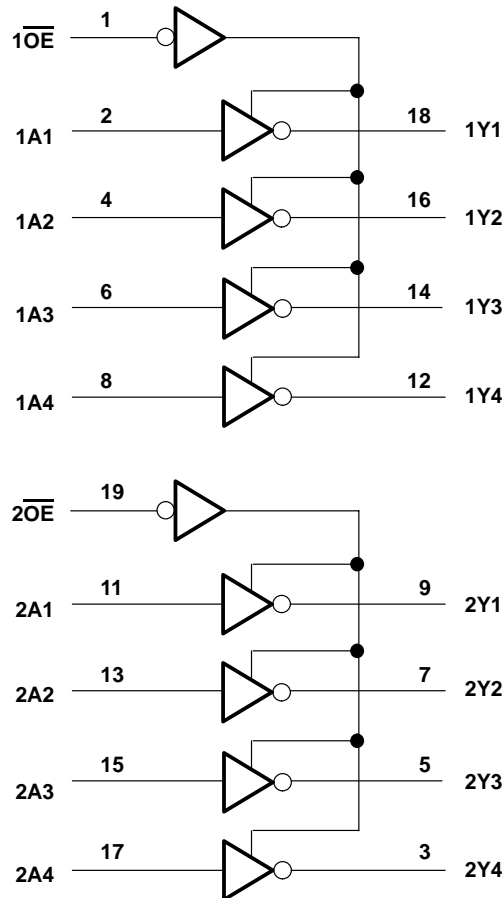
# SN54BCT240, SN74BCT240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS004F – OCTOBER 1987 – REVISED MARCH 2003

FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

## logic diagram (positive logic)



# SN54BCT240, SN74BCT240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS004F – OCTOBER 1987 – REVISED MARCH 2003

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$	–0.5 V to 5.5 V
Voltage range applied to any output in the high state, $V_O$	–0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$	–30 mA
Current into any output in the low state: SN54BCT240	96 mA
SN74BCT240	128 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

		SN54BCT240			SN74BCT240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{IK}$	Input clamp current			–18			–18	mA
$I_{OH}$	High-level output current			–12			–15	mA
$I_{OL}$	Low-level output current			48			64	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54BCT240, SN74BCT240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS004F – OCTOBER 1987 – REVISED MARCH 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT240			SN74BCT240			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA	-1.2			-1.2			V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -3 mA	2.4	3.3		2.4	3.3		V
		I <sub>OH</sub> = -12 mA	2	3.2					
		I <sub>OH</sub> = -15 mA				2	3.1		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA	0.38		0.55				V
		I <sub>OL</sub> = 64 mA				0.42	0.55		
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V	0.1			0.1			mA
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V	20			20			μA
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.5 V	-1			-1			mA
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V	50			50			μA
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V	-50			-50			μA
I <sub>OS‡</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0	-100		-225	-100		-225	mA
I <sub>CCH</sub>	V <sub>CC</sub> = 5.5 V,	Outputs open	19		31	19		31	mA
I <sub>CCL</sub>	V <sub>CC</sub> = 5.5 V,	Outputs open	46		71	46		71	mA
I <sub>CCZ</sub>	V <sub>CC</sub> = 5.5 V,	Outputs open	6		9	6		9	mA
C <sub>i</sub>	V <sub>CC</sub> = 5 V,	V <sub>I</sub> = 2.5 V or 0.5 V	6			6			pF
C <sub>o</sub>	V <sub>CC</sub> = 5 V,	V <sub>O</sub> = 2.5 V or 0.5 V	11			11			pF

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

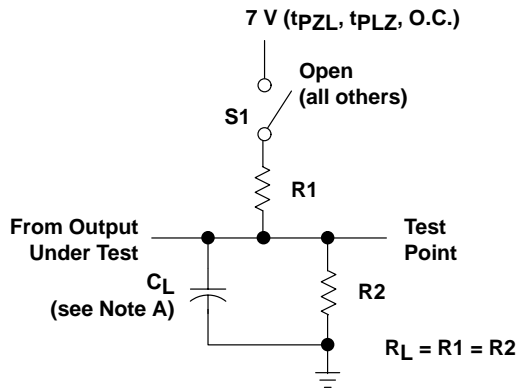
## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX§				UNIT
			BCT240			SN54BCT240		SN74BCT240		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	0.5	3.3	4.8	0.5	6.4	0.5	5.6	ns
t <sub>PHL</sub>			0.4	1.8	3.5	0.4	4.5	0.4	4	
t <sub>PZH</sub>	$\overline{OE}$	Y	1	6.4	7.9	1	9.2	1	8.8	ns
t <sub>PZL</sub>			1	7.5	9.4	1	10.8	1	10.5	
t <sub>PHZ</sub>	$\overline{OE}$	Y	1	6	6.8	1	8.5	1	8.1	ns
t <sub>PLZ</sub>			1	6.7	8.1	1	10.6	1	9.5	

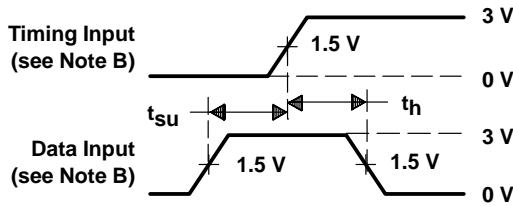
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



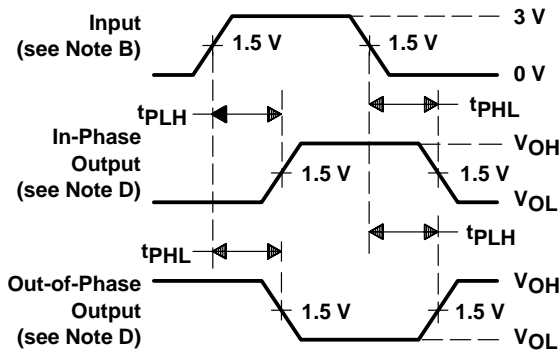
PARAMETER MEASUREMENT INFORMATION



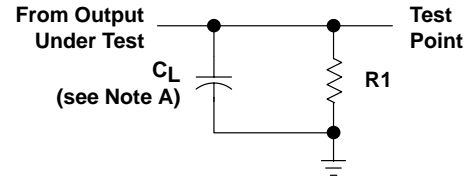
LOAD CIRCUIT FOR  
3-STATE AND OPEN-COLLECTOR OUTPUTS



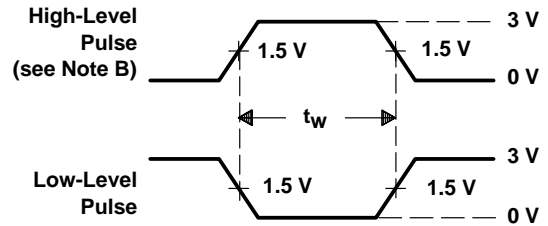
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



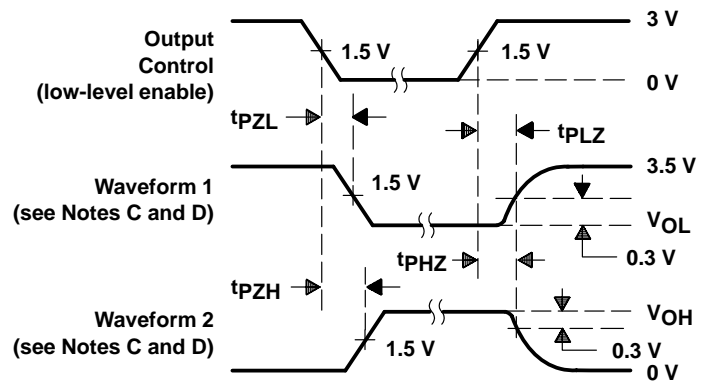
VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES (see Note D)



LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

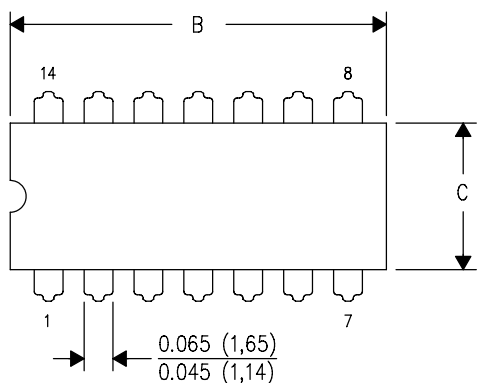
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $t_r = t_f \leq 2.5$  ns, duty cycle = 50%.  
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. The outputs are measured one at a time with one transition per measurement.  
E. When measuring propagation delay times of 3-state outputs, switch S1 is open.  
F. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

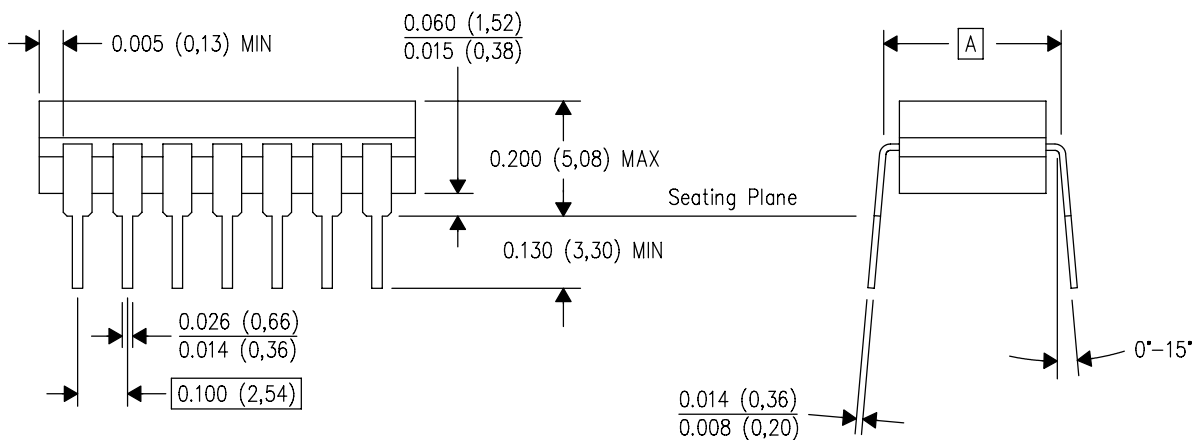
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

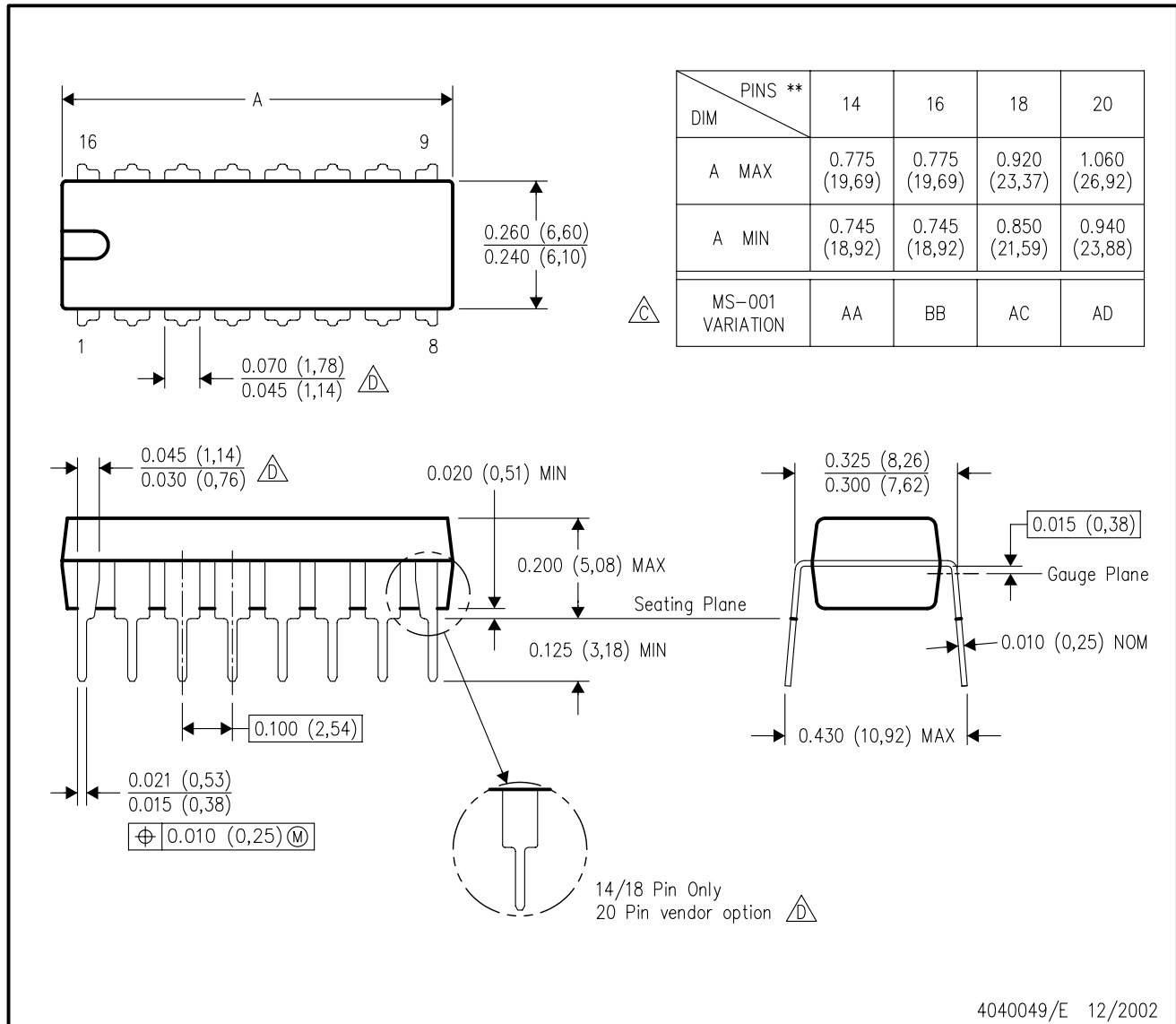


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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