

# SN54BCT2240, SN74BCT2240 OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

SCBS030E – SEPTEMBER 1988 – REVISED MARCH 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- State-of-the-Art BiCMOS Design Significantly Reduces  $I_{CCZ}$
- Output Ports Have Equivalent 33- $\Omega$  Series Resistors, So No External Resistors Are Required
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers

## description/ordering information

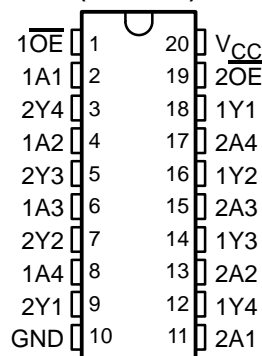
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the SN74BCT2241 and the 'BCT2244 devices, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ( $\overline{OE}$ ) inputs, and complementary OE and  $\overline{OE}$  inputs. These devices feature high fan-out and improved fan-in.

The 'BCT2240 devices are organized as two 4-bit line drivers with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

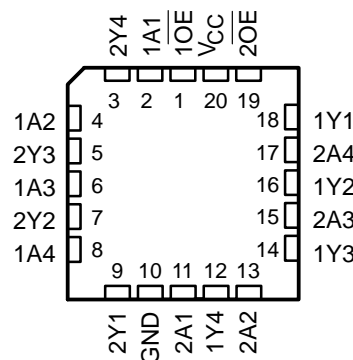
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The outputs, which are designed to source or sink up to 12 mA, include 33- $\Omega$  series resistors to reduce overshoot and undershoot.

SN54BCT2240 . . . J OR W PACKAGE  
SN74BCT2240 . . . DB, DW, N, OR NS PACKAGE  
(TOP VIEW)



SN54BCT2240 . . . FK PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74BCT2240N	SN74BCT2240N
	SOIC – DW	Tube	SN74BCT2240DW	BCT2240
		Tape and reel	SN74BCT2240DWR	
	SOP – NS	Tape and reel	SN74BCT2240NSR	BCT2240
	SSOP – DB	Tape and reel	SN74BCT2240DBR	BA240
–55°C to 125°C	CDIP – J	Tube	SNJ54BCT2240J	SNJ54BCT2240J
	CFP – W	Tube	SNJ54BCT2240W	SNJ54BCT2240W
	LCCC – FK	Tube	SNJ54BCT2240FK	SNJ54BCT2240FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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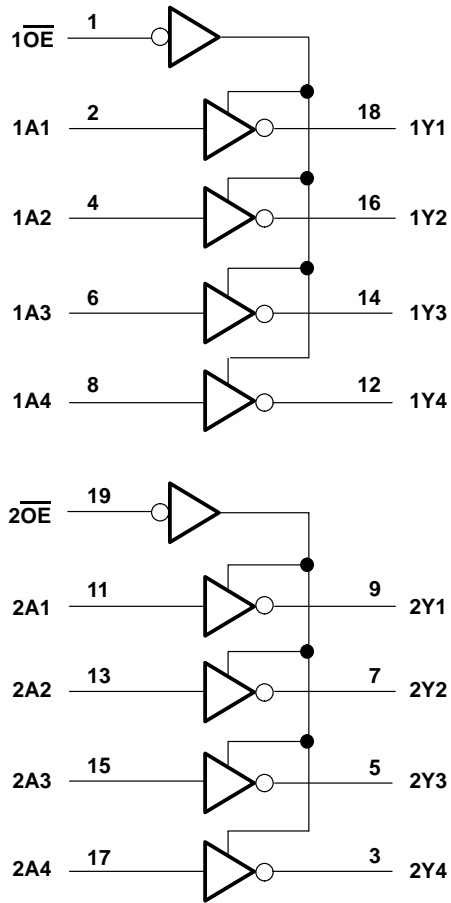
# SN54BCT2240, SN74BCT2240 OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

logic diagram (positive logic)





# SN54BCT2240, SN74BCT2240 OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 3)

		SN54BCT2240			SN74BCT2240			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>IK</sub>	Input clamp current			-18			-18	mA
I <sub>OH</sub>	High-level output current			-12			-12	mA
I <sub>OL</sub>	Low-level output current			12			12	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT2240			SN74BCT2240			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.2			-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -1 mA	2.4	3.3		2.4	3.3		V
		I <sub>OH</sub> = -12 mA	2	3.2		2	3.2		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 1 mA		0.15	0.5		0.15	0.5	V
		I <sub>OL</sub> = 12 mA		0.35	0.8		0.35	0.8	
I <sub>I</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V			0.1			0.1	mA
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 2.7 V			20			20	μA
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 0.5 V			-1			-1	mA
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			50			50	μA
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V			-50			-50	μA
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0	-100		-225	-100		-225	mA
I <sub>CCH</sub>	V <sub>CC</sub> = 5.5 V,	Outputs open		19	32		19	32	mA
I <sub>CCL</sub>	V <sub>CC</sub> = 5.5 V,	Outputs open		46	76		46	76	mA
I <sub>CCZ</sub>	V <sub>CC</sub> = 5.5 V,	Outputs open		6	8		6	8	mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

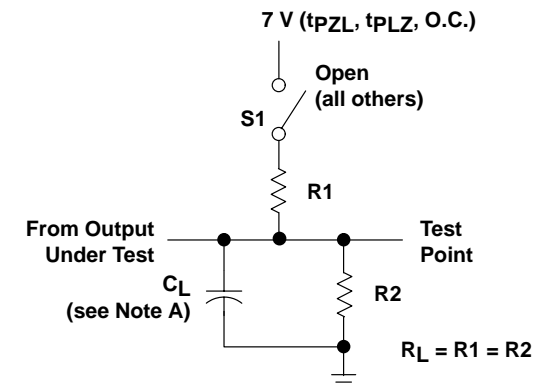
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

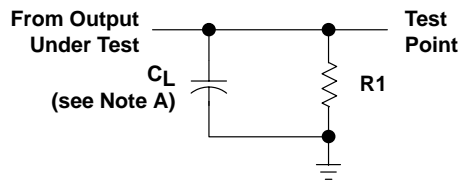
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54BCT2240		SN74BCT2240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	0.5	3.4	4.8	0.5	6.3	0.5	5.7	ns
t <sub>PHL</sub>			0.5	2.8	4	0.5	4.6	0.5	4.4	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Y	2.6	6.2	8.2	2.6	10.1	2.6	9.3	ns
t <sub>PZL</sub>			4.3	8.8	10.9	4.3	12.9	4.3	12.4	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Y	2	5.3	7.1	2	9.2	2	8.7	ns
t <sub>PLZ</sub>			2.2	6.7	8.5	2.2	12.2	2.2	10.6	



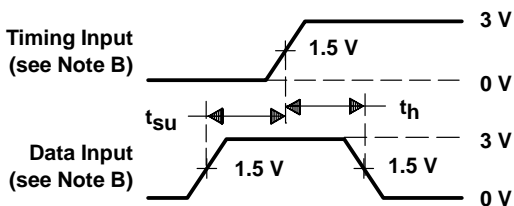
PARAMETER MEASUREMENT INFORMATION



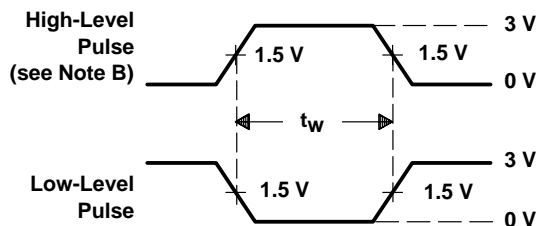
LOAD CIRCUIT FOR  
 3-STATE AND OPEN-COLLECTOR OUTPUTS



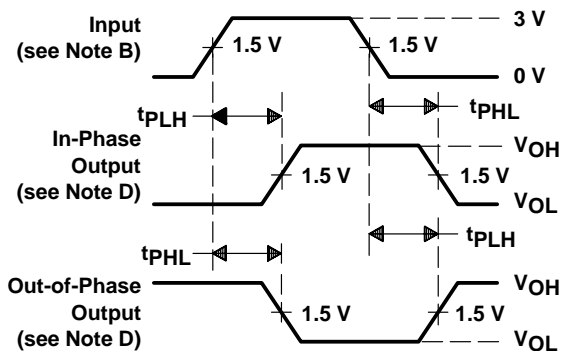
LOAD CIRCUIT FOR  
 TOTEM-POLE OUTPUTS



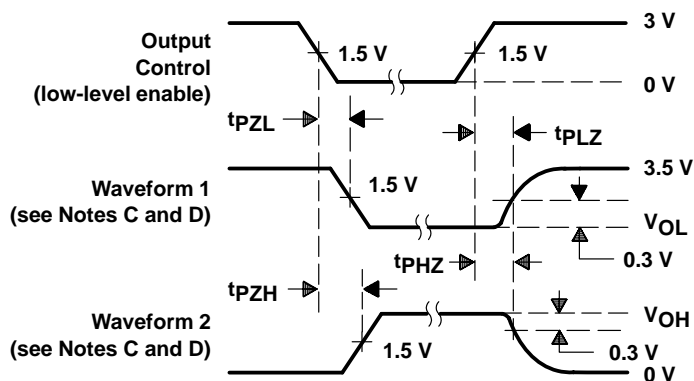
VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 PULSE DURATION



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $t_r = t_f \leq 2.5$  ns, duty cycle = 50%.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. When measuring propagation delay times of 3-state outputs, switch S1 is open.  
 F. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

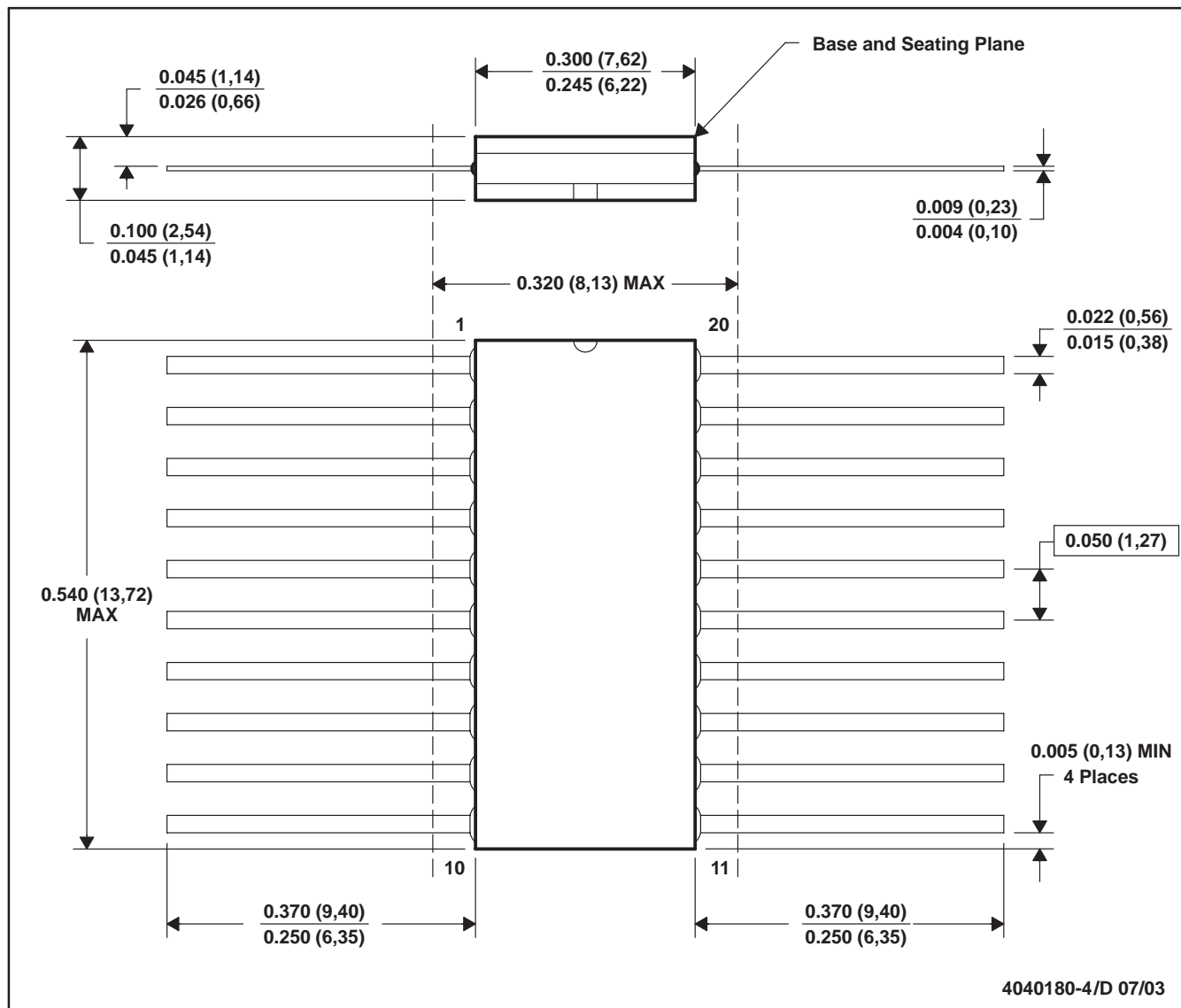


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only.  
 E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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