

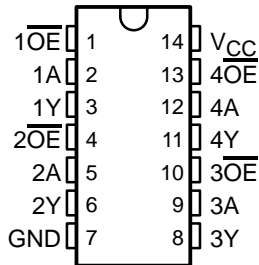
# SN54BCT125A, SN74BCT125A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCBS032F – SEPTEMBER 1988 – REVISED MARCH 2003

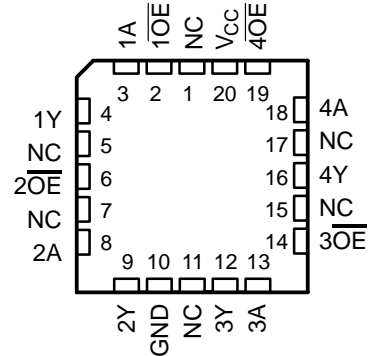
- Operating Voltage Range of 4.5 V to 5.5 V
- State-of-the-Art BiCMOS Design Significantly Reduces  $I_{CCZ}$

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers

SN54BCT125A . . . J OR W PACKAGE  
SN74BCT125A . . . D, N, OR NS PACKAGE  
(TOP VIEW)



SN54BCT125A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'BCT125A bus buffers feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ( $\overline{OE}$ ) input is high.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74BCT125AN	SN74BCT125AN
	SOIC – D	Tube	SN74BCT125AD	BCT125A
		Tape and reel	SN74BCT125ADR	
	SOP – NS	Tape and reel	SN74BCT125ANSR	BCT125A
–55°C to 125°C	CDIP – J	Tube	SNJ54BCT125AJ	SNJ54BCT125AJ
	CFP – W	Tube	SNJ54BCT125AW	SNJ54BCT125AW
	LCCC – FK	Tube	SNJ54BCT125AFK	SNJ54BCT125AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

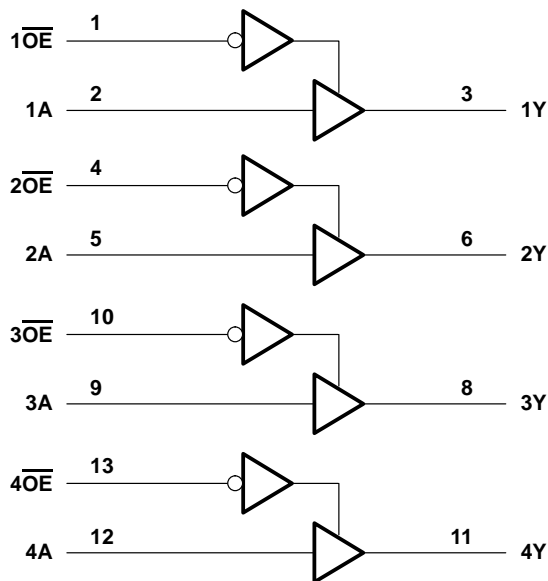
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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## logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	.....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	.....	-0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$	.....	-0.5 V to 5.5 V
Voltage range applied to any output in the high state, $V_O$	.....	-0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	.....	-30 mA
Current into any output in the low state, $I_O$ : SN54BCT125A	.....	96 mA
SN74BCT125A	.....	128 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	.....	86°C/W
N package	.....	80°C/W
NS package	.....	76°C/W
Storage temperature range, $T_{stg}$	.....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.



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# SN54BCT125A, SN74BCT125A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 3)

		SN54BCT125A			SN74BCT125A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage	0.8			0.8			V
$I_{IK}$	Input clamp current	-18			-18			mA
$I_{OH}$	High-level output current	-12			-15			mA
$I_{OL}$	Low-level output current	48			64			mA
$T_A$	Operating free-air temperature	-55	125		0	70		°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54BCT125A		SN74BCT125A		UNIT
			MIN	TYP†	MAX	MIN	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$	-1.2		-1.2		V
$V_{OH}$	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.3	2.4	3.3	V
		$I_{OH} = -12\text{ mA}$	2	3.2			
		$I_{OH} = -15\text{ mA}$			2	3.1	
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$	0.38	0.55			V
		$I_{OL} = 64\text{ mA}$			0.42	0.55	
$I_I$	$V_{CC} = 0$ ,	$V_I = 7\text{ V}$	0.1		0.1		mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$	35		25		$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.5\text{ V}$	-20		-20		$\mu\text{A}$
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.7\text{ V}$	50		50		$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0.5\text{ V}$	-50		-50		$\mu\text{A}$
$I_{OS}^\ddagger$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0$	-100	-225	-100	-225	mA
$I_{CCH}$	$V_{CC} = 5.5\text{ V}$ ,	Outputs open	19	31	19	31	mA
$I_{CCL}$	$V_{CC} = 5.5\text{ V}$ ,	Outputs open	46	49	46	49	mA
$I_{CCZ}$	$V_{CC} = 5.5\text{ V}$ ,	Outputs open	6	14	6	14	mA
$C_i$	$V_{CC} = 5\text{ V}$ ,	$V_I = 2.5\text{ V}$ or $0.5\text{ V}$	4		4		pF
$C_o$	$V_{CC} = 5\text{ V}$ ,	$V_O = 2.5\text{ V}$ or $0.5\text{ V}$	9		9		pF

† All typical values are at  $V_{CC} = 5\text{ V}$ .

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

# SN54BCT125A, SN74BCT125A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

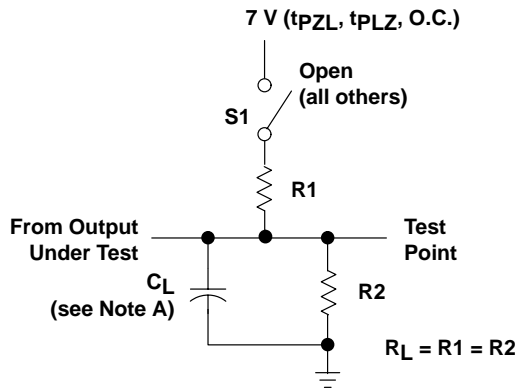
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## switching characteristics (see Figure 1)

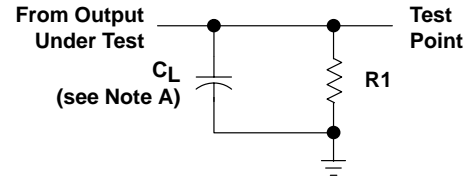
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = MIN to MAX <sup>§</sup>				UNIT
			'BCT125A			SN54BCT125A		SN74BCT125A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	1.6	3.5	5.2	1.6	6	1.6	5.7	ns
t <sub>PHL</sub>			2.7	5	6.9	2.7	8	2.7	7.7	
t <sub>PZH</sub>	$\overline{OE}$	Y	3.4	6.7	9	3.4	11.1	3.4	10.3	ns
t <sub>PZL</sub>			5	8.2	10.4	5	12.8	5	11.7	
t <sub>PHZ</sub>	$\overline{OE}$	Y	3	5.8	7.4	3	9.4	3	8.9	ns
t <sub>PLZ</sub>			2.8	5.5	7.3	2.8	9.9	2.8	8.6	

<sup>§</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

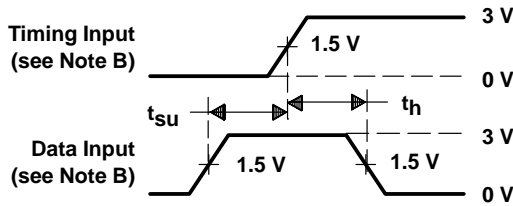
PARAMETER MEASUREMENT INFORMATION



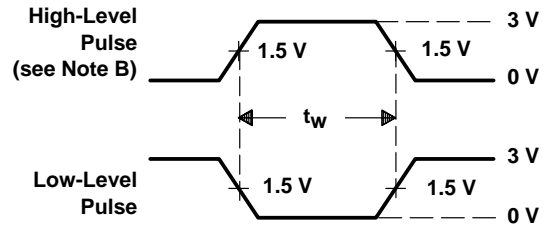
LOAD CIRCUIT FOR 3-STATE AND OPEN-COLLECTOR OUTPUTS



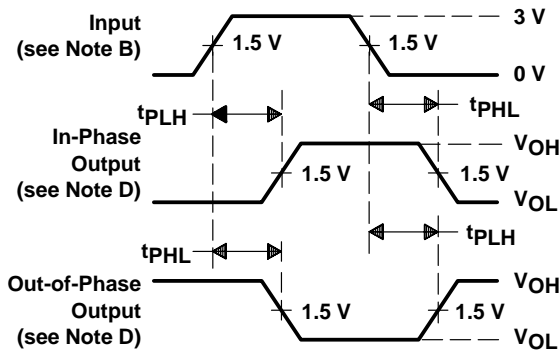
LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS



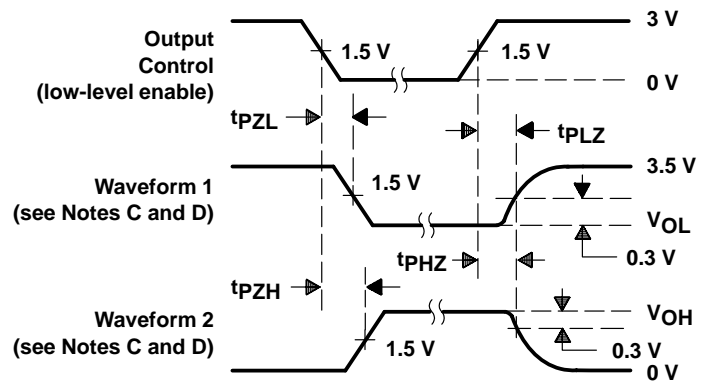
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $t_r = t_f \leq 2.5$  ns, duty cycle = 50%.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one transition per measurement.  
 E. When measuring propagation delay times of 3-state outputs, switch S1 is open.  
 F. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AB.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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