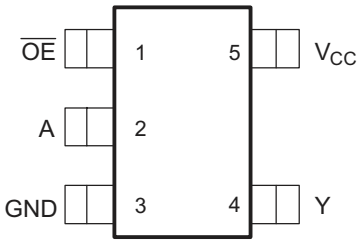
LOW-POWER SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

Check for Samples: SN74AUP1G125

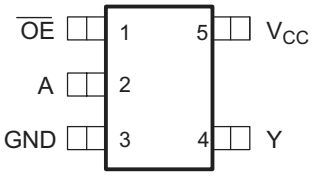
FEATURES

- **Available in the Texas Instruments NanoStar™ Package**
- **Low Static-Power Consumption (I_{CC} = 0.9 µA Max)**
- **Low Dynamic-Power Consumption (C_{pd} = 4 pF Typ at 3.3 V)**
- **Low Input Capacitance (C_i = 1.5 pF Typ)**
- **Low Noise – Overshoot and Undershoot <10% of V_{CC}**
- **Input-Disable Feature Allows Floating Input Conditions**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input**
- **Wide Operating V_{CC} Range of 0.8 V to 3.6 V**
- **Optimized for 3.3-V Operation**
- **3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation**
- **t_{pd} = 4.6 ns Max at 3.3 V**
- **Suitable for Point-to-Point Applications**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**

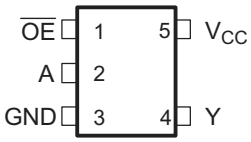
DBV PACKAGE (TOP VIEW)



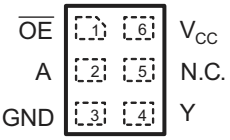
DCK PACKAGE (TOP VIEW)



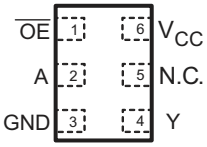
DRL PACKAGE (TOP VIEW)



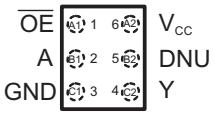
DRY PACKAGE (TOP VIEW)



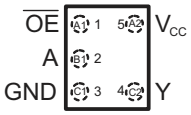
DSF PACKAGE (TOP VIEW)



YFP PACKAGE (TOP VIEW)



YZP/YZT PACKAGE (TOP VIEW)



N.C. – No internal connection.

DNU – Do not use

See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity (see Figure 1 and Figure 2).

This bus buffer gate is a single line driver with a 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high. This device has the input-disable feature, which allows floating input signals.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

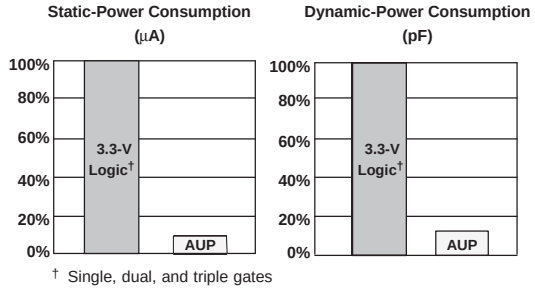


Figure 1. AUP – The Lowest-Power Family

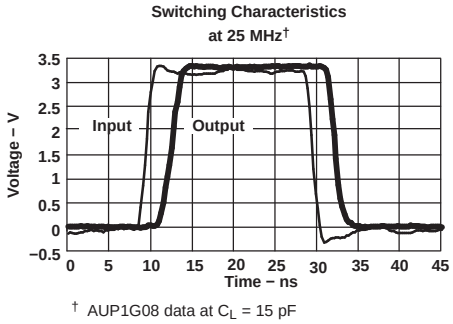


Figure 2. Excellent Signal Integrity

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP1G125YFPR	_ _ _ HM _
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP1G125YZPR	_ _ _ HM _
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YZT (Pb-free)	Reel of 3000	SN74AUP1G125YZTR	_ _ _ HM _
	QFN – DRY	Reel of 5000	SN74AUP1G125DRYR	HM
	uQFN – DSF	Reel of 5000	SN74AUP1G125DSFR	HM
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G125DBVR	H25_
		Reel of 250	SN74AUP1G125DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G125DCKR	HM_
		Reel of 250	SN74AUP1G125DCKT	
	SOT (SOT-553) – DRL	Reel of 4000	SN74AUP1G125DRLR	HM_

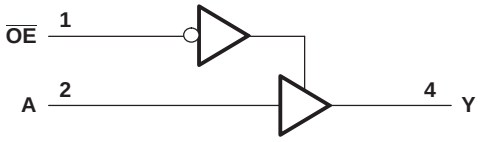
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the wafer fab/assembly site.
YFP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X(1)	Z

(1) Floating inputs allowed.

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)		–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	4.6	V
V_O	Output voltage range in the high or low state(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance(3)	DBV package		206	°C/W
		DCK package		252	
		DRL package		142	
		DSF package		300	
		DRY package		234	
		YFP/YZP package		132	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}	3.6	V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}	3.6	
		V_{CC} = 2.3 V to 2.7 V	1.6	3.6	
		V_{CC} = 3 V to 3.6 V	2	3.6	
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V	0	0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V	0	0.7	
		V_{CC} = 3 V to 3.6 V	0	0.9	
V_O	Output voltage	Active state	0	V_{CC}	V
		3-state	0	3.6	
I_{OH}	High-level output current	V_{CC} = 0.8 V		–20	μA
		V_{CC} = 1.1 V		–1.1	mA
		V_{CC} = 1.4 V		–1.7	
		V_{CC} = 1.65 V		–1.9	
		V_{CC} = 2.3 V		–3.1	
		V_{CC} = 3 V		–4	
I_{OL}	Low-level output current	V_{CC} = 0.8 V		20	μA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow of Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{OL}		I_{OH} = –20 µA	0.8 V to 3.6 V	V_{CC} – 0.1			V_{CC} – 0.1		V
		I_{OH} = –1.1 mA	1.1 V	0.75 × V_{CC}			0.7 × V_{CC}		
		I_{OH} = –1.7 mA	1.4 V	1.11			1.03		
		I_{OH} = –1.9 mA	1.65 V	1.32			1.3		
		I_{OH} = –2.3 mA	2.3 V	2.05			1.97		
		I_{OH} = –3.1 mA		1.9			1.85		
		I_{OH} = –2.7 mA	3 V	2.72			2.67		
		I_{OH} = –4 mA		2.6			2.55		
V_{OL}		I_{OL} = 20 µA	0.8 V to 3.6 V			0.1		0.1	V
		I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}		0.3 × V_{CC}	
		I_{OL} = 1.7 mA	1.4 V			0.31		0.37	
		I_{OL} = 1.9 mA	1.65 V			0.31		0.35	
		I_{OL} = 2.3 mA	2.3 V			0.31		0.33	
		I_{OL} = 3.1 mA				0.44		0.45	
		I_{OL} = 2.7 mA	3 V			0.31		0.33	
		I_{OL} = 4 mA				0.44		0.45	
I_I	A or $\overline{OE}$ input	V_I = GND to 3.6 V	0 V to 3.6 V			0.1		0.5	µA
I_{off}		V_I or V_O = 0 V to 3.6 V	0 V			0.2		0.6	µA
ΔI_{off}		V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.2		0.6	µA
I_{OZ}		V_O = V_{CC} or GND	3.6 V			0.1		0.5	µA
I_{CC}		V_I = GND or (V_{CC} to 3.6 V), $\overline{OE}$ = GND, I_O = 0	0.8 V to 3.6 V			0.5		0.9	µA
ΔI_{CC}	A input	V_I = V_{CC} – 0.6 V(1), I_O = 0	3.3 V			40		50	µA
	$\overline{OE}$ input					110		120	
	All inputs	V_I = GND to 3.6 V, $\overline{OE}$ = V_{CC} (2)	0.8 V to 3.6 V			0		0	
C_I		V_I = V_{CC} or GND	0 V		1.5				pF
			3.6 V		1.5				
C_o		V_O = V_{CC} or GND	3.6 V		3				pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND
(2) To show I_{CC} is very low when the input-disable feature is enabled

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V		18.1				ns
			1.2 V ± 0.1 V	4.3	7.4	12.6	2.7	15.3	
			1.5 V ± 0.1 V	3.3	5.2	8.5	1	10.2	
			1.8 V ± 0.15 V	2.6	4.1	6.8	1.3	8.3	
			2.5 V ± 0.2 V	2	2.9	4.7	1.1	5.8	
			3.3 V ± 0.3 V	1.7	2.4	3.8	1	4.6	
t_{en}	$\overline{OE}$	Y	0.8 V		19.1				ns
			1.2 V ± 0.1 V	5.1	9.3	15.9	3.6	19.2	
			1.5 V ± 0.1 V	4.1	6.6	10.5	2.5	12.7	
			1.8 V ± 0.15 V	3.2	5.3	8.7	2.1	10.3	
			2.5 V ± 0.2 V	2.5	3.8	6	1.6	7.2	
			3.3 V ± 0.3 V	2.1	3.2	4.9	1.4	5.9	
t_{dis}	$\overline{OE}$	Y	0.8 V		12.1				ns
			1.2 V ± 0.1 V	2.4	4.1	6.9	2.2	7.7	
			1.5 V ± 0.1 V	1.8	2.9	4.5	1.7	5.1	
			1.8 V ± 0.15 V	1	2.9	4.3	1.5	4.7	
			2.5 V ± 0.2 V	1	1.8	2.7	1	3.3	
			3.3 V ± 0.3 V	1.2	2.2	3.2	1.1	4	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		20.5				ns
			1.2 V ± 0.1 V	4.6	8.4	13.7	3.6	16.6	
			1.5 V ± 0.1 V	3.5	5.9	9.3	2.4	11.1	
			1.8 V ± 0.15 V	3.9	4.7	7.5	1.3	9.1	
			2.5 V ± 0.2 V	2.3	3.4	5.3	1.6	6.4	
			3.3 V ± 0.3 V	2.1	2.8	4.3	1.4	5.2	
t_{en}	$\overline{OE}$	Y	0.8 V		21.8				ns
			1.2 V ± 0.1 V	4.9	10.2	16.8	4.4	20.2	
			1.5 V ± 0.1 V	3.9	7.3	11.2	3.3	13.5	
			1.8 V ± 0.15 V	3.4	5.8	9.2	2.7	11	
			2.5 V ± 0.2 V	2.5	4.3	6.4	2.1	7.8	
			3.3 V ± 0.3 V	2.1	3.7	5.4	1.9	6.4	
t_{dis}	$\overline{OE}$	Y	0.8 V		13				ns
			1.2 V ± 0.1 V	3.8	6.6	11.7	1.2	14	
			1.5 V ± 0.1 V	2.2	4.7	7.9	1.3	9.3	
			1.8 V ± 0.15 V	2.4	4.4	6.4	2.2	7.5	
			2.5 V ± 0.2 V	1.3	3.1	4.9	1.2	5.4	
			3.3 V ± 0.3 V	1.9	3.4	5	1.9	5.6	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		22.5				ns
			1.2 V ± 0.1 V	5.8	9.3	15.1	4.3	17.9	
			1.5 V ± 0.1 V	4.4	6.6	10.2	3	12.1	
			1.8 V ± 0.15 V	3.5	5.3	8.3	2.3	9.9	
			2.5 V ± 0.2 V	2.7	3.9	5.8	1.9	7	
			3.3 V ± 0.3 V	2.4	3.2	4.7	1.8	5.7	
t_{en}	$\overline{OE}$	Y	0.8 V		25.2				ns
			1.2 V ± 0.1 V	7	11.3	18.1	5.4	21.4	
			1.5 V ± 0.1 V	5.5	8.1	12.2	4.1	14.5	
			1.8 V ± 0.15 V	4.3	6.5	10.1	3.3	12	
			2.5 V ± 0.2 V	3.4	4.8	7.1	2.6	8.4	
			3.3 V ± 0.3 V	2.9	4.1	5.9	2.3	6.9	
t_{dis}	$\overline{OE}$	Y	0.8 V		14				ns
			1.2 V ± 0.1 V	3.7	5.8	8.2	3.3	11	
			1.5 V ± 0.1 V	5.5	3.9	5.9	2.1	8	
			1.8 V ± 0.15 V	3.3	4.5	6.6	2.9	7.4	
			2.5 V ± 0.2 V	2.3	3.2	4.3	1.8	5.1	
			3.3 V ± 0.3 V	2.4	4.8	6.2	3.1	6.7	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

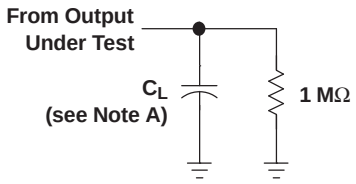
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A or B	Y	0.8 V		29				ns
			1.2 V ± 0.1 V	7.4	12	18.7	6.6	21.4	
			1.5 V ± 0.1 V	5.7	8.6	12.5	4.9	14.7	
			1.8 V ± 0.15 V	4.8	6.9	10.1	3.1	12	
			2.5 V ± 0.2 V	3.9	5.1	7.2	3.3	8.7	
			3.3 V ± 0.3 V	3.5	4.8	6	3	7	
t_{en}	$\overline{OE}$	Y	0.8 V		33.4				ns
			1.2 V ± 0.1 V	8.8	14.1	21.8	7.4	25.5	
			1.5 V ± 0.1 V	6.9	10.1	14.6	5.6	17.4	
			1.8 V ± 0.15 V	5.6	8.1	12	4.7	14.1	
			2.5 V ± 0.2 V	4.3	6.1	8.5	3.8	10	
			3.3 V ± 0.3 V	3.7	5.2	7.1	3.4	8.3	
t_{dis}	$\overline{OE}$	Y	0.8 V		17.7				ns
			1.2 V ± 0.1 V	5.8	10	16	3.7	16	
			1.5 V ± 0.1 V	5.7	7.7	10.9	1	10.7	
			1.8 V ± 0.15 V	4.5	7.7	9.8	4.4	12.5	
			2.5 V ± 0.2 V	3.9	5.6	7.4	3.2	9	
			3.3 V ± 0.3 V	3.3	8.4	10.7	6.6	10.8	

OPERATING CHARACTERISTICS

T_A = 25°c

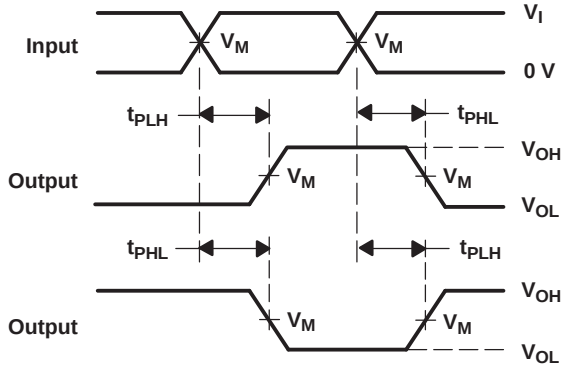
PARAMETER			TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	f = 10 MHz	0.8 V	3.8	pF
				1.2 V ± 0.1 V	3.8	
				1.5 V ± 0.1 V	3.7	
				1.8 V ± 0.15 V	3.8	
				2.5 V ± 0.2 V	3.9	
				3.3 V ± 0.3 V	4	
		Outputs disabled	f = 10 MHz	0.8 V	0	
				1.2 V ± 0.1 V	0	
				1.5 V ± 0.1 V	0	
				1.8 V ± 0.15 V	0	
				2.5 V ± 0.2 V	0	
				3.3 V ± 0.3 V	0	

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Duration)

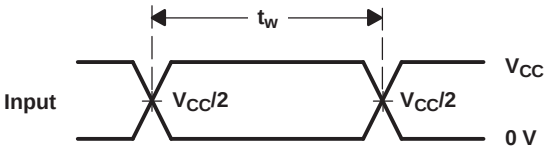


LOAD CIRCUIT

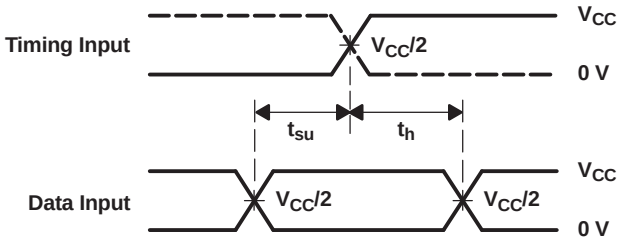
	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION

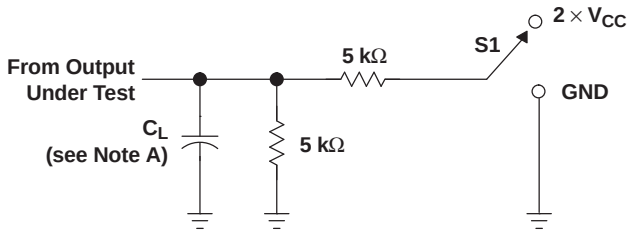


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

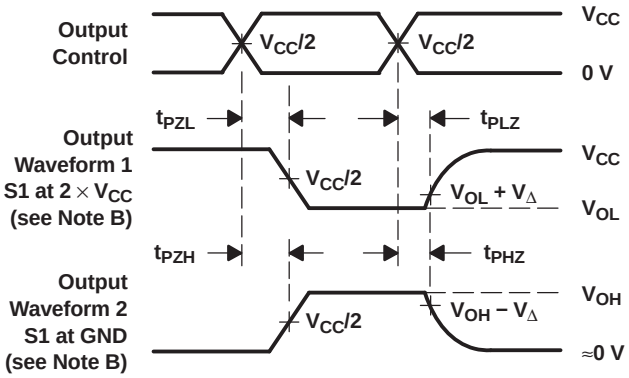
PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



TEST	S1
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	$2 \times V_{CC}$ GND

LOAD CIRCUIT

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision K (November 2012) to Revision L	Page
• Changed $\overline{Y}$ to Y for pin 4 in DSF Package pin out	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AUP1G125DBVRE4	ACTIVE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85		Samples
74AUP1G125DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H25R	Samples
74AUP1G125DBVTE4	ACTIVE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85		Samples
74AUP1G125DBVTG4	ACTIVE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85		Samples
74AUP1G125DCKRE4	ACTIVE	SC70	DCK	5		TBD	Call TI	Call TI	-40 to 85		Samples
74AUP1G125DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HM5 ~ HMF ~ HMK ~ HMR)	Samples
74AUP1G125DCKTE4	ACTIVE	SC70	DCK	5		TBD	Call TI	Call TI	-40 to 85		Samples
74AUP1G125DCKTG4	ACTIVE	SC70	DCK	5		TBD	Call TI	Call TI	-40 to 85		Samples
74AUP1G125DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HM7 ~ HMR)	Samples
SN74AUP1G125DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H25R	Samples
SN74AUP1G125DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H25R	Samples
SN74AUP1G125DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HM5 ~ HMF ~ HMK ~ HMR)	Samples
SN74AUP1G125DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HM5 ~ HMR)	Samples
SN74AUP1G125DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HM7 ~ HMR)	Samples
SN74AUP1G125DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HM	Samples
SN74AUP1G125DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HM	Samples
SN74AUP1G125YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		(HM2 ~ HM7 ~ HMN)	Samples
SN74AUP1G125YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(HM7 ~ HMN)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1G125YZTR	ACTIVE	DSBGA	YZT	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(HM ~ HM2 ~ HM7)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

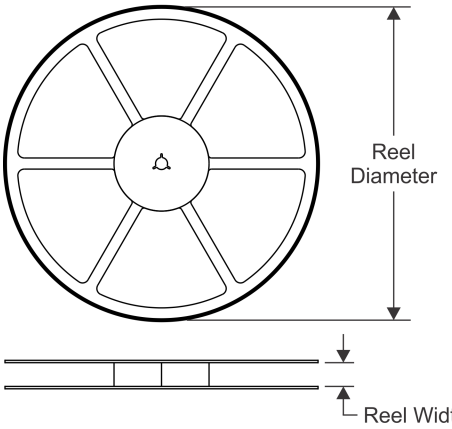
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

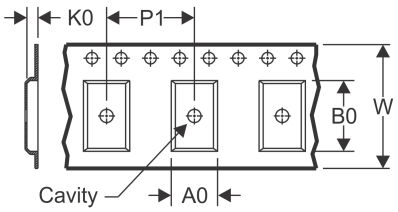
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

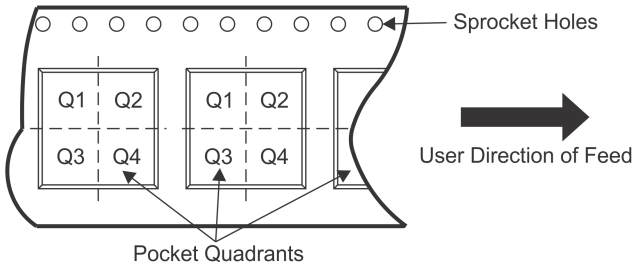


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

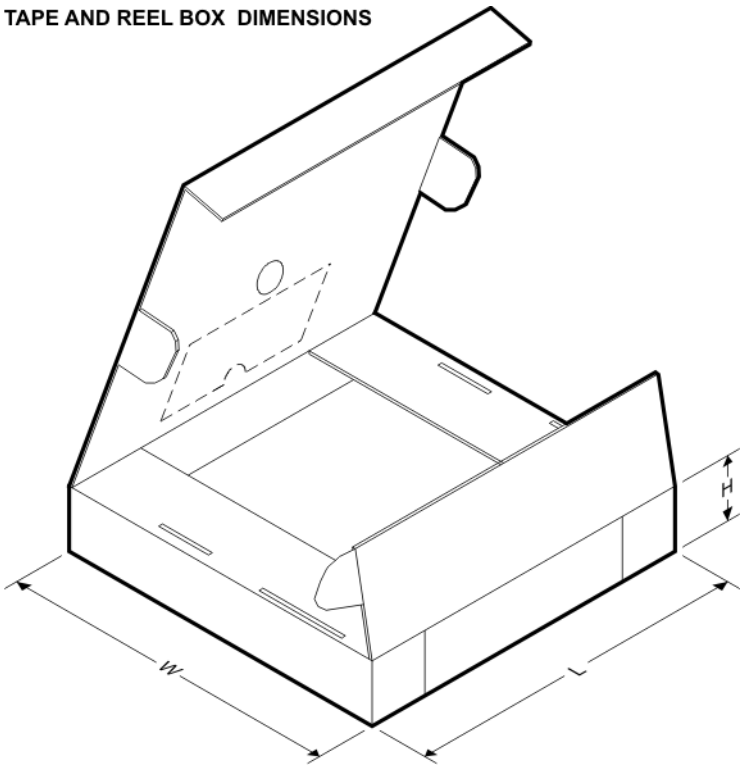
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G125DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G125DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G125DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G125DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G125DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP1G125DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G125DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G125DRLR	SOT	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AUP1G125DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G125DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G125YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G125YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

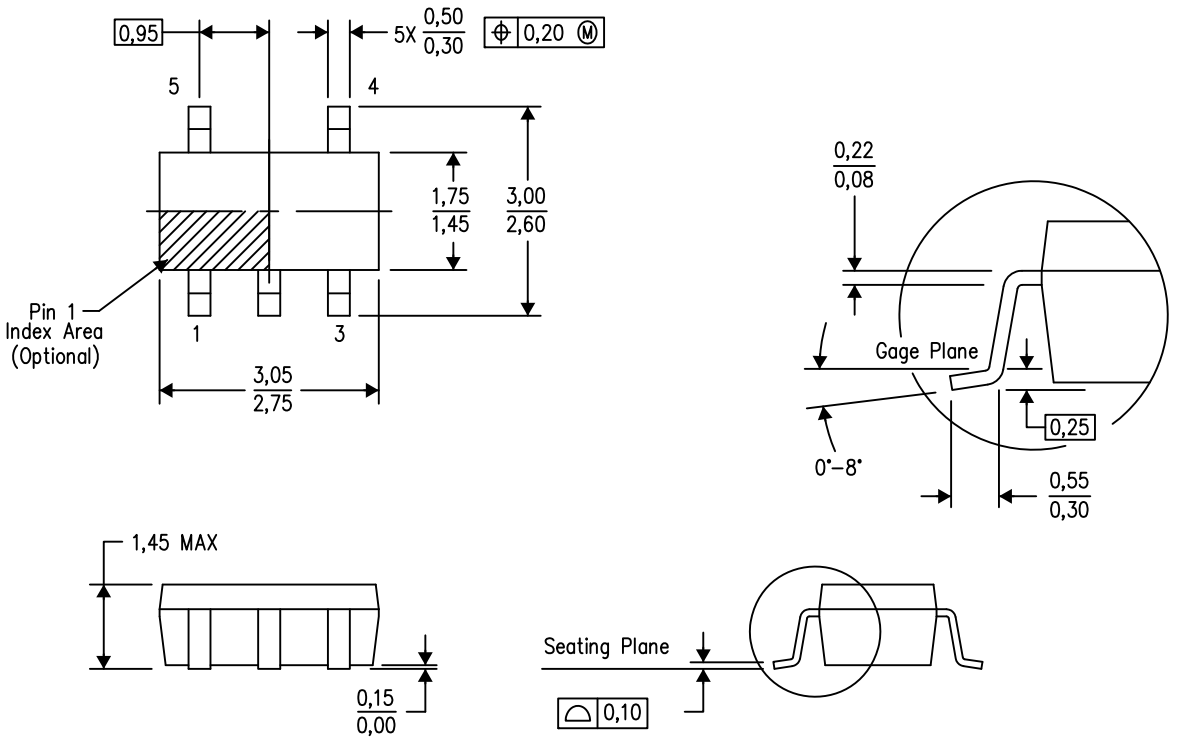
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G125DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G125DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G125DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G125DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUP1G125DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74AUP1G125DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G125DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G125DRLR	SOT	DRL	5	4000	184.0	184.0	19.0
SN74AUP1G125DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G125DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1G125YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G125YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

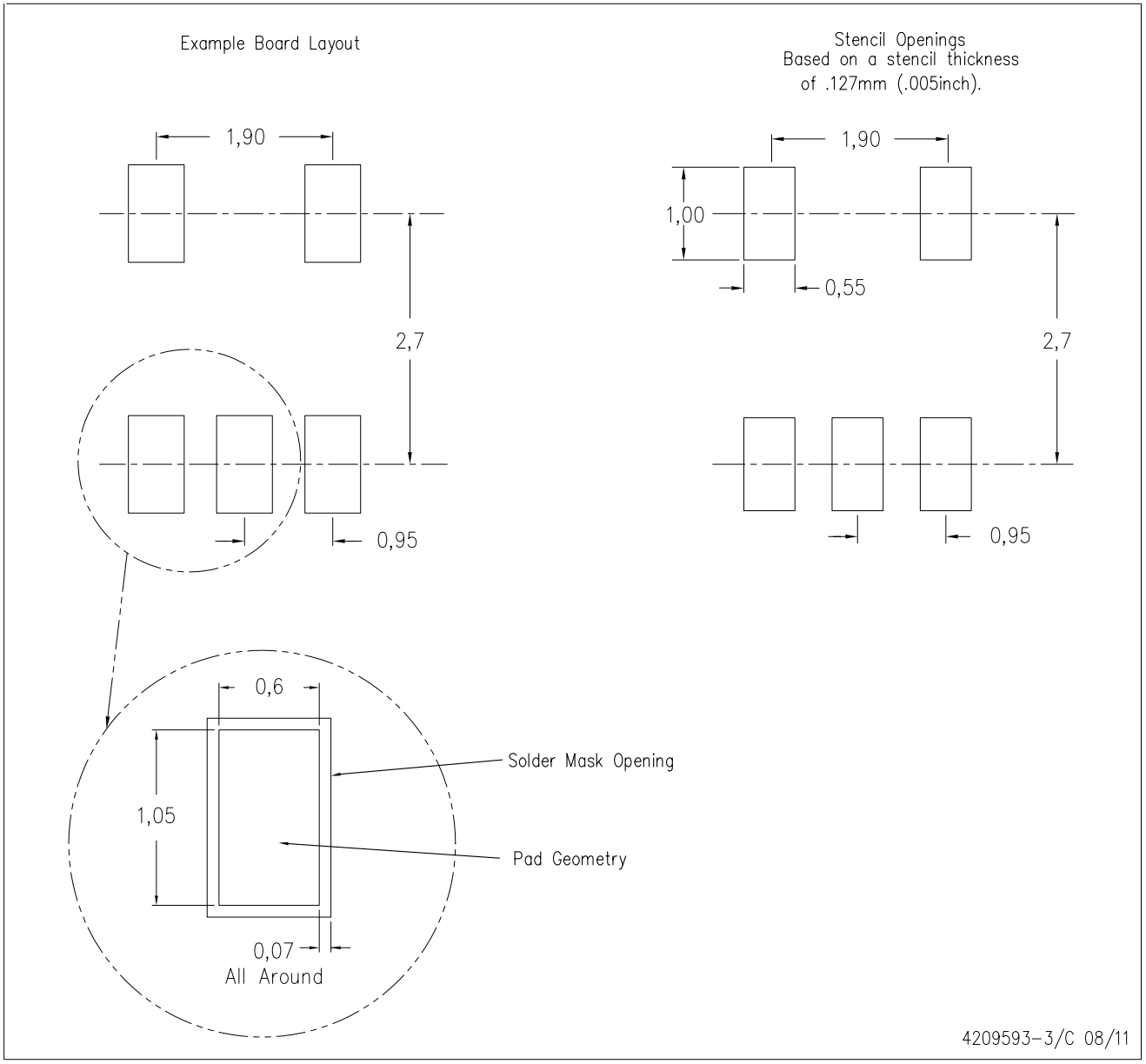
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/L 08/2013

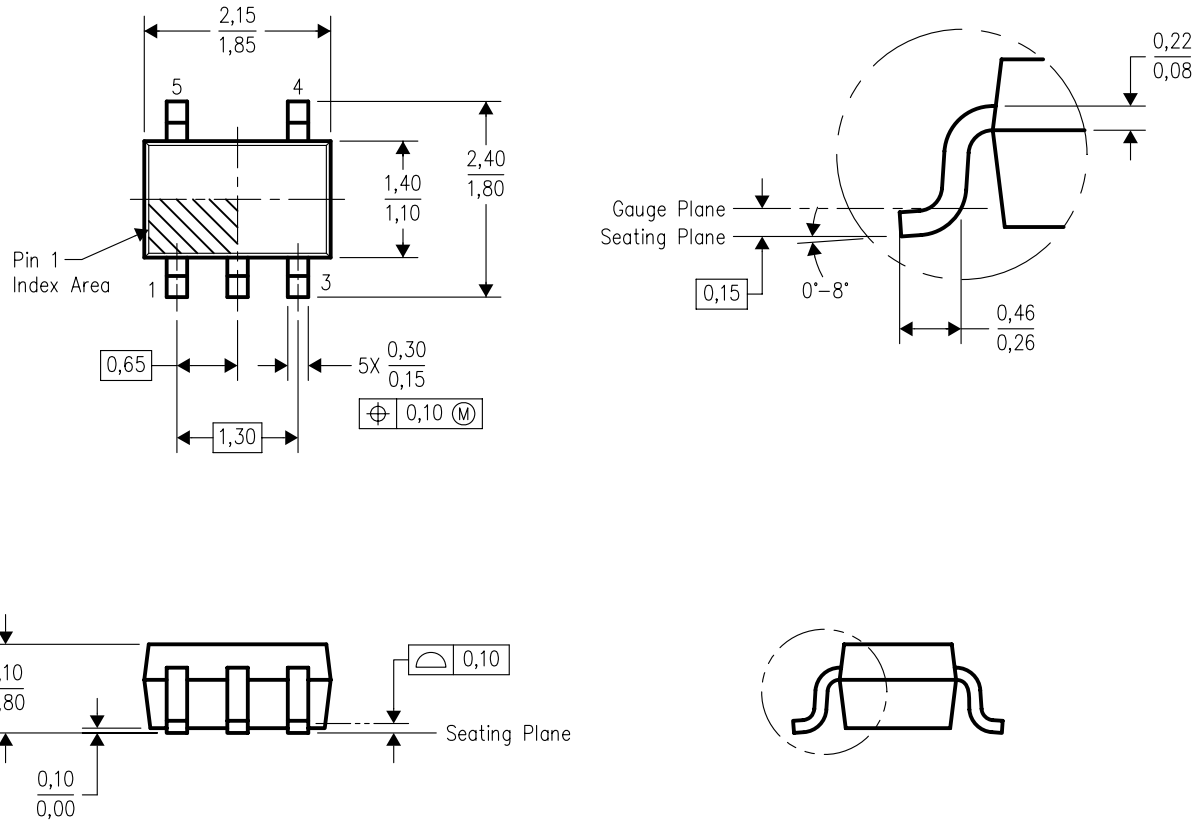
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

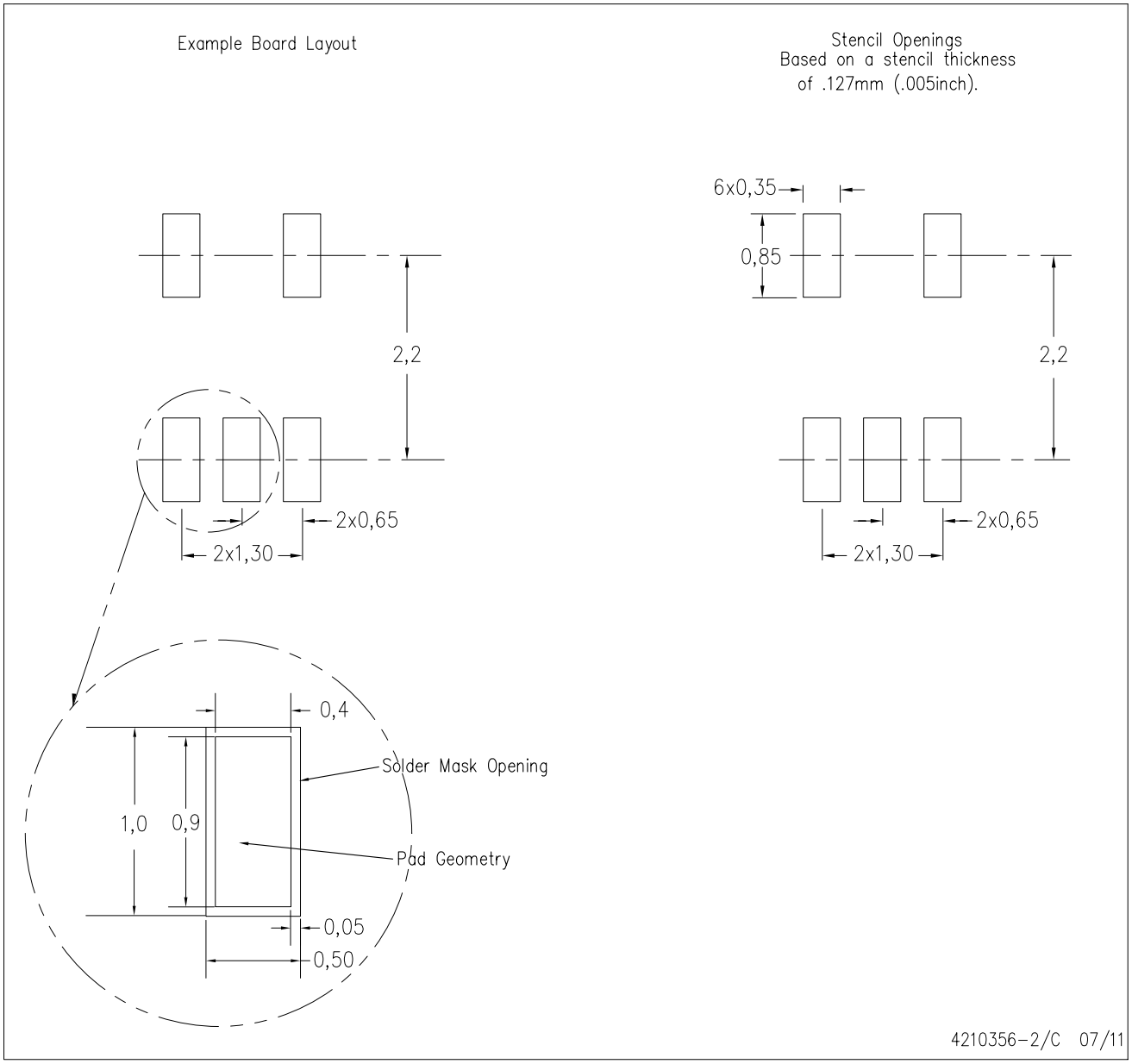
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



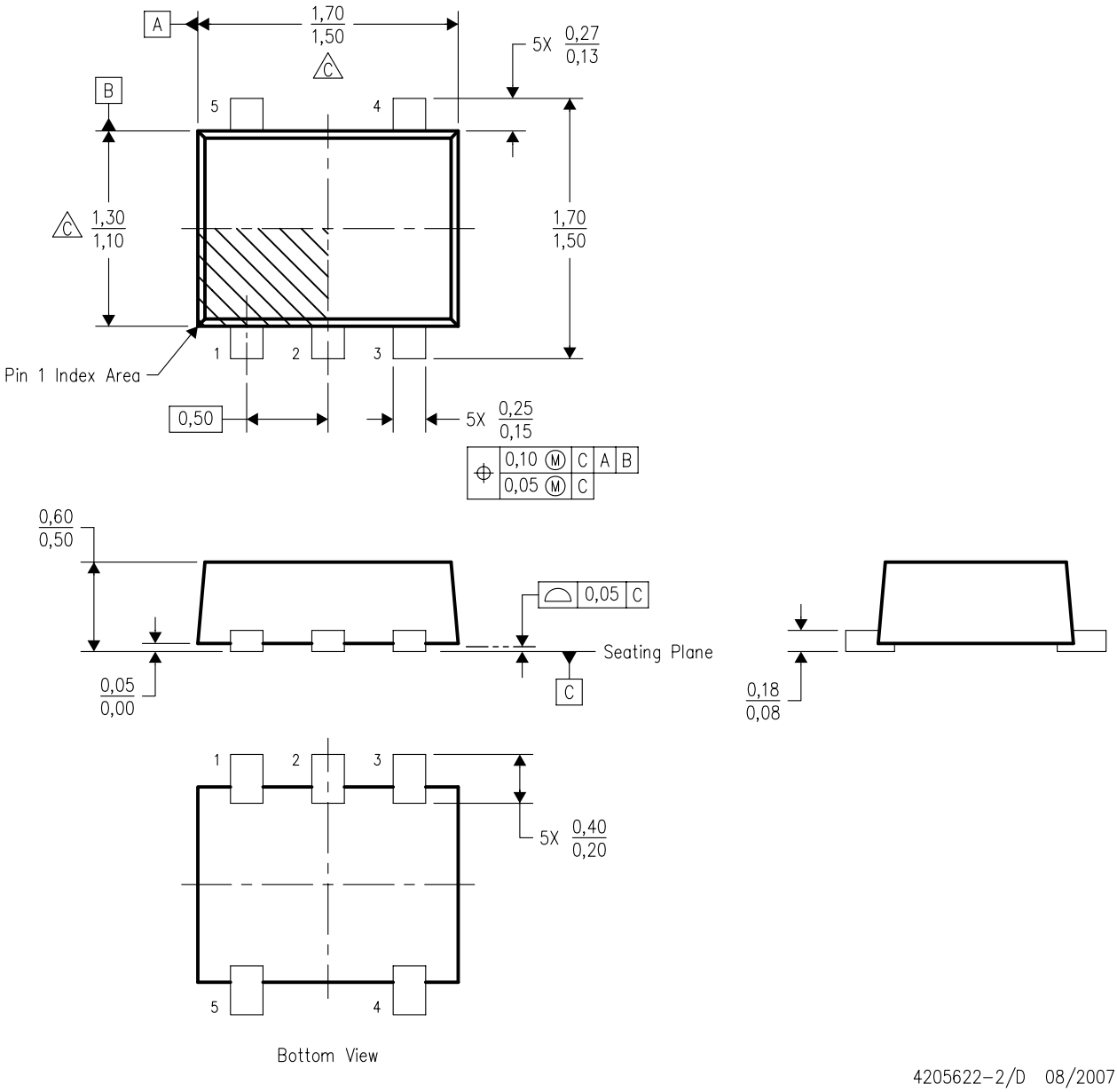
4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



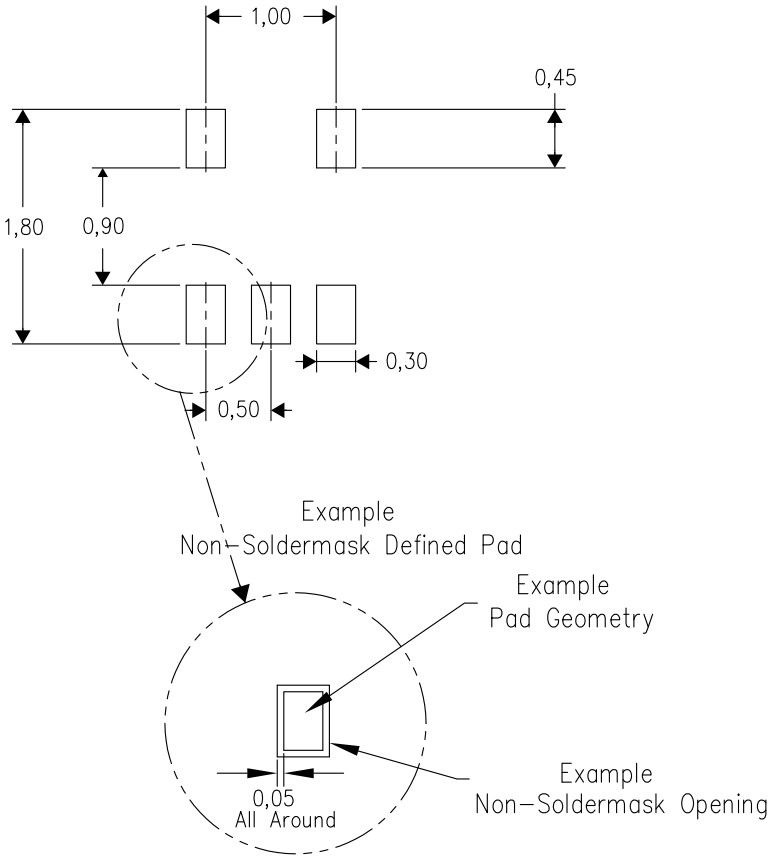
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.



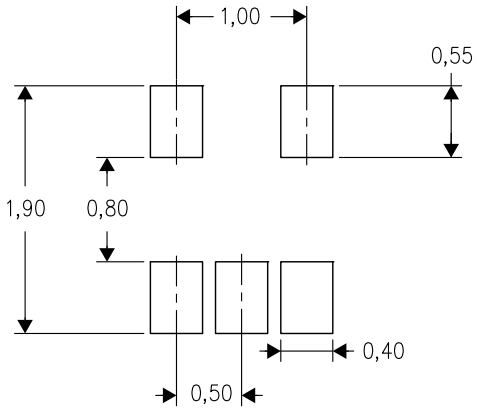
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R–PDSO–N5) PLASTIC SMALL OUTLINE

Example Board Layout



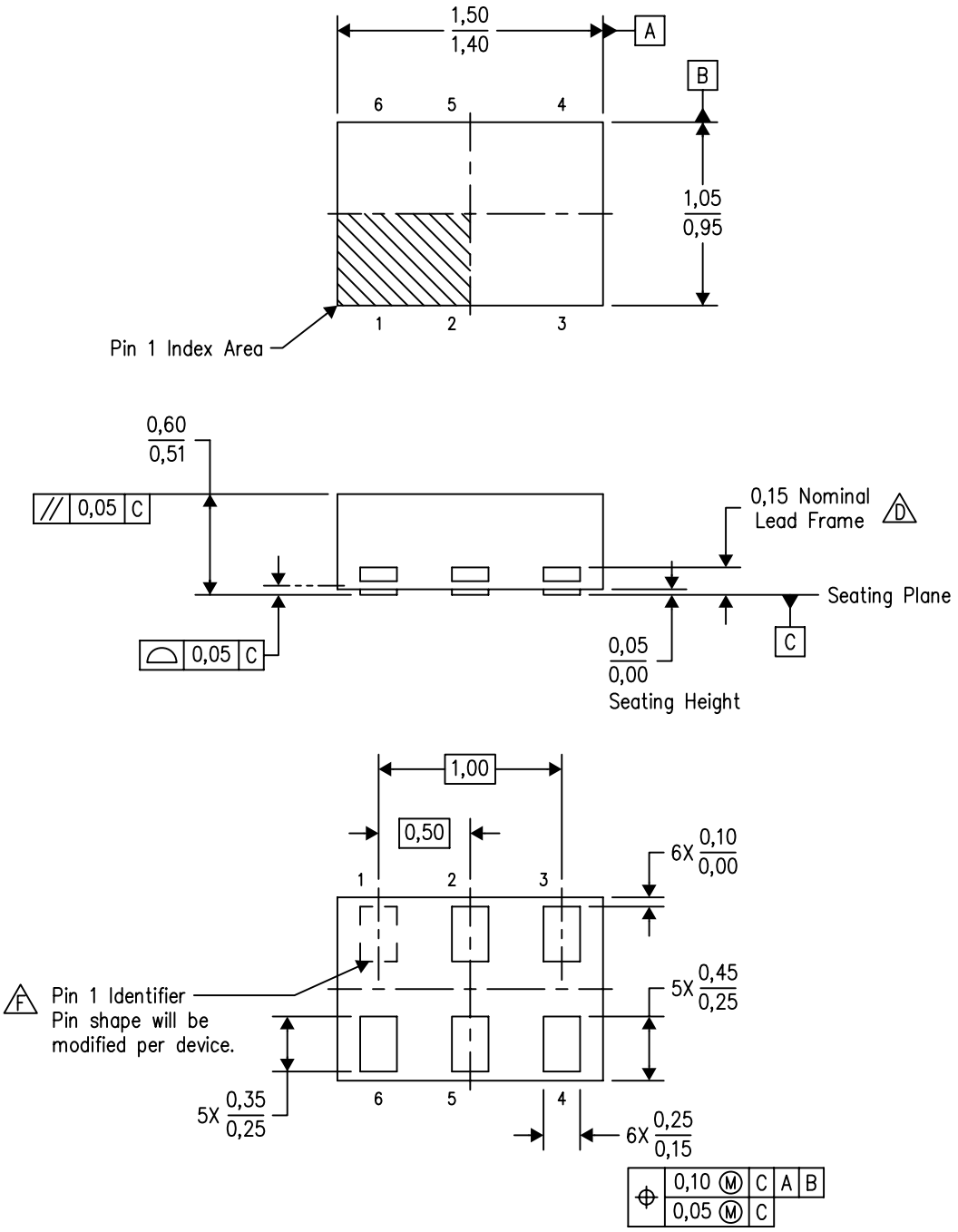
Example Stencil Design
(Note E)



4208207–2/E 06/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

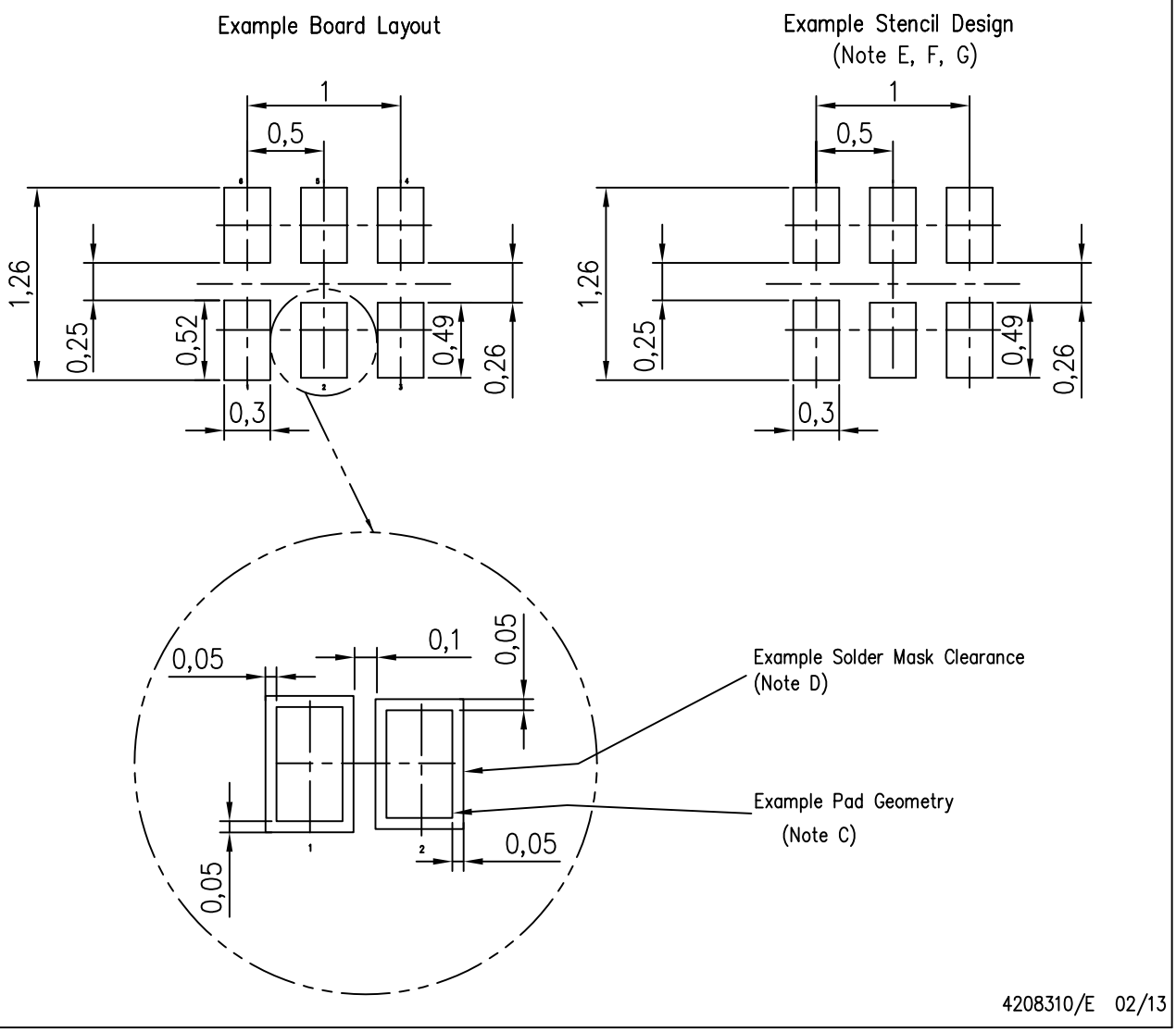
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4207181/F 12/11

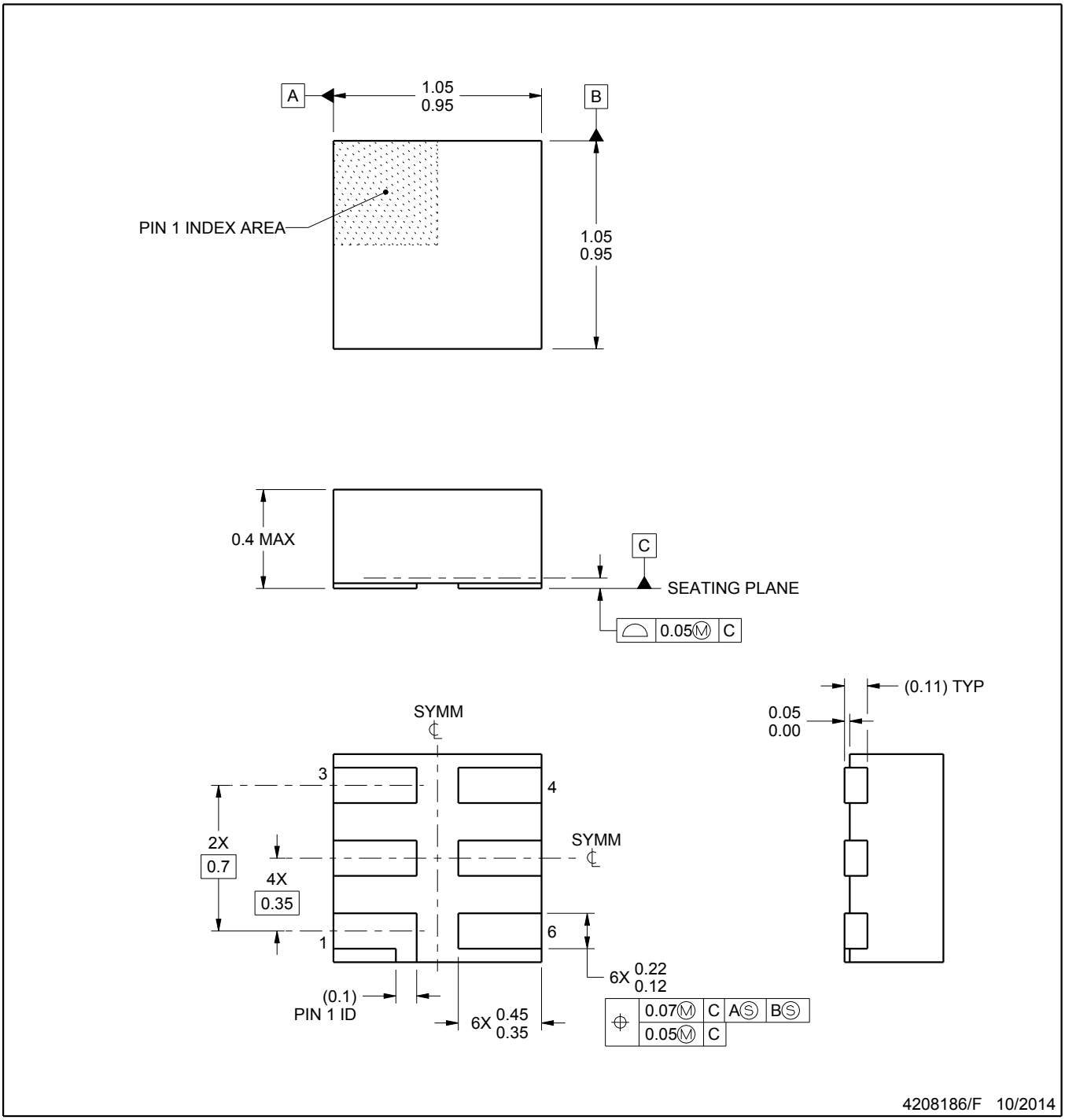
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

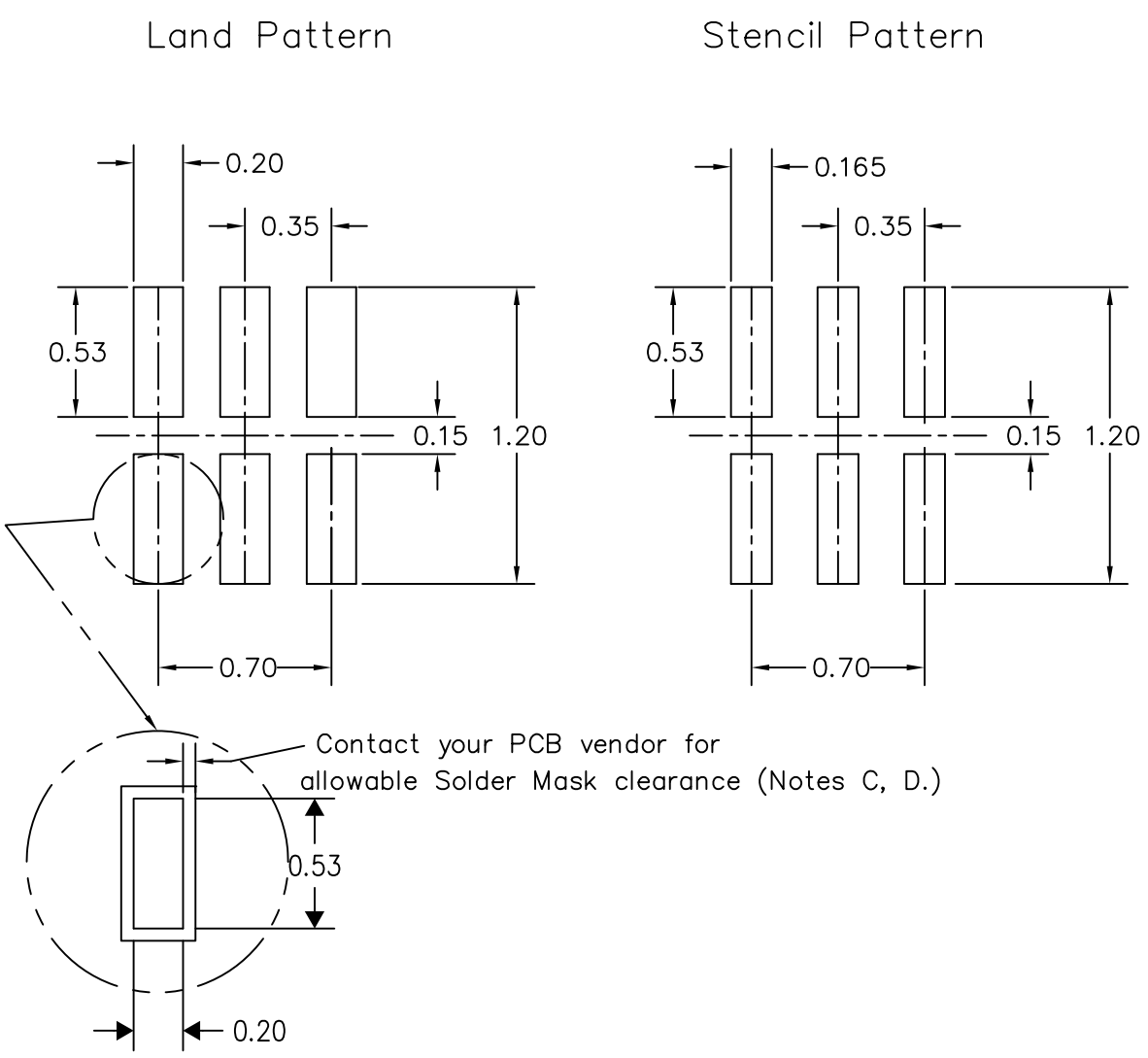
DSF (S-PX2SON-N6) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

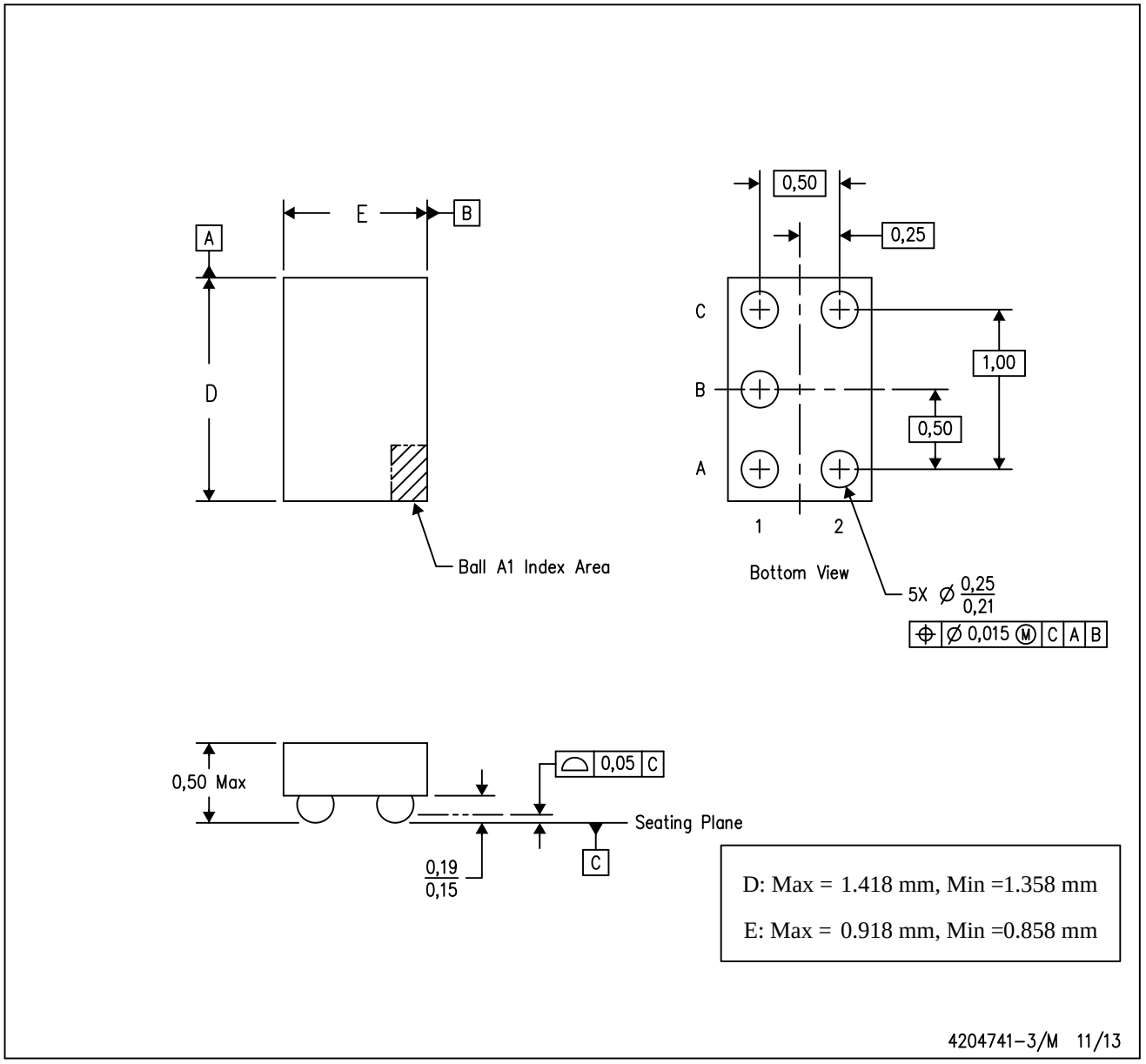
DSF (S–PX2SON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4210277/D 05/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
H. Component placement force should be minimized to prevent excessive paste block deformation.

YZP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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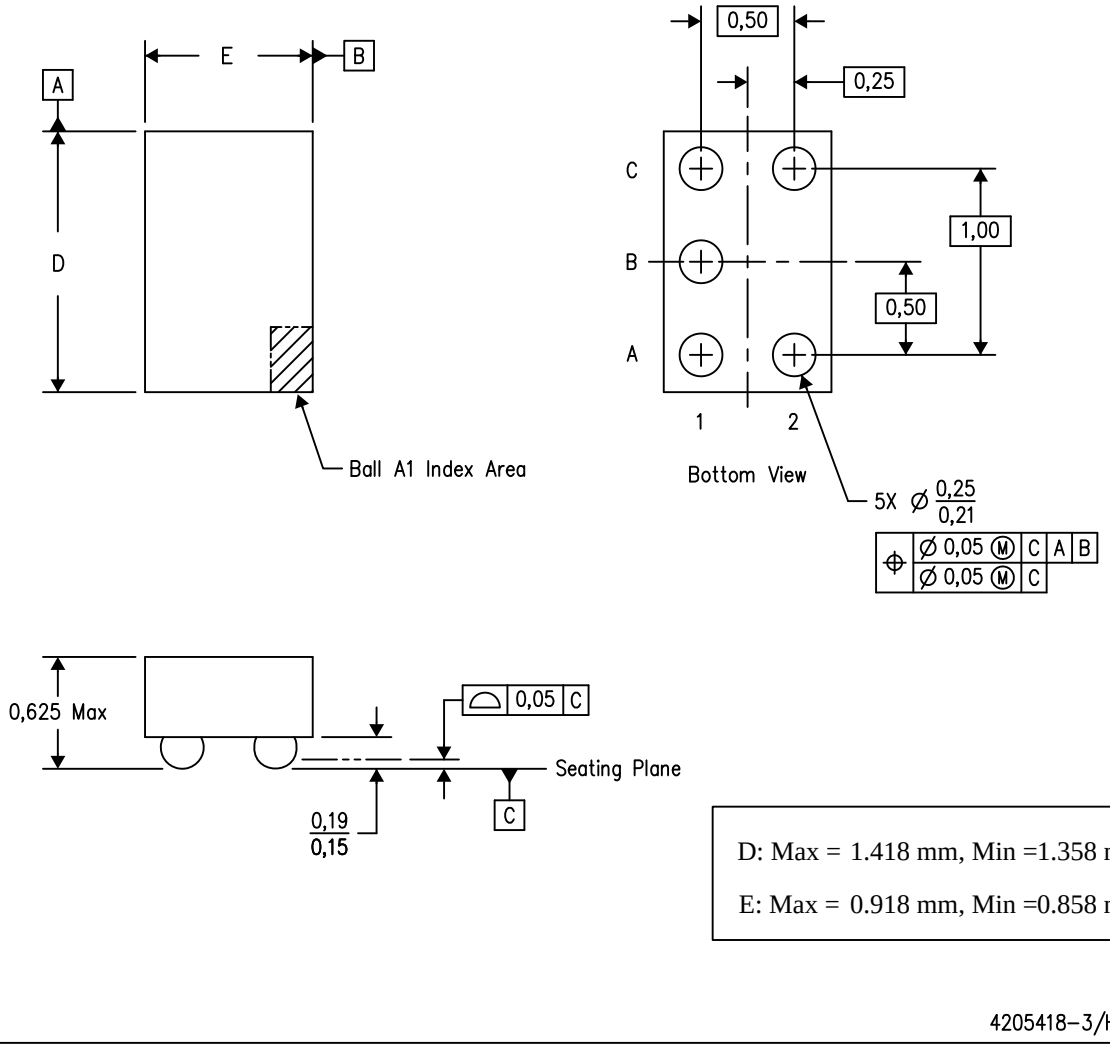
YZT (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
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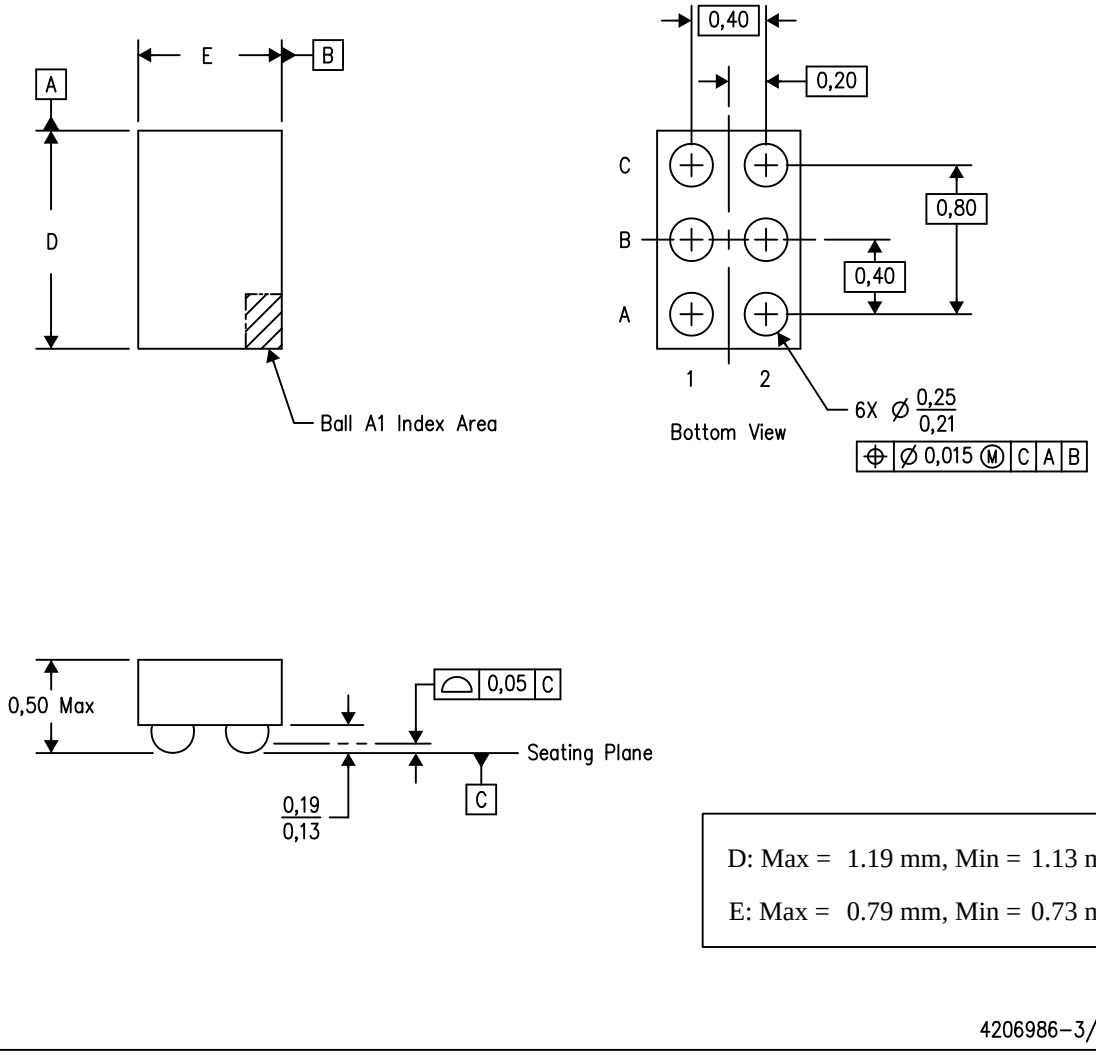
YFP (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
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