

# SN54AS877, SN74AS877 8-BIT UNIVERSAL TRANSCEIVER PORT CONTROLLERS

SDAS234 – D2661, DECEMBER 1982 – REVISED AUGUST 1985

- Package Options Include Plastic Small Outline Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Buffered 3-State Outputs Drive Bus Lines Directly
- Cascaded to n-Bits
- Eight Selectable Transceiver/Port Functions:
  - A to B or B to A
  - Register to A or Register to B
  - Shifted to A or Shifted to B
  - Off-Line Shifts (A and B Ports in High-Impedance State)
  - Register Clear
- Particularly Suitable for Use in Signature Analysis Circuitry
- Serial Register Provides:
  - Parallel Storage of Either A or B Input Data
  - Serial Transmission of Data from Either A or B Port
- Dependable Texas Instruments Quality and Reliability

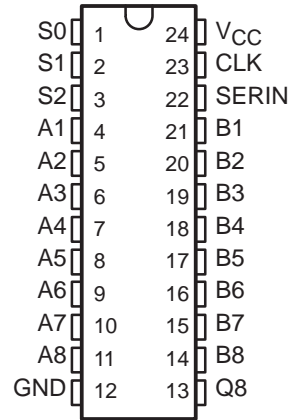
## description

The 'AS877 features two 8-bit I/O ports (A1-A8 and B1-B8), an 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three select lines S0, S1, and S2. These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), transferring data from the register to either port, serial shifting data to either port, performing off-line shifts (with A and B ports in high-impedance state), and clearing the register. Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS877 is ideally suited for applications needing signature-analysis circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

The SN54AS877 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AS877 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

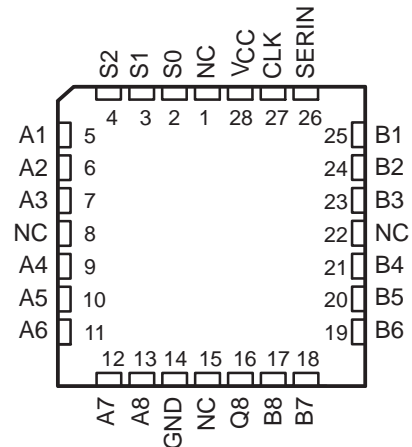
SN54AS877 . . . JT PACKAGE  
SN74AS877 . . . DW OR NT PACKAGE

(TOP VIEW)



SN54AS877 . . . JT PACKAGE  
SN74AS877 . . . DW OR NT PACKAGE

(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

MODE			CLOCK	SERIN	A1 Q1 B1			A2 Q2 B2			A3 Q3 B3			A4 Q4 B4			A5 Q5 B5			A6 Q6 B6			A7 Q7 B7			A8 Q8 B8			PORT FUNCTION	
S2	S1	S0			A1	Q1	B1	A2	Q2	B2	A3	Q3	B3	A4	Q4	B4	A5	Q5	B5	A6	Q6	B6	A7	Q7	B7	A8	Q8	B8		
L	L	L	H or L	X	Z	Q <sub>n</sub>	A1	Z	Q <sub>n</sub>	A2	Z	Q <sub>n</sub>	A3	Z	Q <sub>n</sub>	Q4	Z	Q <sub>n</sub>	A5	Z	Q <sub>n</sub>	Q6	Z	Q <sub>n</sub>	Q7	Z	Q <sub>n</sub>	A8	A To B	
L	L	L	↑	X	Z	A1	A1	Z	A2	A2	Z	A3	A3	Z	A4	Q4	Z	Q5	A5	Z	A6	Q6	Z	A7	Q7	Z	A8	A8		
L	L	H	H or L	X	B1	Q <sub>n</sub>	Z	B2	Q <sub>n</sub>	Z	B3	Q <sub>n</sub>	Z	B4	Q <sub>n</sub>	Z	B5	Q <sub>n</sub>	Z	B6	Q <sub>n</sub>	Z	B7	Q <sub>n</sub>	Z	B8	Q <sub>n</sub>	Z	B To A	
L	L	H	↑	X	B1	B1	Z	B2	B2	Z	B3	B3	Z	B4	B4	Z	B5	B5	Z	B6	B6	Z	B7	B7	Z	B8	B8	Z		
L	H	L	H or L	X	X	Q <sub>n</sub>	Q1	X	Q <sub>n</sub>	Q2	X	Q <sub>n</sub>	Q3	X	Q <sub>n</sub>	Q4	X	Q <sub>n</sub>	Q5	X	Q <sub>n</sub>	Q6	X	Q <sub>n</sub>	Q7	X	Q <sub>n</sub>	Q8	Q <sub>N</sub> To B <sub>N</sub>	
L	H	L	↑	X	Z	A1	A1	Z	A2	A2	Z	A3	A3	Z	A4	A4	Z	A5	A5	Z	A6	A6	Z	A7	A7	Z	A8	A8		
L	H	H	H or L	X	Q1	Q <sub>n</sub>	X	Q2	Q <sub>n</sub>	X	Q3	Q <sub>n</sub>	Z	Q4	Q <sub>n</sub>	Z	Q5	Q <sub>n</sub>	X	Q6	Q <sub>n</sub>	Z	Q7	Q <sub>n</sub>	Z	Q8	Q <sub>n</sub>	X	Q <sub>N</sub> To A <sub>N</sub>	
L	H	H	↑	X	B1	B1	Z	B2	B2	Z	B3	B3	Z	B4	B4	Z	B5	B5	Z	B6	B6	Z	B7	B7	Z	B8	B8	Z		
H	L	L	H or L	X	Z	Q <sub>n</sub>	Q1	Z	Q <sub>n</sub>	Q2	Q3	Q <sub>n</sub>	Q3	Z	Q <sub>n</sub>	Q4	Z	Q <sub>n</sub>	Q5	Z	Q <sub>n</sub>	Q6	Z	Q <sub>n</sub>	Q7	Z	Q <sub>n</sub>	Q8	Shift To B	
H	L	L	↑	H	Z	H	H	Z	Q1	Q1	Z	Q2	Q2	Q2	Z	Q3	Q3	Z	Q4	Q4	Z	Q5	Q5	Z	Q6	Q6	Z	Q7	Q7	
H	L	L	↑	L	Z	L	L	Z	Q1	Q1	Z	Q2	Q2	Q2	Z	Q3	Q3	Z	Q4	Q4	Z	Q5	Q5	Z	Q6	Q6	Z	Q7	Q7	
H	L	H	H or L	X	Q1	Q <sub>n</sub>	Z	Q2	Q <sub>n</sub>	Z	Q3	Q <sub>n</sub>	Z	Q4	Q <sub>n</sub>	Z	Q5	Q <sub>n</sub>	Z	Q6	Q <sub>n</sub>	Z	Q7	Q <sub>n</sub>	Z	Q8	Q <sub>n</sub>	Z	Shift To A	
H	L	H	↑	H	H	H	Z	Q1	Q1	Z	Q2	Q2	Z	Q3	Q3	Z	Q4	Q4	Z	Q5	Q5	Z	Q6	Q6	Z	Q7	Q7	Z		
H	L	H	↑	L	L	L	Z	Q1	Q1	Z	Q2	Q2	Z	Q3	Q3	Z	Q4	Q4	Z	Q5	Q5	Z	Q6	Q6	Z	Q7	Q7	Z		
H	H	L	H or L	X	Z	Q <sub>n</sub>	Z	Z	Q <sub>n</sub>	Z	Z	Q <sub>n</sub>	Z	Z	Q <sub>n</sub>	Q4	Z	Z	Q <sub>n</sub>	Z	Z	Q <sub>n</sub>	Q6	Z	Z	Q <sub>n</sub>	Q7	Z	Shift	
H	H	L	↑	H	Z	H	Z	Z	Q1	Z	Z	Q2	Z	Z	Q3	Q3	Z	Z	Q4	Z	Z	Q5	Q5	Z	Z	Q6	Q6	Z	Q7	Q7
H	H	L	↑	L	Z	L	Z	Z	Q1	Z	Z	Q2	Z	Z	Q3	Q3	Z	Z	Q4	Z	Z	Q5	Q5	Z	Z	Q6	Q6	Z	Q7	Q7
H	H	H	H or L	X	Z	Q <sub>n</sub>	Z	Z	Q <sub>n</sub>	Z	Z	Q <sub>n</sub>	Z	Z	Q <sub>n</sub>	Z	Z	Q <sub>n</sub>	Z	Z	Q <sub>n</sub>	Z	Z	Q <sub>n</sub>	Z	Z	Q <sub>n</sub>	Z	Clear	
H	H	H	↑	H	Z	H	Z	Z	L	Z	Z	L	Z	Z	L	Z	Z	L	Z	Z	L	Z	Z	L	Z	Z	L	Z		

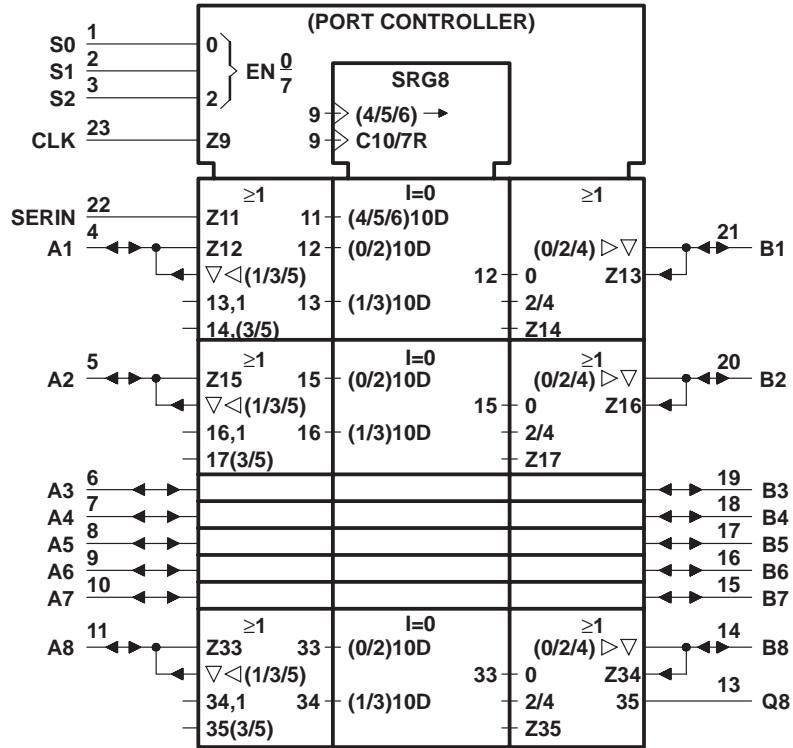
n = level Of Q<sub>n</sub>(n = 1, 2 . . . 8) established on most recent transition of CLK. Q1 thru Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

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logic symbol †



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

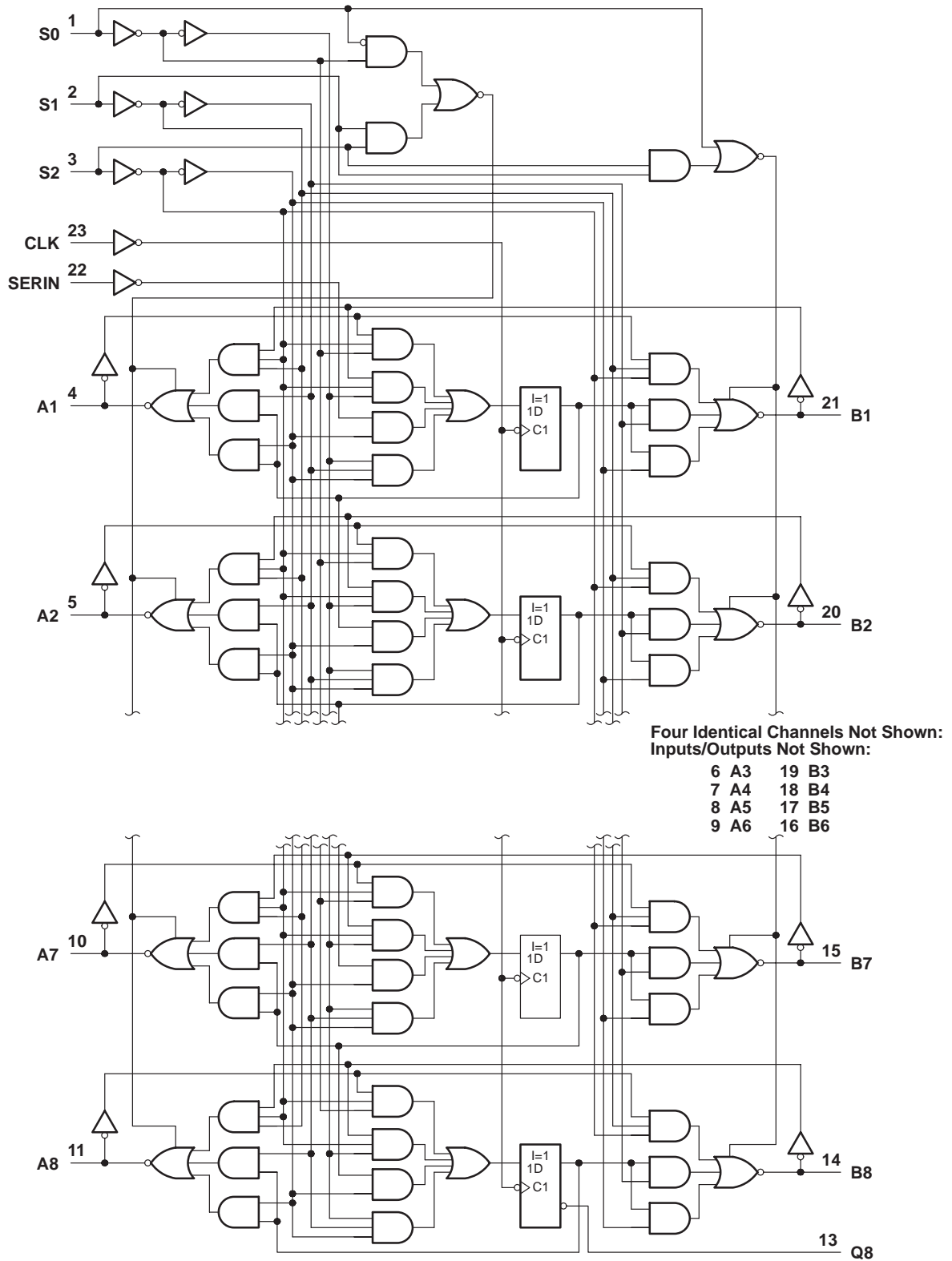


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FAMILY NAME

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## logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.



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## 8-BIT UNIVERSAL TRANCEIVER PORT CONTROLLERS

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### absolute maximum ratings over free-air temperature range

Supply voltage, $V_{CC}$ .....	7 V
Input voltage: All inputs .....	7 V
I/O ports .....	5.5 V
Voltage applied to a disabled 3-state output .....	5.5 V
Operating free-air temperature range: SN54AS877 .....	–55°C to 125°C
SN74AS877 .....	0°C to 70°C
Storage temperature range .....	–65°C to 150°C

### recommended operating conditions

		SN54AS877			SN74AS877			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{OH}$	High-level input voltage	A1-A8, B1-B8		–12	–15		mA	
		Q8		–2	–2			
$I_{OL}$	Low-level input voltage	A1-A8, B1-B8		32	48		mA	
		Q8		20	20			
$f_{clock}$	Clock frequency	0		45	0		50	MHz
$t_w$	Pulse duration, CLK	11			10			ns
$t_{su}$	Setup time before CLK↑	A1-A8, B1-B8		5.5	5.5		ns	
		SERIN						
		S0, S1, S2			5.5			
$t_h$	Hold time, data after CLK↑	A1-A8, B1-B8		0	0		ns	
		SERIN						
		S0, S1, S2			0			
$T_A$	Operating free-air temperature	–55		125	0		70	°C



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## 8-BIT UNIVERSAL TRANCEIVER PORT CONTROLLERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS877			SN74AS877			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2			-1.2	V
$V_{OH}$	A1-A8	$V_{CC} = 4.5\text{ V}$		$I_{OH} = -12\text{ mA}$	2	3.2		V
	B1-B8	$V_{CC} = 4.5\text{ V}$		$I_{OH} = -15\text{ mA}$			2 3.3	
	All outputs	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		$I_{OH} = -2\text{ mA}$	$V_{CC}-2$		$V_{CC}-2$	
$V_{OL}$	All outputs except Q8	$V_{CC} = 4.5\text{ V}$		$I_{OL} = 32\text{ mA}$	0.25	0.5		V
		$V_{CC} = 4.5\text{ V}$		$I_{OL} = 48\text{ mA}$			0.35 0.5	
	Q8	$V_{CC} = 4.5\text{ V}$		$I_{OL} = 20\text{ mA}$	0.25	0.5	0.25 0.5	
$I_I$	S0, S1, S2	$V_{CC} = 5.5\text{ V}$	$V_I = 7\text{ V}$		0.3		0.3	mA
	CLK and SERIN				0.1		0.1	
	A1-A8, B1-B8			$V_{CC} = 5.5\text{ V}$	$V_I = 5.5\text{ V}$		0.2	
$I_{IH}$	S0, S1, S2	$V_{CC} = 5.5\text{ V}$	$V_I = 2.7\text{ V}$		60		60	$\mu\text{A}$
	CLK and SERIN				20		20	
	A1-A8, B1-B8‡				70		70	
$I_{IL}$	S0, S1, S2	$V_{CC} = 5.5\text{ V}$	$V_I = 0.4\text{ V}$		-1		-1	mA
	CLK and SERIN				-0.5		-0.5	
	A1-A8, B1-B8				-0.75		-0.75	
$I_{O\S}$	Except Q8	$V_{CC} = 5.5\text{ V}$	$V_O = 2.25\text{ V}$	-30	-112	-30	-112	mA
	Q8			-20	-112	-20	-112	
$I_{CC}$	$V_{CC} = 5.5\text{ V}$			136	220	136	220	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the output currents  $I_{OZH}$  and  $I_{OZL}$ , respectively.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



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### switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX				UNIT
			SN54AS877		SN74AS877		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			45		50		MHz
t <sub>PLH</sub>	Any A port	Any B port	2	8.5	2	7	ns
t <sub>PHL</sub>			3	10.5	3	9	
t <sub>PLH</sub>	Any B port	Any A port	2	9	2	7.5	ns
t <sub>PHL</sub>			3	10.5	3	9	
t <sub>PLH</sub>	S0, S1, S2 †	Any A or B port	2	11.5	2	10	ns
t <sub>PHL</sub>			3	9.5	3	8	
t <sub>PLH</sub>	CLK	Any A or B port	2	11	2	9	ns
t <sub>PHL</sub>			3	13	3	11.5	
t <sub>PLH</sub>	CLK	QB	2	10.5	2	8	ns
t <sub>PHL</sub>			3	10	3	8.5	
t <sub>PHZ</sub>	S0, S1, S2 †	Any A or B port	2	7.5	2	6.5	ns
t <sub>PLZ</sub>			3	13	3	10.5	
t <sub>PZH</sub>			2	9	2	7	ns
t <sub>PZL</sub>			3	11.5	3	9.5	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

† The positive transition of S2 will cause low-level data at the A output Bus or stored in the shift register to be invalid for 12 ns.

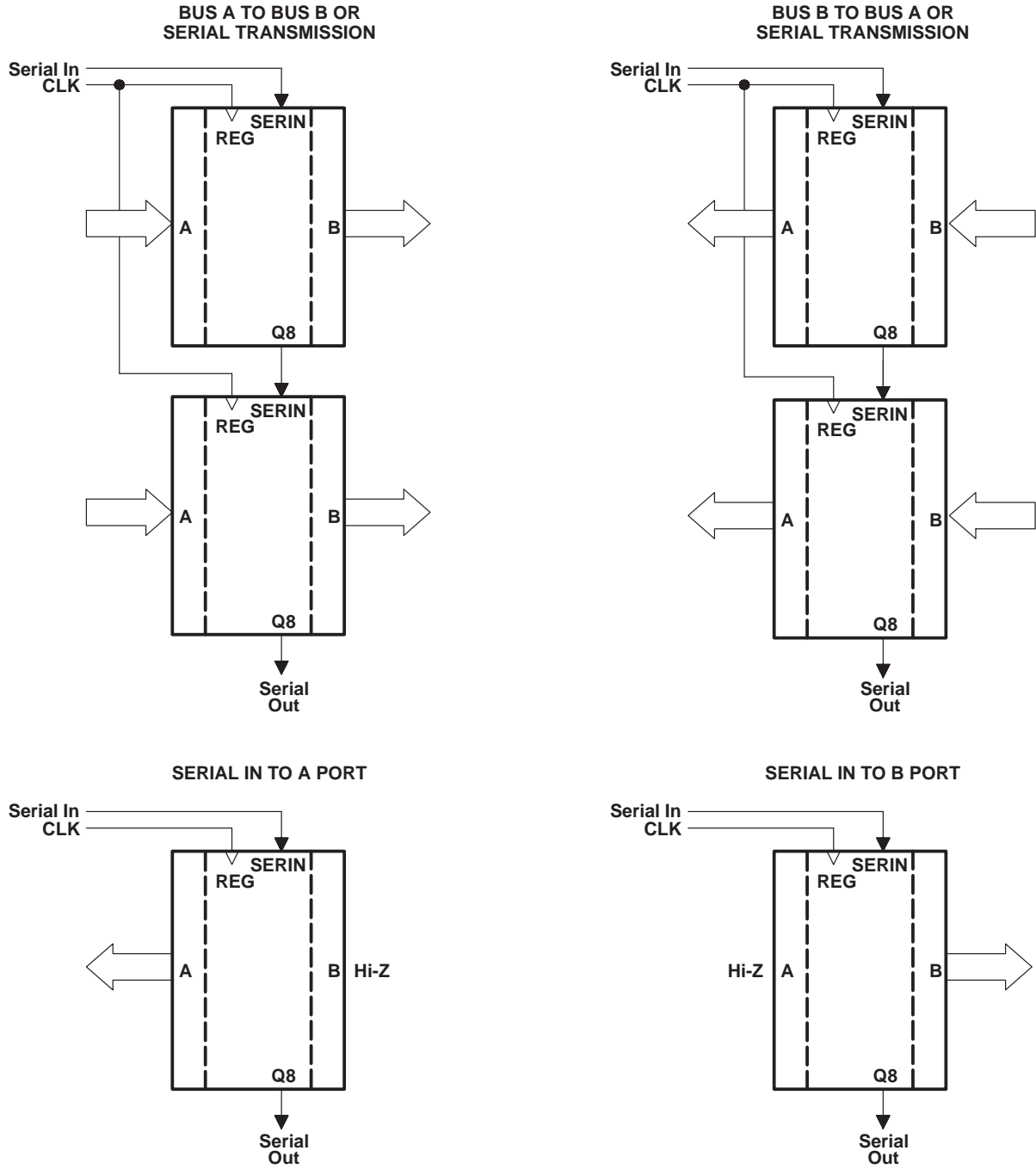


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### TYPICAL APPLICATION DATA



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