

# SN54AS821A, SN74AS821A 10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS230A – DECEMBER 1983 – REVISED AUGUST 1995

- Functionally Equivalent to AMD's AM29821
- Provide Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs to Reduce dc Loading Effects
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

## description

These 10-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

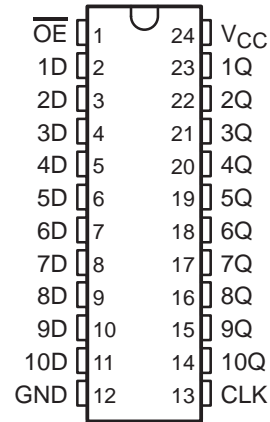
The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are true to the data (D) input.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

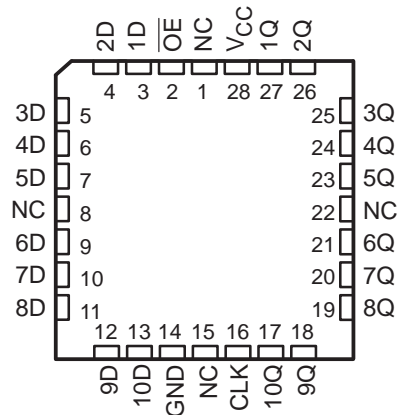
$\overline{OE}$  does not affect the internal operation of the flip-flops. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AS821A is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AS821A is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54AS821A . . . JT PACKAGE  
SN74AS821A . . . DW OR NT PACKAGE  
(TOP VIEW)



SN54AS821A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

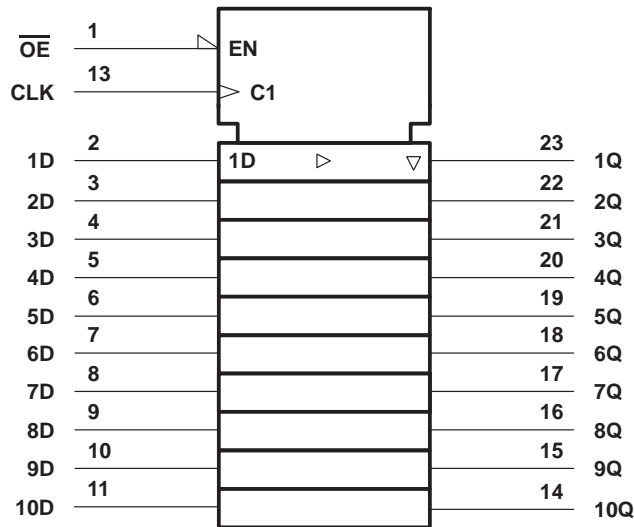
FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	L	X	$Q_0$
H	X	X	Z

# SN54AS821A, SN74AS821A 10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

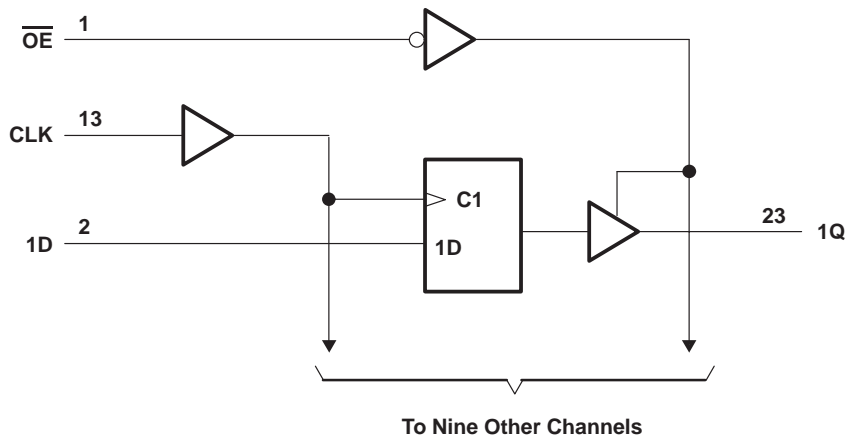
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the DW, JT, and NT packages.

## logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$ : SN54AS821A	-55°C to 125°C
SN74AS821A	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# SN54AS821A, SN74AS821A 10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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## recommended operating conditions

		SN54AS821A			SN74AS821A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{OH}$	High-level output current			-24			-24	mA
$I_{OL}$	Low-level output current			32			48	mA
$t_w^*$	Pulse duration, CLK high or low	9			8			ns
$t_{su}^*$	Setup time, data before CLK $\uparrow$	7			6			ns
$t_h^*$	Hold time, data after CLK $\uparrow$	0			0			ns
$T_A$	Operating free-air temperature	-55		125	0		70	°C

\* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS821A			SN74AS821A			UNIT
			MIN	TYP $\dagger$	MAX	MIN	TYP $\dagger$	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ ,	$I_{OH} = -2\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -15\text{ mA}$	2.4	3.2		2.4	3.2		
		$I_{OH} = -24\text{ mA}$	2			2			
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 32\text{ mA}$	0.25	0.5					V
		$I_{OL} = 48\text{ mA}$				0.35	0.5		
$I_{OZH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.7\text{ V}$			50			50	$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$			-50			-50	$\mu\text{A}$
$I_I$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 7\text{ V}$			0.1			0.1	mA
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			20			20	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$			-0.5			-0.5	mA
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.25\text{ V}$	-30		-112	-30		-112	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$	Outputs high	55	88		55	88		mA
		Outputs low	68	109		68	109		
		Outputs disabled	70	113		70	113		

$\dagger$  All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

$\ddagger$  The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

**SN54AS821A, SN74AS821A**  
**10-BIT BUS-INTERFACE FLIP-FLOPS**  
**WITH 3-STATE OUTPUTS**

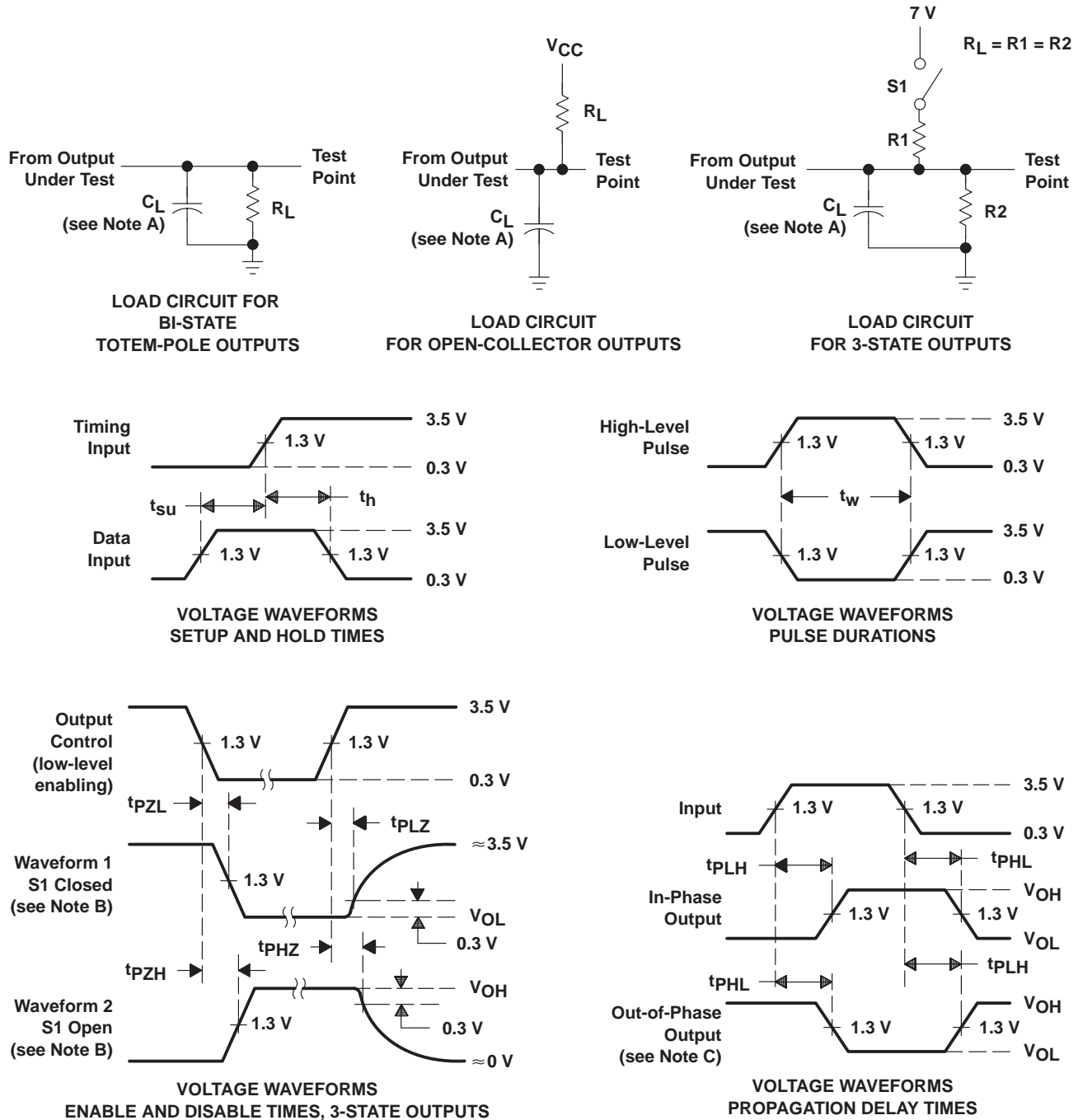
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**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>1</sub> = 500 Ω, R <sub>2</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54AS821A		SN74AS821A		
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	CLK	Any Q	3.5	9	3.5	7.5	ns
t <sub>PHL</sub>			3.5	14	3.5	13	
t <sub>PZH</sub>	$\overline{OE}$	Any Q	4	12	3	11	ns
t <sub>PZL</sub>			4	13	4	12	
t <sub>PHZ</sub>	$\overline{OE}$	Any Q	1	10	1	8	ns
t <sub>PLZ</sub>			1	10	1	8	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION  
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9078001M3A	LIFEBUY	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9078001M3A SNJ54AS 821AFK	
5962-9078001MKA	LIFEBUY	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9078001MK A SNJ54AS821AW	
5962-9078001MLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9078001ML A SNJ54AS821AJT	Samples
SN54AS821AJT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54AS821AJT	Samples
SN74AS821ADW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	0 to 70	AS821A	
SN74AS821ANT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70	SN74AS821ANT	
SNJ54AS821AFK	LIFEBUY	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9078001M3A SNJ54AS 821AFK	
SNJ54AS821AJT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9078001ML A SNJ54AS821AJT	Samples
SNJ54AS821AW	LIFEBUY	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9078001MK A SNJ54AS821AW	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54AS821A, SN74AS821A :**

● Catalog: [SN74AS821A](#)

● Military: [SN54AS821A](#)

NOTE: Qualified Version Definitions:

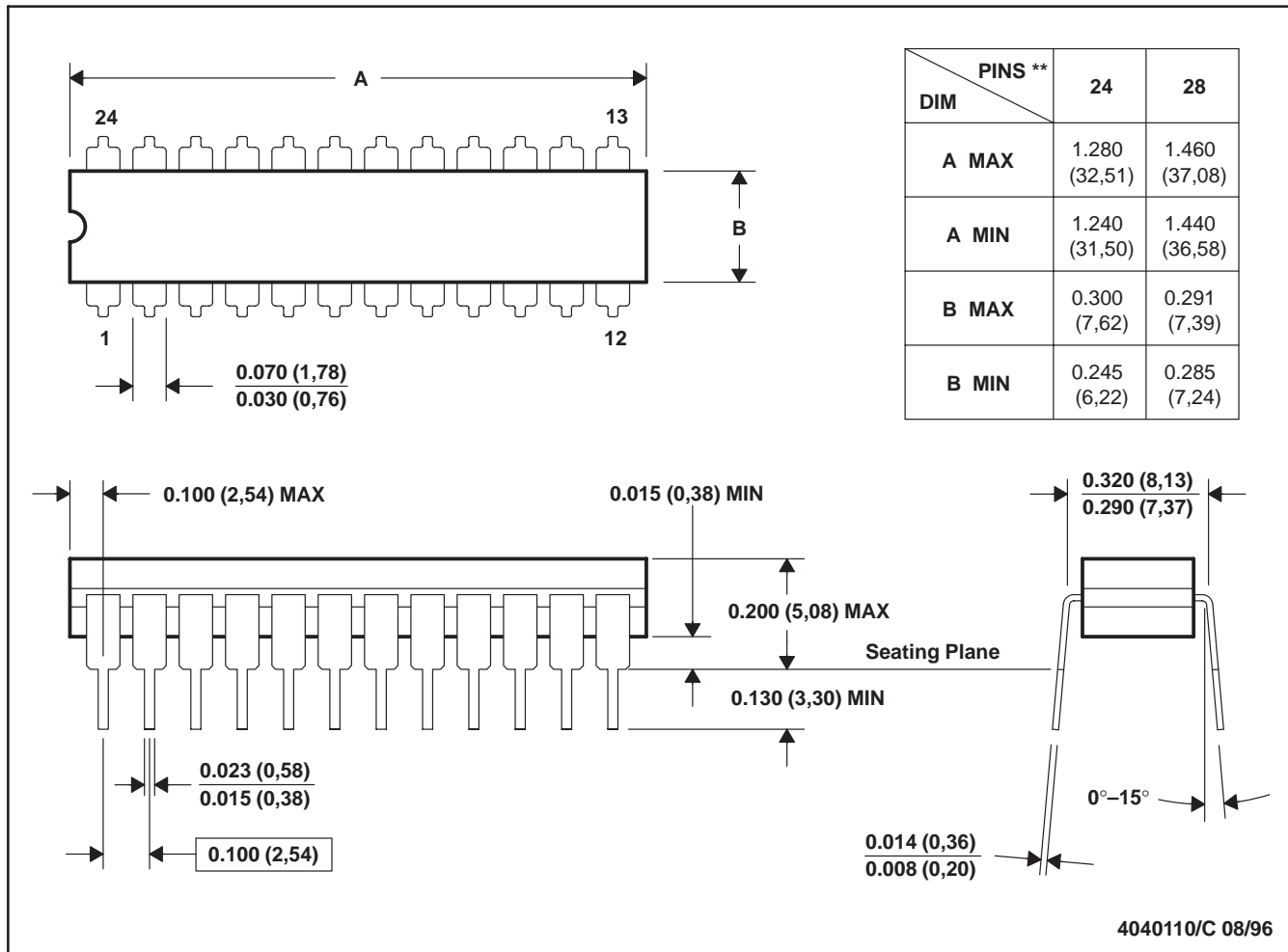
● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

JT (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE

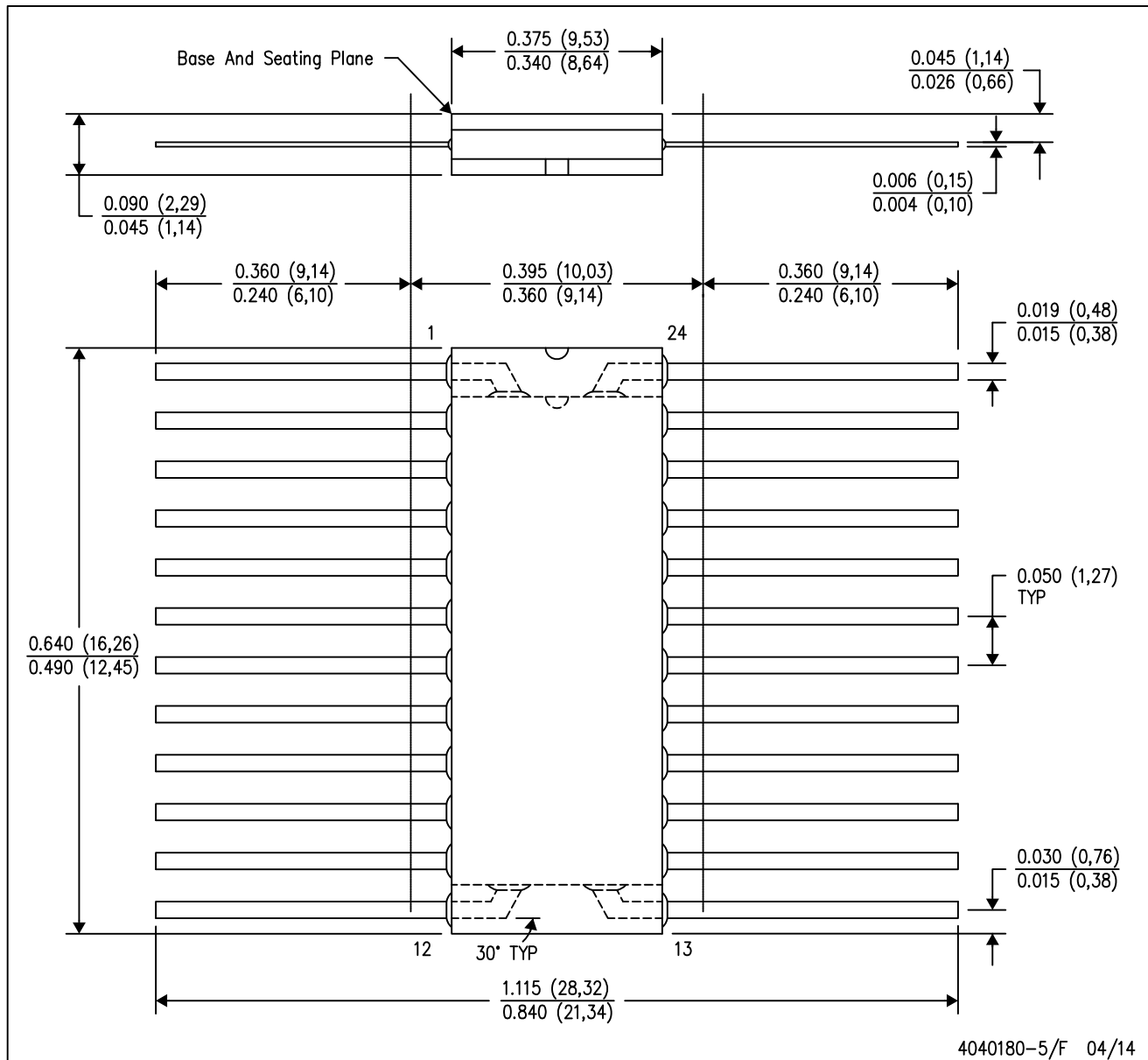
24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK

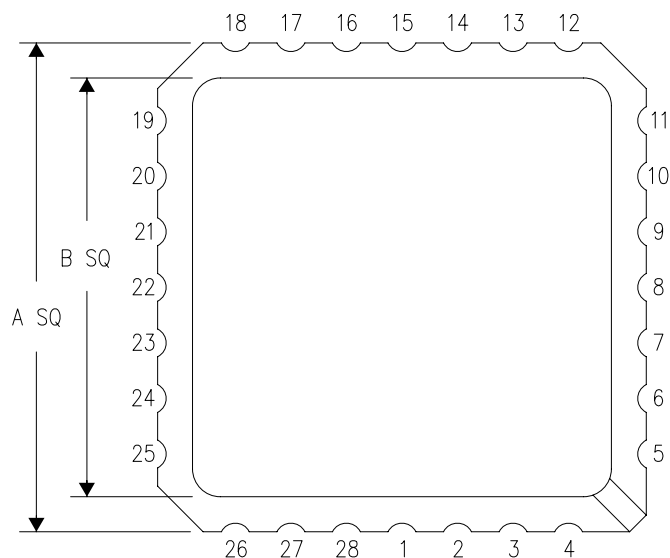


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



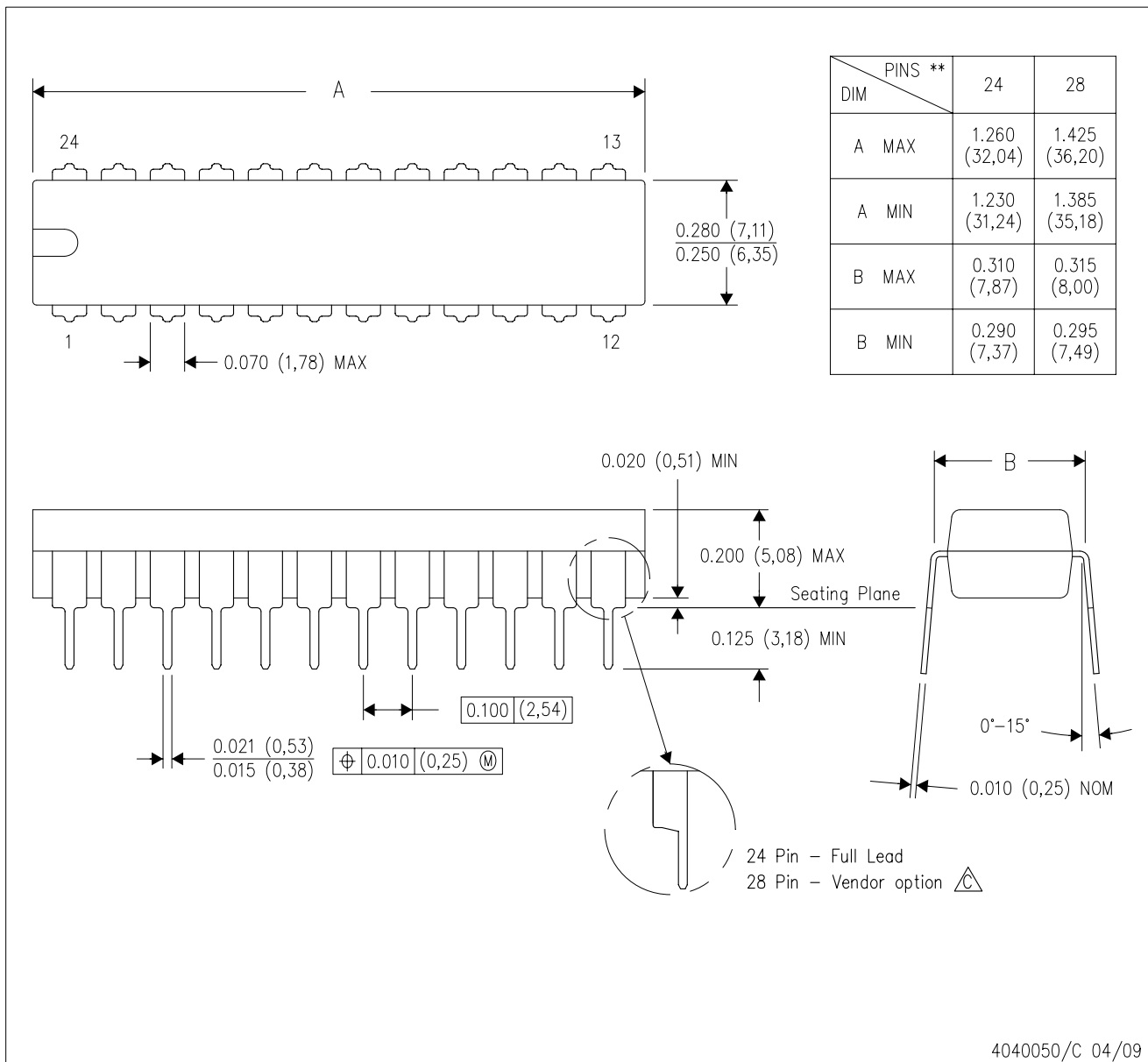
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- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NT (R-PDIP-T\*\*) 24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

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