

SN54AS756, SN74AS756, SN74AS757 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

SDAS040B – DECEMBER 1983 – REVISED JANUARY 1995

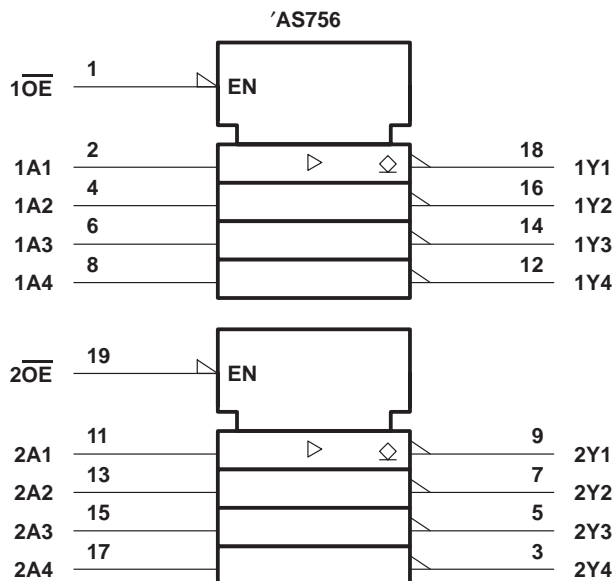
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- Eliminate the Need for 3-State Overlap Protection
- pnp Inputs Reduce dc Loading
- Open-Collector Versions of 'AS240A and 'AS241
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

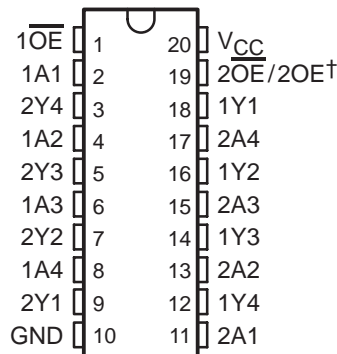
These octal buffers and line drivers are designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for 3-state overlap protection. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable (\overline{OE}) inputs, and complementary OE and \overline{OE} inputs. These devices feature high fan-out and improved fan-in.

The SN54AS756 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS756 and SN74AS757 are characterized for operation from 0°C to 70°C .

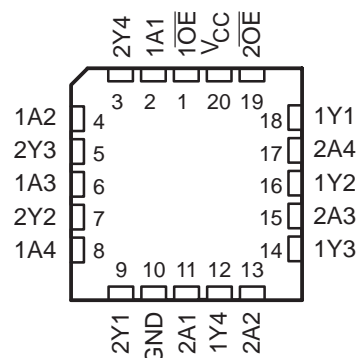
logic symbols†



SN54AS756 . . . J PACKAGE
SN74AS756, SN74AS757 . . . DW OR N PACKAGE
(TOP VIEW)



SN54AS756 . . . FK PACKAGE
(TOP VIEW)



† $\overline{2OE}$ for 'AS756 or 2OE for SN74AS757

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



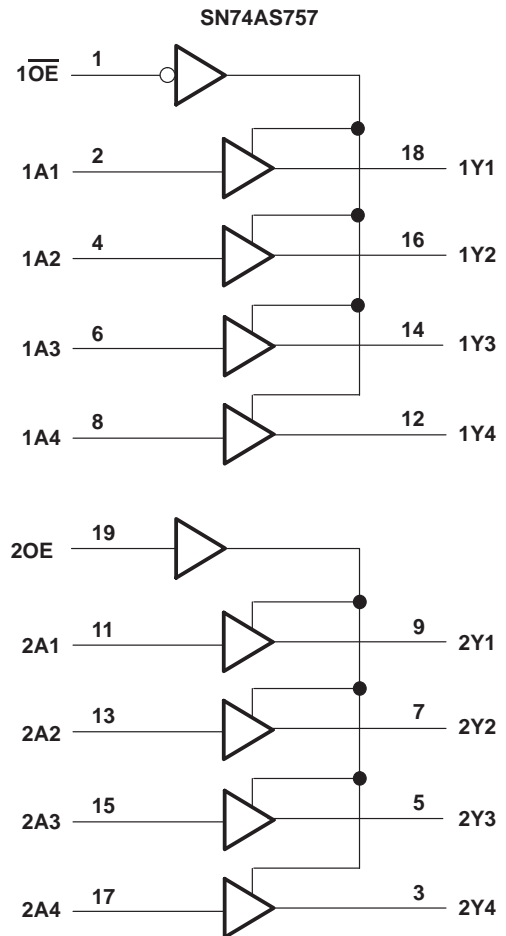
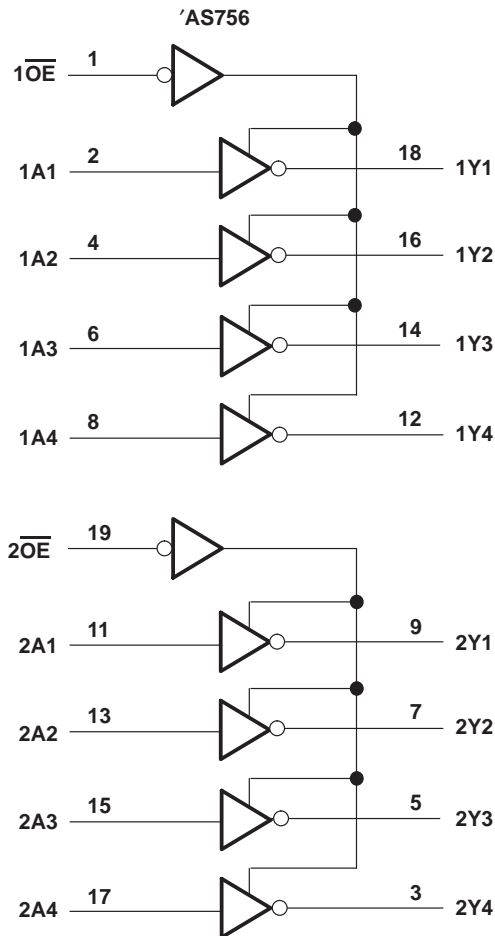
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SN54AS756, SN74AS756, SN74AS757 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

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logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Off-state output voltage | 7 V |
| Operating free-air temperature range, T_A : SN54AS756 | -55°C to 125°C |
| SN74AS756, SN74AS757 | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN54AS756, SN74AS756, SN74AS757 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

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recommended operating conditions

| | | SN54AS756 | | | SN74AS756 SN74AS757 | | | UNIT |
|----------|--------------------------------|-----------|-----|-----|------------------------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.7 | | | 0.8 | V |
| V_{OH} | High-level output voltage | | | 5.5 | | | 5.5 | V |
| I_{OL} | Low-level output current | | | 48 | | | 64 | mA |
| T_A | Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54AS756 | | SN74AS756 SN74AS757 | | UNIT | |
|-----------|-------------------------------|---------------------------|-------------------------|-----------|------|------------------------|-----|------|------|
| | | | | MIN | TYP† | MAX | MIN | | TYP† |
| V_{IK} | | $V_{CC} = 4.5\text{ V}$, | $I_I = -18\text{ mA}$ | | | -1.2 | | -1.2 | V |
| I_{OH} | | $V_{CC} = 4.5\text{ V}$, | $V_{OH} = 5.5\text{ V}$ | | | 0.1 | | 0.1 | mA |
| V_{OL} | | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 48\text{ mA}$ | | | 0.55 | | | V |
| | | | $I_{OL} = 64\text{ mA}$ | | | | | 0.55 | |
| I_I | | $V_{CC} = 5.5\text{ V}$, | $V_I = 7\text{ V}$ | | | 0.1 | | 0.1 | mA |
| I_{IH} | | $V_{CC} = 5.5\text{ V}$, | $V_I = 2.7\text{ V}$ | | | 20 | | 20 | μA |
| I_{IL} | A inputs of SN74AS757 only | $V_{CC} = 5.5\text{ V}$, | $V_I = 0.4\text{ V}$ | | | -1 | | -1 | mA |
| | All other inputs | | | | | -0.5 | | -0.5 | |
| I_{CC} | 'AS756 | $V_{CC} = 5.5\text{ V}$ | Outputs high | 9 | 15 | | 9 | 15 | mA |
| | | | Outputs low | 51 | 80 | | 51 | 80 | |
| | SN74AS757 | | Outputs high | 21 | 33 | | 21 | 33 | |
| | | | Outputs low | 61 | 95 | | 61 | 95 | |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.



SN54AS756, SN74AS756, SN74AS757 OCTAL BUFFERS AND LINE DRIVERS WITH OPEN-COLLECTOR OUTPUTS

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switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX† | | | | UNIT |
|------------------|-----------------|----------------|---|-----|-----------|------|------|
| | | | SN54AS756 | | SN74AS756 | | |
| | | | MIN | MAX | MIN | MAX | |
| t _{PLH} | A | Y | 3 | 20 | 3 | 19 | ns |
| t _{PHL} | | | 1 | 7 | 1 | 6 | |
| t _{PLH} | \overline{OE} | Y | 3 | 22 | 3 | 19.5 | ns |
| t _{PHL} | | | 1 | 8.5 | 1 | 7.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

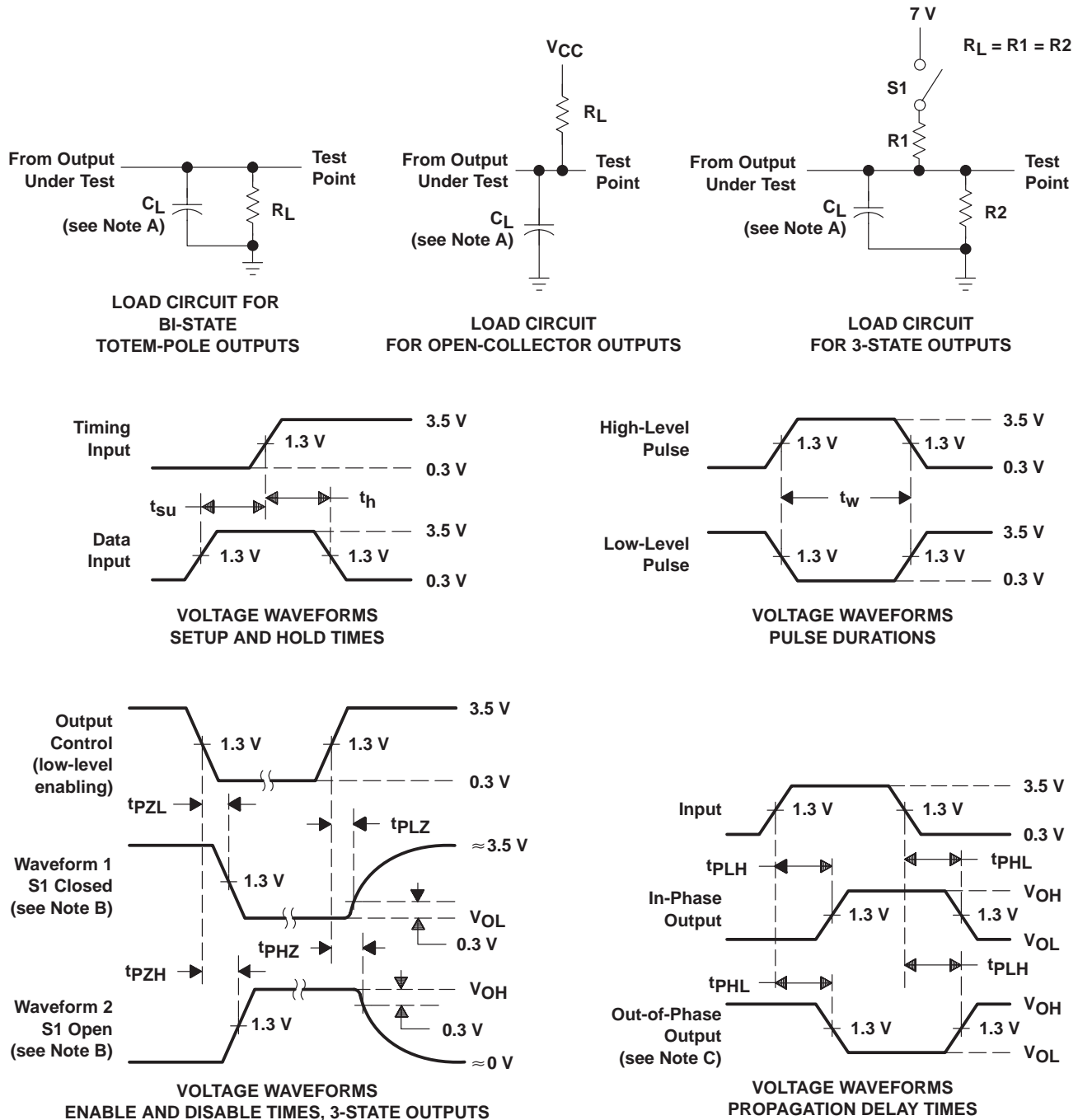
switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX† | | UNIT |
|------------------|------------------|----------------|---|------|------|
| | | | SN74AS757 | | |
| | | | MIN | MAX | |
| t _{PLH} | A | Y | 3 | 18.5 | ns |
| t _{PHL} | | | 1 | 6 | |
| t _{PLH} | $\overline{1OE}$ | 1Y | 3 | 20 | ns |
| t _{PHL} | | | 1 | 7 | |
| t _{PLH} | 2OE | 2Y | 3 | 21 | ns |
| t _{PHL} | | | 1 | 7.5 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



PARAMETER MEASUREMENT INFORMATION
 SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| 5962-90563012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Call TI | |
| 5962-9056301RA | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | Call TI | |
| 5962-9056301SA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | Call TI | |
| SN54AS756J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN74AS756DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AS756DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AS756DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AS756DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AS756DWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AS756DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AS756N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74AS756NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74AS757DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AS757DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AS757DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AS757DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AS757DWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AS757DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74AS757N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74AS757NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SNJ54AS756FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|--------------------------|
| SNJ54AS756J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54AS756W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54AS756, SN74AS756 :

● Catalog: [SN74AS756](#)

● Military: [SN54AS756](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AS756DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AS757DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AS756DWR | SOIC | DW | 20 | 2000 | 346.0 | 346.0 | 41.0 |
| SN74AS757DWR | SOIC | DW | 20 | 2000 | 346.0 | 346.0 | 41.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

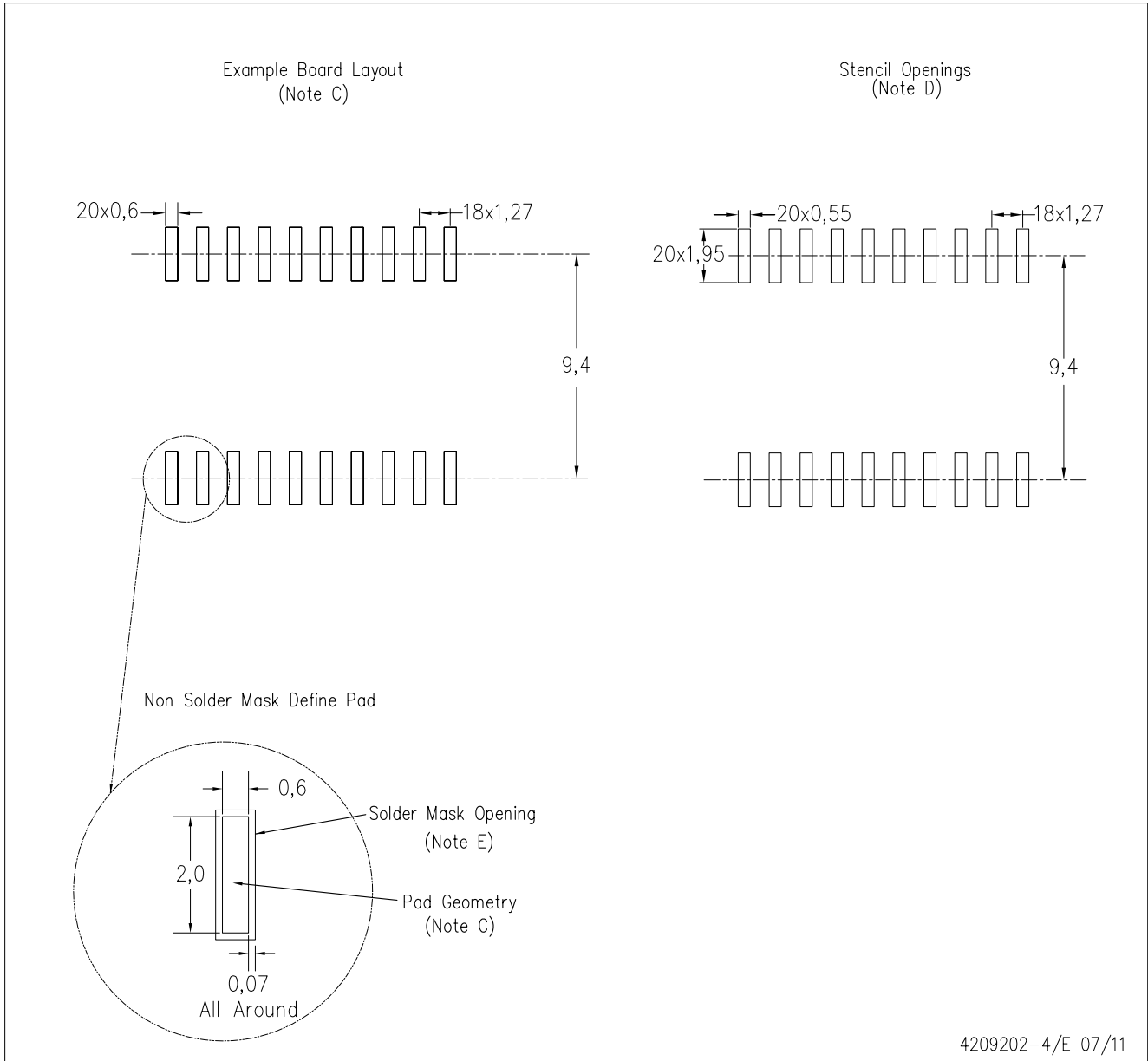
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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