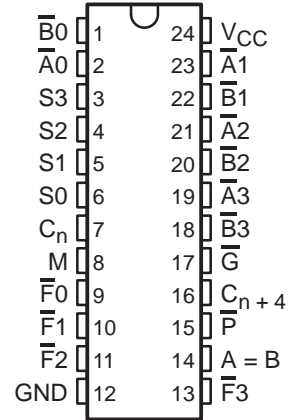


# SN54AS181B, SN74AS181A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

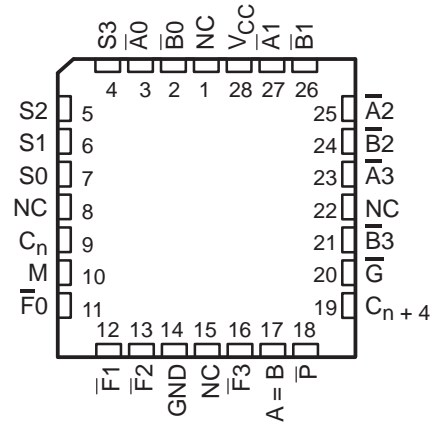
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- Full Look Ahead for High-Speed Operations on Long Words
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Twelve Other Arithmetic Operations
- Logic Function Modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
- Package Options Include Plastic Small-Outline (N) Packages, Ceramic (FK) Chip Carriers, Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs, and Ceramic (JW) 600-mil DIPs

SN54AS181B . . . JT OR JW PACKAGE  
SN74AS181A . . . N OR NT PACKAGE  
(TOP VIEW)



SN54AS181B . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description

The SN54AS181B and SN74AS181A arithmetic logic units (ALUs)/function generators have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select ( $S_0$ ,  $S_1$ ,  $S_2$ , and  $S_3$ ) lines and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries are enabled by applying a low-level voltage to the mode-control ( $M$ ) input. A full carry look-ahead scheme is used to generate fast, simultaneous carry by means of two cascade ( $\bar{G}$  and  $\bar{P}$ ) outputs for the four bits in the package.

If high speed is not important, a ripple-carry ( $C_n$ ) input and a ripple-carry ( $C_{n+4}$ ) output are available. The ripple-carry delay is minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The SN54AS181B and SN74AS181A accommodate active-high or active-low data if the pin designations are interpreted as follows:

| PIN NUMBER                 | 2          | 1          | 23         | 22         | 21         | 20         | 19         | 18         | 9          | 10         | 11         | 13         | 7           | 16              | 15        | 17        |
|----------------------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|-------------|-----------------|-----------|-----------|
| Active-low data (Table 1)  | $\bar{A}0$ | $\bar{B}0$ | $\bar{A}1$ | $\bar{B}1$ | $\bar{A}2$ | $\bar{B}2$ | $\bar{A}3$ | $\bar{B}3$ | $\bar{F}0$ | $\bar{F}1$ | $\bar{F}2$ | $\bar{F}3$ | $C_n$       | $C_{n+4}$       | $\bar{P}$ | $\bar{G}$ |
| Active-high data (Table 2) | A0         | B0         | A1         | B1         | A2         | B2         | A3         | B3         | F0         | F1         | F2         | F3         | $\bar{C}_n$ | $\bar{C}_{n+4}$ | X         | Y         |

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is  $A-B-1$ , which requires an end-around or forced carry to provide  $A-B$ .

# SN54AS181B, SN74AS181A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

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## description (continued)

The SN54AS181B and SN74AS181A also can be used as comparators. The  $A = B$  output is internally decoded from the function (F0, F1, F2, F3) outputs so that when two words of equal magnitude are applied at the A and B inputs, the output assumes a high level to indicate equality ( $A = B$ ). The ALU must be in the subtract mode with  $C_n = H$  when performing this comparison. The  $A = B$  output is open collector so that it can be wire-AND connected to give a comparison for more than four bits.  $C_{n+4}$  also can be used to supply relative magnitude information. The ALU must be placed in the subtract mode by placing the function-select inputs S3, S2, S1, and S0 at L, H, H, and L, respectively.

| INPUT<br>$C_n$ | OUTPUT<br>$C_{n+4}$ | ACTIVE-LOW DATA<br>(Figure 1) | ACTIVE-HIGH DATA<br>(Figure 2) |
|----------------|---------------------|-------------------------------|--------------------------------|
| H              | H                   | $A \geq B$                    | $A \leq B$                     |
| H              | L                   | $A < B$                       | $A > B$                        |
| L              | H                   | $A > B$                       | $A < B$                        |
| L              | L                   | $A \leq B$                    | $A \geq B$                     |

These circuits not only incorporate all of the designer's requirements for arithmetic operations, but also provide 16 possible functions of two Boolean variables without using external circuitry. These logic functions are selected by the four function-select inputs with M at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

TYPICAL ADDITION TIME  
( $C_L = 15 \text{ pF}$ ,  $R_L = 280 \Omega$ ,  $T_A = 25^\circ\text{C}$ )

| NUMBER OF BITS | ADDITION TIME USING 'S181 AND 'S182 | PACKAGE COUNT |                             | CARRY METHOD BETWEEN ALUs |
|----------------|-------------------------------------|---------------|-----------------------------|---------------------------|
|                |                                     | ALUs          | LOOK-AHEAD CARRY GENERATORS |                           |
| 1 to 4         | 11 ns                               | 1             |                             | None                      |
| 5 to 8         | 18 ns                               | 2             |                             | Ripple                    |
| 9 to 16        | 19 ns                               | 3 or 4        | 1                           | Full look ahead           |
| 17 to 64       | 28 ns                               | 5 to 16       | 2 to 5                      | Full look ahead           |

The SN54AS181B is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74AS181A is characterized for operation from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ .

## application note

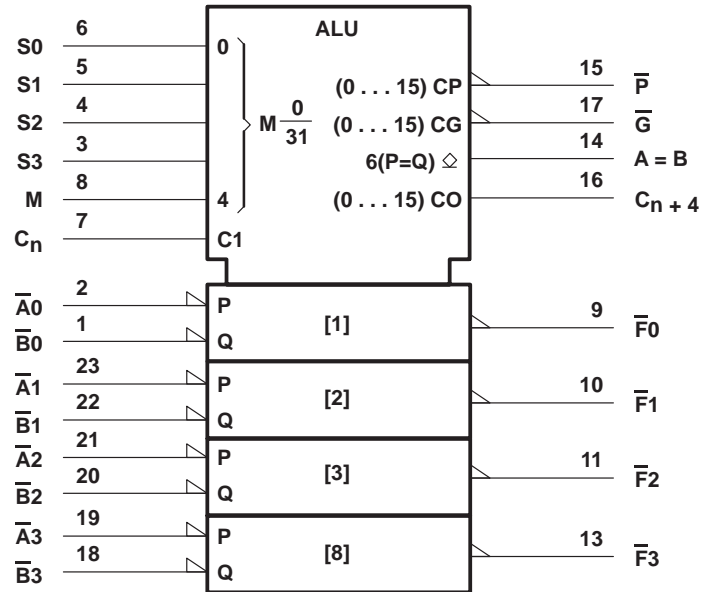
An application-specific problem has been identified in the SN54AS181B device. The F0–F4 outputs exhibit voltage transients when one or more B-data inputs transition from a high to a low state. The resultant voltage transients can have an amplitude of 2 V relative to  $V_{OL}$  with a width of 5 ns at an input threshold of 1.5 V. The transient pulse occurs coincidentally with the high-to-low transition of the B-data input(s) and appears to be caused by internal coupling.

In system operations in which this device is used, it is likely that transmission-line effects minimize this anomaly. Narrow width of the voltage transient makes the pulse transparent to most circuitry; however, in certain applications, the transients can cause system errors.

# SN54AS181B, SN74AS181A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

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logic symbol†

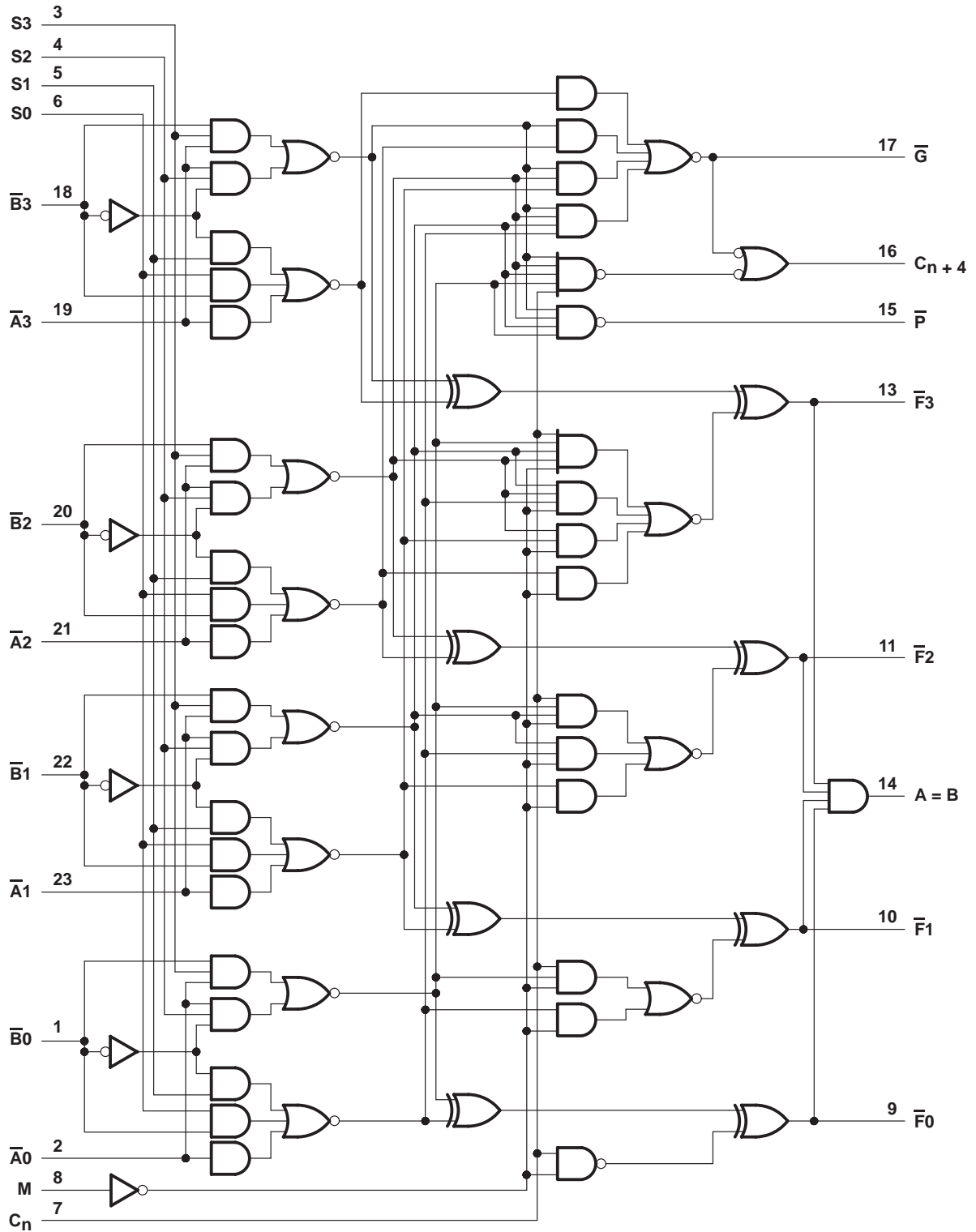


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the JT, JW, N, and NT packages.

# SN54AS181B, SN74AS181A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

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## logic diagram



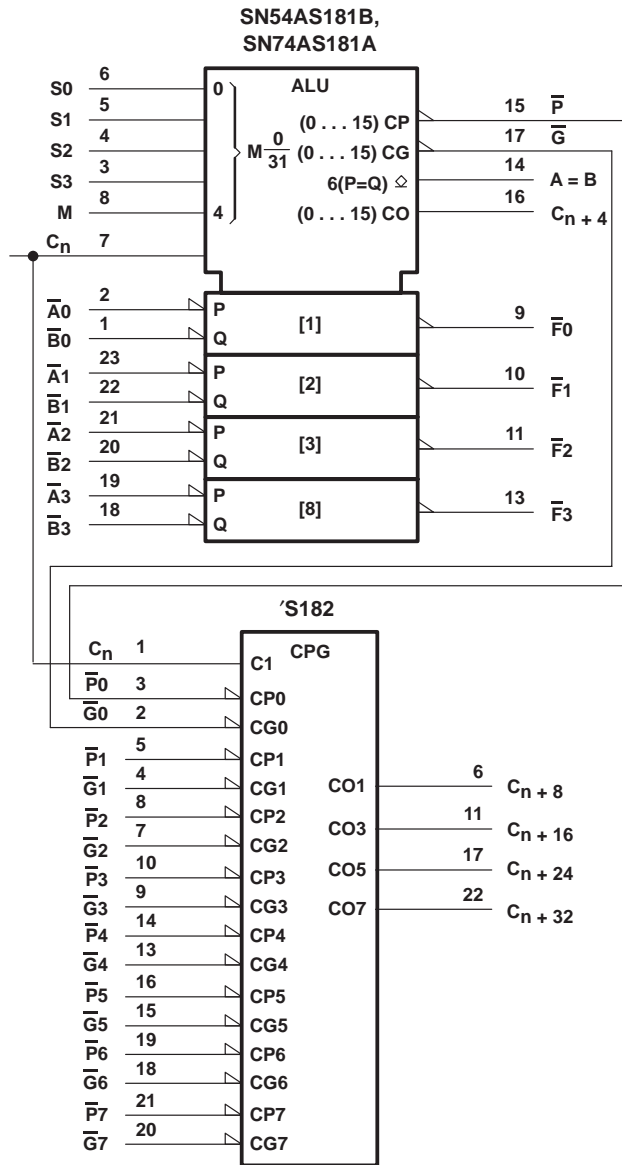
Pin numbers shown are for the JT, JW, N, and NT packages.

# SN54AS181B, SN74AS181A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

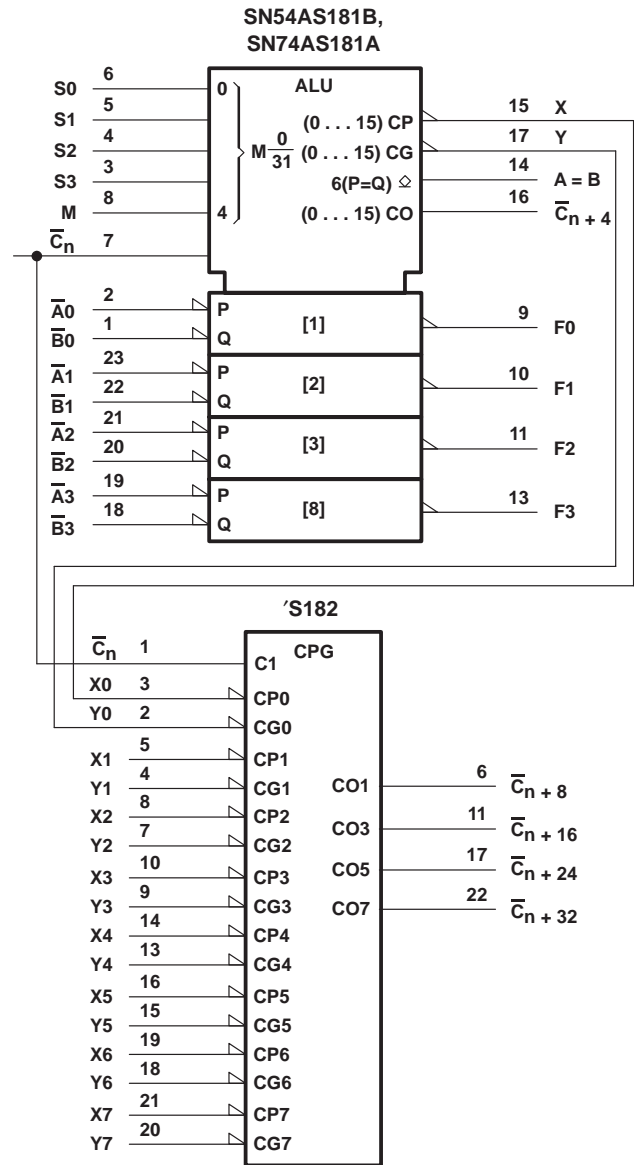
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## signal designations

In Figures 1 and 2, the polarity indicators ( $\triangle$ ) indicate that the associated input or output is active low with respect to the function shown inside the symbol. The symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The SN54AS181B and SN74AS181A together with the 'S182 can be used with the signal designation of either Figure 1 or Figure 2.



**Figure 1**  
(use with Table 1)



**Figure 2**  
(use with Table 2)

# SN54AS181B, SN74AS181A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

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Table 1

| SELECTION |    |    |    |                             | ACTIVE-LOW DATA                  |   |  |
|-----------|----|----|----|-----------------------------|----------------------------------|---|--|
| S3        | S2 | S1 | S0 | M = H<br>LOGIC<br>FUNCTIONS | M = L; ARITHMETIC OPERATIONS     |   |  |
|           |    |    |    |                             | C <sub>n</sub> = L<br>(no carry) | C <sub>n</sub> = H<br>(with carry)      |  |
| L         | L  | L  | L  | $F = \bar{A}$               | F = A MINUS 1                    | F = A                                   |  |
| L         | L  | L  | H  | $F = \overline{AB}$         | F = AB MINUS 1                   | F = AB                                  |  |
| L         | L  | H  | L  | $F = \bar{A} + B$           | F = $\overline{AB}$ MINUS 1      | F = $\overline{AB}$                     |  |
| L         | L  | H  | H  | F = 1                       | F = MINUS 1 (2's COMP)           | F = ZERO                                |  |
| L         | H  | L  | L  | $F = \overline{A + B}$      | F = A PLUS (A + $\bar{B}$ )      | F = A PLUS (A + $\bar{B}$ ) PLUS 1      |  |
| L         | H  | L  | H  | $F = \bar{B}$               | F = AB PLUS (A + $\bar{B}$ )     | F = AB PLUS (A + $\bar{B}$ ) PLUS 1     |  |
| L         | H  | H  | L  | $F = \overline{A \oplus B}$ | F = A MINUS B MINUS 1            | F = A MINUS B                           |  |
| L         | H  | H  | H  | $F = A + \bar{B}$           | F = A + $\bar{B}$                | F = (A + $\bar{B}$ ) PLUS 1             |  |
| H         | L  | L  | L  | $F = \overline{AB}$         | F = A PLUS (A + B)               | F = A PLUS (A + B) PLUS 1               |  |
| H         | L  | L  | H  | $F = A \oplus B$            | F = A PLUS B                     | F = A PLUS B PLUS 1                     |  |
| H         | L  | H  | L  | F = B                       | F = $\overline{AB}$ PLUS (A + B) | F = $\overline{AB}$ PLUS (A + B) PLUS 1 |  |
| H         | L  | H  | H  | $F = A + B$                 | F = (A + B)                      | F = (A + B) PLUS 1                      |  |
| H         | H  | L  | L  | F = 0                       | F = A PLUS A <sup>†</sup>        | F = A PLUS A PLUS 1                     |  |
| H         | H  | L  | H  | $F = \overline{AB}$         | F = AB PLUS A                    | F = AB PLUS A PLUS 1                    |  |
| H         | H  | H  | L  | F = AB                      | F = $\overline{AB}$ PLUS A       | F = $\overline{AB}$ PLUS A PLUS 1       |  |
| H         | H  | H  | H  | F = A                       | F = A PLUS 1                     | F = A PLUS 1                            |  |

<sup>†</sup> Each bit is shifted to the next more significant position.

Table 2

| SELECTION |    |    |    |                             | ACTIVE-HIGH DATA                 |   |  |
|-----------|----|----|----|-----------------------------|----------------------------------|---|--|
| S3        | S2 | S1 | S0 | M = H<br>LOGIC<br>FUNCTIONS | M = L; ARITHMETIC OPERATIONS     |   |  |
|           |    |    |    |                             | C <sub>n</sub> = H<br>(no carry) | C <sub>n</sub> = L<br>(with carry)      |  |
| L         | L  | L  | L  | $F = \bar{A}$               | F = A                            | F = A PLUS 1                            |  |
| L         | L  | L  | H  | $F = \overline{A + B}$      | F = A + B                        | F = (A + B) PLUS 1                      |  |
| L         | L  | H  | L  | $F = \overline{AB}$         | F = A + $\bar{B}$                | F = (A + $\bar{B}$ ) PLUS 1             |  |
| L         | L  | H  | H  | F = 0                       | F = MINUS 1 (2's COMPL)          | F = ZERO                                |  |
| L         | H  | L  | L  | $F = \overline{AB}$         | F = A PLUS $\overline{AB}$       | F = A PLUS $\overline{AB}$ PLUS 1       |  |
| L         | H  | L  | H  | $F = \bar{B}$               | F = (A + B) PLUS $\overline{AB}$ | F = (A + B) PLUS $\overline{AB}$ PLUS 1 |  |
| L         | H  | H  | L  | $F = A \oplus B$            | F = A MINUS B MINUS 1            | F = A MINUS B                           |  |
| L         | H  | H  | H  | $F = \overline{AB}$         | F = $\overline{AB}$ MINUS 1      | F = A $\bar{B}$                         |  |
| H         | L  | L  | L  | $F = \bar{A} + B$           | F = A PLUS AB                    | F = A PLUS AB PLUS 1                    |  |
| H         | L  | L  | H  | $F = \overline{A \oplus B}$ | F = A PLUS B                     | F = A PLUS B PLUS 1                     |  |
| H         | L  | H  | L  | F = B                       | F = (A + $\bar{B}$ ) PLUS AB     | F = (A + $\bar{B}$ ) PLUS AB PLUS 1     |  |
| H         | L  | H  | H  | F = AB                      | F = AB MINUS 1                   | F = AB                                  |  |
| H         | H  | L  | L  | F = 1                       | F = A PLUS A <sup>†</sup>        | F = A PLUS A PLUS 1                     |  |
| H         | H  | L  | H  | $F = A + \bar{B}$           | F = (A + B) PLUS A               | F = (A + B) PLUS A PLUS 1               |  |
| H         | H  | H  | L  | $F = A + B$                 | F = (A + $\bar{B}$ ) PLUS A      | F = (A + $\bar{B}$ ) PLUS A PLUS 1      |  |
| H         | H  | H  | H  | F = A                       | F = A MINUS 1                    | F = A                                   |  |

<sup>†</sup> Each bit is shifted to the next more significant position.



# SN54AS181B, SN74AS181A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|  |                |
|--|----------------|
| Supply voltage, $V_{CC}$ .....                                 | 7 V            |
| Input voltage, $V_I$ .....                                     | 7 V            |
| Off-state output voltage (A = B output only) .....             | 7 V            |
| Operating free-air temperature range, $T_A$ : SN54AS181B ..... | –55°C to 125°C |
| SN74AS181A .....   | 0°C to 70°C    |
| Storage temperature range .....                                | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

|          |                                | SN54AS181B                                  |     |     | SN74AS181A |     |     | UNIT |
|----------|--------------------------------|---|-----|-----|------------|-----|-----|------|
|          |                                | MIN   | NOM | MAX | MIN        | NOM | MAX |      |
| $V_{CC}$ | Supply voltage                 | 4.5   | 5   | 5.5 | 4.5        | 5   | 5.5 | V    |
| $V_{IH}$ | High-level input voltage       | 2   |     |     | 2          |     |     | V    |
| $V_{IL}$ | Low-level input voltage        |   |     | 0.8 |            |     | 0.8 | V    |
| $V_{OH}$ | High-level output voltage      | A = B output only                           |     | 5.5 |            |     | 5.5 | V    |
| $I_{OH}$ | High-level output current      | All outputs except A = B and $\overline{G}$ |     | –2  |            |     | –2  | mA   |
|          |                                | $\overline{G}$                              |     | –3  |            |     | –3  |      |
| $I_{OL}$ | Low-level output current       | All outputs except $\overline{G}$           |     | 20  |            |     | 20  | mA   |
|          |                                | $\overline{G}$                              |     | 48  |            |     | 48  |      |
| $T_A$    | Operating free-air temperature | –55   |     | 125 | 0          |     | 70  | °C   |



# SN54AS181B, SN74AS181A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       |  | TEST CONDITIONS   |  | SN54AS181B              |      |      | SN74AS181A          |      |      | UNIT |
|-----------------|--|---|--|-------------------------|------|------|---------------------|------|------|------|
|                 |  |   |  | MIN                     | TYP† | MAX  | MIN                 | TYP† | MAX  |      |
| V <sub>IK</sub> |  | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA          |  | -1.2                    |      |      | -1.2                |      |      | V    |
| V <sub>OH</sub> | Any output except A = B                | V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -2 mA |  | V <sub>CC</sub> - 2     |      |      | V <sub>CC</sub> - 2 |      |      | V    |
|                 | $\bar{G}$                              | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA          |  | 2.4                     | 3.4  |      | 2.4                 | 3.4  |      |      |
| V <sub>OL</sub> | Any output except $\bar{G}$            | V <sub>CC</sub> = 4.5 V                                   |  | I <sub>OL</sub> = 20 mA |      |      | 0.3 0.5             |      |      | V    |
|                 | $\bar{G}$                              |   |  | I <sub>OL</sub> = 48 mA |      |      | 0.4 0.5             |      |      |      |
| I <sub>OH</sub> | A = B                                  | V <sub>CC</sub> = 4.5 V, V <sub>OH</sub> = 5.5 V          |  | 0.1                     |      |      | 0.1                 |      |      | mA   |
| I <sub>I</sub>  | M                                      | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V             |  | 0.1                     |      |      | 0.1                 |      |      | mA   |
|                 | Any $\bar{A}$ or $\bar{B}$             |   |  | 0.3                     |      |      | 0.3                 |      |      |      |
|                 | Any S                                  |   |  | 0.4                     |      |      | 0.4                 |      |      |      |
|                 | C <sub>n</sub>                         |   |  | 0.6                     |      |      | 0.6                 |      |      |      |
| I <sub>IH</sub> | M                                      | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V           |  | 20                      |      |      | 20                  |      |      | μA   |
|                 | Any $\bar{A}$ or $\bar{B}$             |   |  | 60                      |      |      | 60                  |      |      |      |
|                 | Any S                                  |   |  | 80                      |      |      | 80                  |      |      |      |
|                 | C <sub>n</sub>                         |   |  | 120                     |      |      | 120                 |      |      |      |
| I <sub>IL</sub> | M                                      | V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V           |  | -0.5                    |      |      | -2                  |      |      | mA   |
|                 | Any $\bar{A}$ or $\bar{B}$             |   |  | -1.5                    |      |      | -6                  |      |      |      |
|                 | Any S                                  |   |  | -2                      |      |      | -8                  |      |      |      |
|                 | C <sub>n</sub>                         |   |  | -3                      |      |      | -12                 |      |      |      |
| I <sub>O‡</sub> | All outputs except A = B and $\bar{G}$ | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V          |  | -30                     | -45  | -112 | -30                 | -45  | -112 | mA   |
|                 | $\bar{G}$                              |   |  | -30                     |      | -125 | -30                 |      | -125 |      |
| I <sub>CC</sub> |  | V <sub>CC</sub> = 5.5 V                                   |  | 74                      | 117  |      | 135                 | 200  | mA   |      |

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

# SN54AS181B, SN74AS181A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

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## switching characteristics (see Figure 3)

| PARAMETER        | FROM<br>(INPUT)            | TO<br>(OUTPUT)   | TEST CONDITIONS†                                   | V <sub>CC</sub> = 4.5 V to 5.5 V,<br>C <sub>L</sub> = 50 pF,<br>R <sub>L</sub> = 500 Ω,<br>T <sub>A</sub> = MIN to MAX‡ |      |            |      | UNIT |
|------------------|----------------------------|------------------|--|---|------|------------|------|------|
|                  |                            |                  |  | SN54AS181B  |      | SN74AS181A |      |      |
|                  |                            |                  |  | MIN   | MAX  | MIN        | MAX  |      |
| t <sub>PLH</sub> | C <sub>n</sub>             | C <sub>n+4</sub> |  | 3   | 9    | 2          | 9    | ns   |
| t <sub>PHL</sub> |                            |                  |  | 2   | 7    | 2          | 9    |      |
| t <sub>PLH</sub> | Any $\bar{A}$ or $\bar{B}$ | C <sub>n+4</sub> | M = 0, S1 = S2 = 0,<br>S0 = S3 = 4.5 V (SUM mode)  | 2   | 16   | 2          | 12   | ns   |
| t <sub>PHL</sub> |                            |                  |  | 2   | 14   | 2          | 12   |      |
| t <sub>PLH</sub> | Any $\bar{A}$ or $\bar{B}$ | C <sub>n+4</sub> | M = 0, S1 = S3 = 0,<br>S1 = S2 = 4.5 V (DIFF mode) | 3   | 18   | 4          | 16   | ns   |
| t <sub>PHL</sub> |                            |                  |  | 3   | 14.5 | 2          | 16   |      |
| t <sub>PLH</sub> | C <sub>n</sub>             | Any $\bar{F}$    | M = 0 (SUM or DIFF mode)                           | 3   | 10.5 | 3          | 9    | ns   |
| t <sub>PHL</sub> |                            |                  |  | 3   | 10   | 3          | 9    |      |
| t <sub>PLH</sub> | Any $\bar{A}$ or $\bar{B}$ | $\bar{G}$        | M = 0, S1 = S2 = 0,<br>S0 = S3 = 4.5 V (SUM mode)  | 3   | 9.5  | 2          | 8    | ns   |
| t <sub>PHL</sub> |                            |                  |  | 2   | 7    | 2          | 7    |      |
| t <sub>PLH</sub> | Any $\bar{A}$ or $\bar{B}$ | $\bar{G}$        | M = 0, S1 = S3 = 0,<br>S1 = S2 = 4.5 V (DIFF mode) | 3   | 12   | 2          | 9.5  | ns   |
| t <sub>PHL</sub> |                            |                  |  | 2   | 9    | 2          | 9    |      |
| t <sub>PLH</sub> | Any $\bar{A}$ or $\bar{B}$ | $\bar{P}$        | M = 0, S1 = S2 = 0,<br>S0 = S3 = 4.5 V (SUM mode)  | 3   | 9.5  | 2          | 8    | ns   |
| t <sub>PHL</sub> |                            |                  |  | 2   | 7.5  | 2          | 8    |      |
| t <sub>PLH</sub> | Any $\bar{A}$ or $\bar{B}$ | $\bar{P}$        | M = 0, S1 = S3 = 0,<br>S1 = S2 = 4.5 V (DIFF mode) | 3   | 12   | 2          | 10   | ns   |
| t <sub>PHL</sub> |                            |                  |  | 3   | 8.5  | 2          | 10   |      |
| t <sub>PLH</sub> | $\bar{A}_i$ or $\bar{B}_i$ | $\bar{F}_i$      | M = 0, S1 = S2 = 0,<br>S0 = S3 = 4.5 V (SUM mode)  | 3   | 11   | 2          | 9.5  | ns   |
| t <sub>PHL</sub> |                            |                  |  | 3   | 9    | 2          | 8    |      |
| t <sub>PLH</sub> | $\bar{A}_i$ or $\bar{B}_i$ | $\bar{F}_i$      | M = 0, S1 = S3 = 0,<br>S1 = S2 = 4.5 V (DIFF mode) | 3   | 13.5 | 2          | 10.5 | ns   |
| t <sub>PHL</sub> |                            |                  |  | 3   | 11   | 2          | 10   |      |
| t <sub>PLH</sub> | $\bar{A}_i$ or $\bar{B}_i$ | $\bar{F}_i$      | M = 4.5 V (LOGIC mode)                             | 3   | 16   | 2          | 11   | ns   |
| t <sub>PHL</sub> |                            |                  |  | 3   | 10   | 2          | 11   |      |
| t <sub>PLH</sub> | Any $\bar{A}$ or $\bar{B}$ | A = B            | M = 0, S1 = S3 = 0,<br>S1 = S2 = 4.5 V (DIFF mode) | 2   | 19   | 4          | 21   | ns   |
| t <sub>PHL</sub> |                            |                  |  | 3   | 22   | 4          | 21   |      |

† Refer to the parameter measurement information tables for the SUM-, DIFF-, and LOGIC-mode test tables.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN54AS181B, SN74AS181A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDAS209B – DECEMBER 1982 – REVISED DECEMBER 1994

## PARAMETER MEASUREMENT INFORMATION

**SUM-MODE TEST TABLE**  
(Function Inputs:  $S_0 = S_3 = 4.5\text{ V}$ ,  $S_1 = S_2 = M = 0$ )

| PARAMETER | INPUT UNDER TEST | OTHER INPUT SAME BIT |             | OTHER DATA INPUTS                 |   | OUTPUT UNDER TEST          | OUTPUT WAVEFORM (See Note 1) |
|-----------|------------------|----------------------|-------------|-----------------------------------|---|----------------------------|------------------------------|
|           |                  | APPLY 4.5 V          | APPLY GND   | APPLY 4.5 V                       | APPLY GND                                 |                            |                              |
| $t_{PLH}$ | $\bar{A}_i$      | $\bar{B}_i$          | None        | Remaining $\bar{A}$ and $\bar{B}$ | $C_n$                                     | $\bar{F}_i$                | In phase                     |
| $t_{PHL}$ |                  |                      |             |                                   |   |                            |                              |
| $t_{PLH}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | Remaining $\bar{A}$ and $\bar{B}$ | $C_n$                                     | $\bar{F}_i$                | In phase                     |
| $t_{PHL}$ |                  |                      |             |                                   |   |                            |                              |
| $t_{PLH}$ | $\bar{A}_i$      | $\bar{B}_i$          | None        | None                              | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{P}$                  | In phase                     |
| $t_{PHL}$ |                  |                      |             |                                   |   |                            |                              |
| $t_{PLH}$ | $\bar{B}_i$      | $\bar{A}_i$          | None        | None                              | Remaining $\bar{A}$ and $\bar{B}$ , $C_n$ | $\bar{P}$                  | In phase                     |
| $t_{PHL}$ |                  |                      |             |                                   |   |                            |                              |
| $t_{PLH}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{B}$               | Remaining $\bar{A}$ , $C_n$               | $\bar{G}$                  | In phase                     |
| $t_{PHL}$ |                  |                      |             |                                   |   |                            |                              |
| $t_{PLH}$ | $\bar{B}_i$      | None                 | $\bar{A}_i$ | Remaining $\bar{B}$               | Remaining $\bar{A}$ , $C_n$               | $\bar{G}$                  | In phase                     |
| $t_{PHL}$ |                  |                      |             |                                   |   |                            |                              |
| $t_{PLH}$ | $C_n$            | None                 | None        | All $\bar{A}$                     | All $\bar{B}$                             | Any $\bar{F}$ or $C_{n+4}$ | In phase                     |
| $t_{PHL}$ |                  |                      |             |                                   |   |                            |                              |
| $t_{PLH}$ | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{B}$               | Remaining $\bar{A}$ , $C_n$               | $C_{n+4}$                  | Out of phase                 |
| $t_{PHL}$ |                  |                      |             |                                   |   |                            |                              |
| $t_{PLH}$ | $\bar{B}_i$      | None                 | $\bar{A}_i$ | Remaining $\bar{B}$               | Remaining $\bar{A}$ , $C_n$               | $C_{n+4}$                  | Out of phase                 |
| $t_{PHL}$ |                  |                      |             |                                   |   |                            |                              |

**PARAMETER MEASUREMENT INFORMATION**

**DIFF-MODE TEST TABLE**  
(Function Inputs: S1 = S2 = 4.5 V, S0 = S3 = M = 0)

| PARAMETER        | INPUT UNDER TEST | OTHER INPUT SAME BIT |             | OTHER DATA INPUTS           |  | OUTPUT UNDER TEST           | OUTPUT WAVEFORM (See Note 1) |
|------------------|------------------|----------------------|-------------|-----------------------------|--|-----------------------------|------------------------------|
|                  |                  | APPLY 4.5 V          | APPLY GND   | APPLY 4.5 V                 | APPLY GND                              |                             |                              |
| t <sub>PLH</sub> | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{A}$         | Remaining $\bar{B}, C_n$               | $\bar{F}_i$                 | In phase                     |
| t <sub>PHL</sub> |                  |                      |             |                             |  |                             |                              |
| t <sub>PLH</sub> | $\bar{B}_i$      | $\bar{A}_i$          | None        | Remaining $\bar{A}$         | Remaining $\bar{B}, C_n$               | $\bar{F}_i$                 | Out of phase                 |
| t <sub>PHL</sub> |                  |                      |             |                             |  |                             |                              |
| t <sub>PLH</sub> | $\bar{A}_i$      | None                 | $\bar{B}_i$ | None                        | Remaining $\bar{A}$ and $\bar{B}, C_n$ | $\bar{P}$                   | In phase                     |
| t <sub>PHL</sub> |                  |                      |             |                             |  |                             |                              |
| t <sub>PLH</sub> | $\bar{B}_i$      | $\bar{A}_i$          | None        | None                        | Remaining $\bar{A}$ and $\bar{B}, C_n$ | $\bar{P}$                   | Out of phase                 |
| t <sub>PHL</sub> |                  |                      |             |                             |  |                             |                              |
| t <sub>PLH</sub> | $\bar{A}_i$      | $\bar{B}_i$          | None        | None                        | Remaining $\bar{A}$ and $\bar{B}, C_n$ | $\bar{G}$                   | In phase                     |
| t <sub>PHL</sub> |                  |                      |             |                             |  |                             |                              |
| t <sub>PLH</sub> | $\bar{B}_i$      | None                 | $\bar{A}_i$ | None                        | Remaining $\bar{A}$ and $\bar{B}, C_n$ | $\bar{G}$                   | Out of phase                 |
| t <sub>PHL</sub> |                  |                      |             |                             |  |                             |                              |
| t <sub>PLH</sub> | $\bar{A}_i$      | None                 | $\bar{B}_i$ | Remaining $\bar{A}$         | Remaining $\bar{B}, C_n$               | A = B                       | In phase                     |
| t <sub>PHL</sub> |                  |                      |             |                             |  |                             |                              |
| t <sub>PLH</sub> | $\bar{B}_i$      | $\bar{A}_i$          | None        | Remaining $\bar{A}$         | Remaining $\bar{B}, C_n$               | A = B                       | Out of phase                 |
| t <sub>PHL</sub> |                  |                      |             |                             |  |                             |                              |
| t <sub>PLH</sub> | C <sub>n</sub>   | None                 | None        | All $\bar{A}$ and $\bar{B}$ | None                                   | C <sub>n</sub> + 4 or any F | In phase                     |
| t <sub>PHL</sub> |                  |                      |             |                             |  |                             |                              |
| t <sub>PLH</sub> | $\bar{A}_i$      | $\bar{B}_i$          | None        | None                        | Remaining $\bar{A}, \bar{B}, C_n$      | C <sub>n</sub> + 4          | Out of phase                 |
| t <sub>PHL</sub> |                  |                      |             |                             |  |                             |                              |
| t <sub>PLH</sub> | $\bar{B}_i$      | None                 | $\bar{A}_i$ | None                        | Remaining $\bar{A}, \bar{B}, C_n$      | C <sub>n</sub> + 4          | In phase                     |
| t <sub>PHL</sub> |                  |                      |             |                             |  |                             |                              |

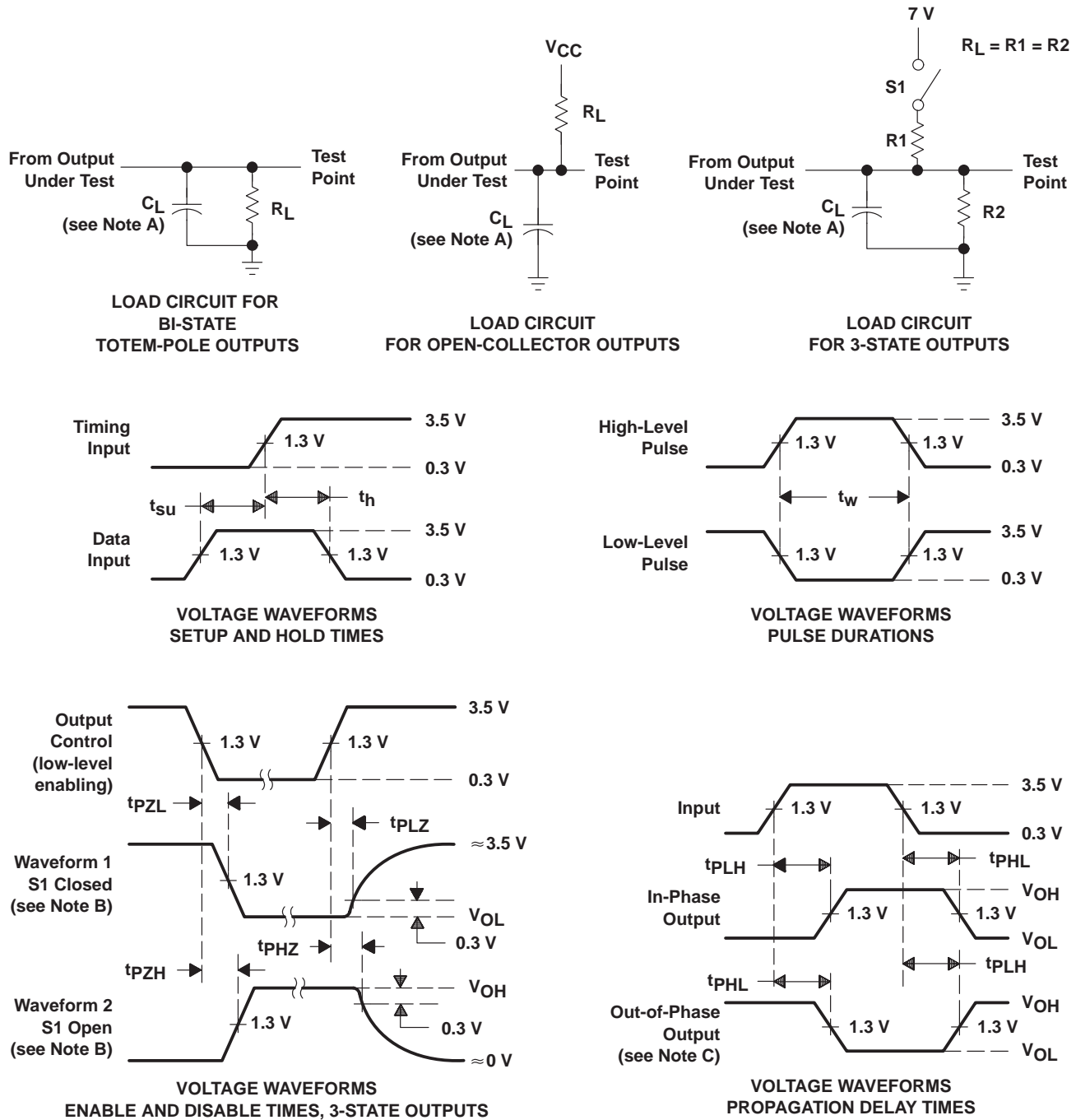
**LOGIC-MODE TEST TABLE**  
(Function Inputs: S1 = S2 = M = 4.5 V, S0 = S3 = 0)

| PARAMETER        | INPUT UNDER TEST | OTHER INPUT SAME BIT |           | OTHER DATA INPUTS |  | OUTPUT UNDER TEST | OUTPUT WAVEFORM (See Note 1) |
|------------------|------------------|----------------------|-----------|-------------------|--|-------------------|------------------------------|
|                  |                  | APPLY 4.5 V          | APPLY GND | APPLY GND         | APPLY 4.5 V                            |                   |                              |
| t <sub>PLH</sub> | $\bar{A}_i$      | $\bar{B}_i$          | None      | None              | Remaining $\bar{A}$ and $\bar{B}, C_n$ | $\bar{F}_i$       | Out of phase                 |
| t <sub>PHL</sub> |                  |                      |           |                   |  |                   |                              |
| t <sub>PLH</sub> | $\bar{B}_i$      | $\bar{A}_i$          | None      | None              | Remaining $\bar{A}$ and $\bar{B}, C_n$ | $\bar{F}_i$       | Out of phase                 |
| t <sub>PHL</sub> |                  |                      |           |                   |  |                   |                              |

# SN54AS181B, SN74AS181A ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

SDAS209B – DECEMBER 1982 – REVISED DECEMBER 1994

## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN54AS181BJT     | OBSOLETE              | CDIP         | JT              | 24   |             | TBD                     | Call TI          | Call TI                      |
| SN74AS181ADW     | ACTIVE                | SOIC         | DW              | 24   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AS181ADWE4   | ACTIVE                | SOIC         | DW              | 24   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AS181ADWG4   | ACTIVE                | SOIC         | DW              | 24   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AS181ADWR    | ACTIVE                | SOIC         | DW              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AS181ADWRE4  | ACTIVE                | SOIC         | DW              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AS181ADWRG4  | ACTIVE                | SOIC         | DW              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74AS181AN      | OBSOLETE              | PDIP         | N               | 24   |             | TBD                     | Call TI          | Call TI                      |
| SN74AS181ANT     | ACTIVE                | PDIP         | NT              | 24   | 15          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN74AS181ANTE4   | ACTIVE                | PDIP         | NT              | 24   | 15          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SNJ54AS181BFK    | OBSOLETE              | LCCC         | FK              | 28   |             | TBD                     | Call TI          | Call TI                      |
| SNJ54AS181BJT    | OBSOLETE              | CDIP         | JT              | 24   |             | TBD                     | Call TI          | Call TI                      |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AS181ADWR | SOIC         | DW              | 24   | 2000 | 330.0              | 24.4               | 10.75   | 15.7    | 2.7     | 12.0    | 24.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**

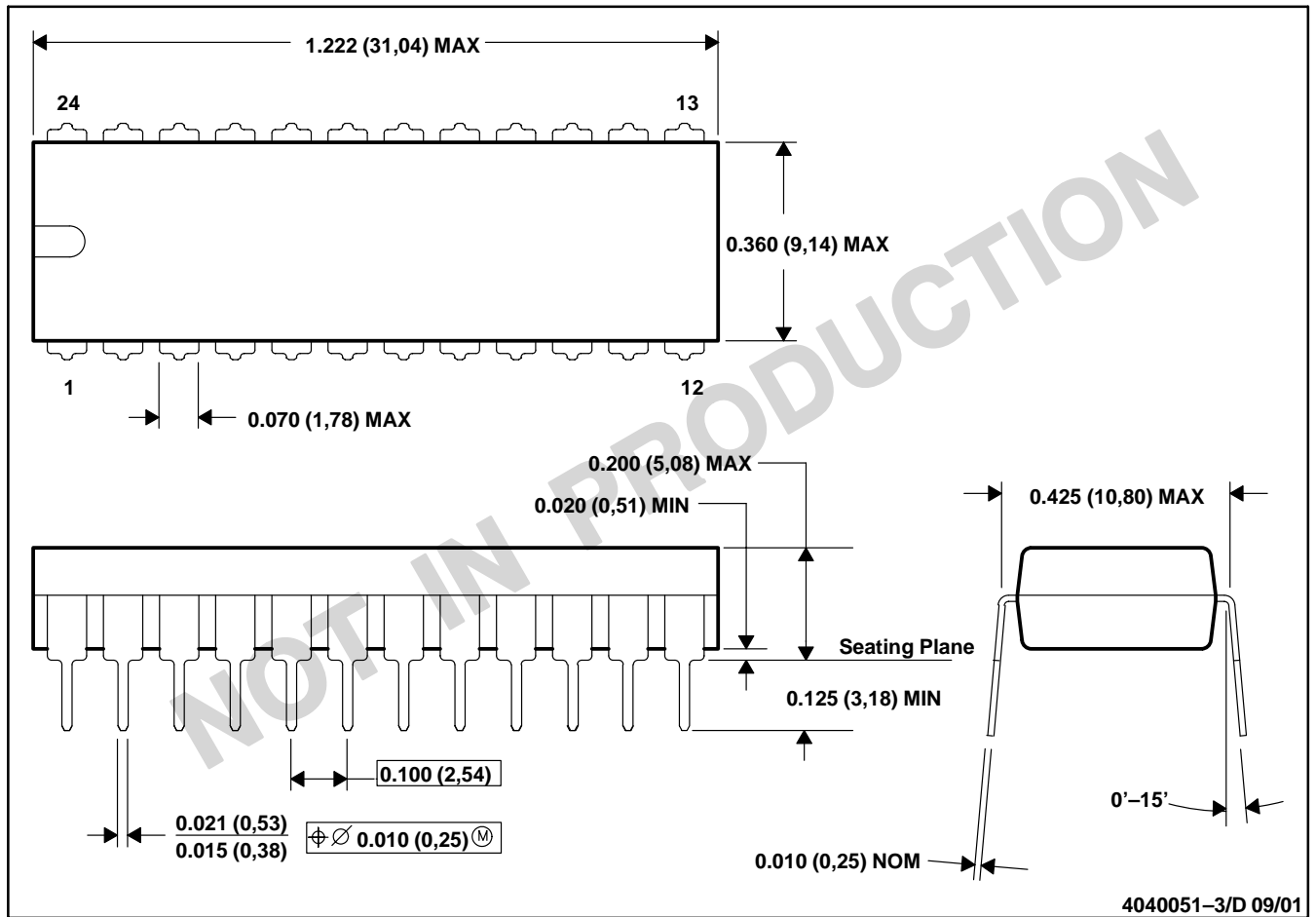


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AS181ADWR | SOIC         | DW              | 24   | 2000 | 346.0       | 346.0      | 41.0        |

N (R-PDIP-T24)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-010

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



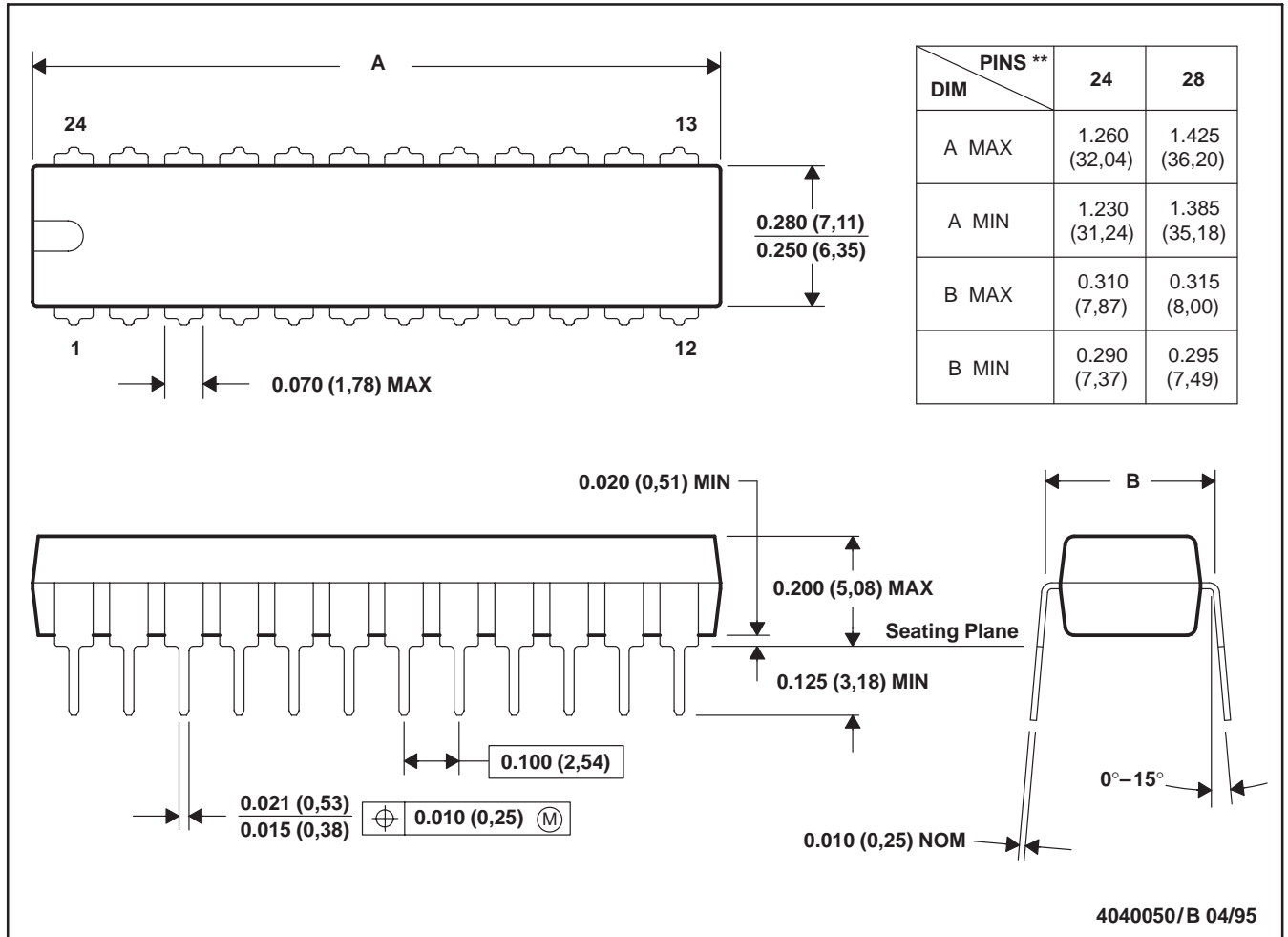
4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

NT (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

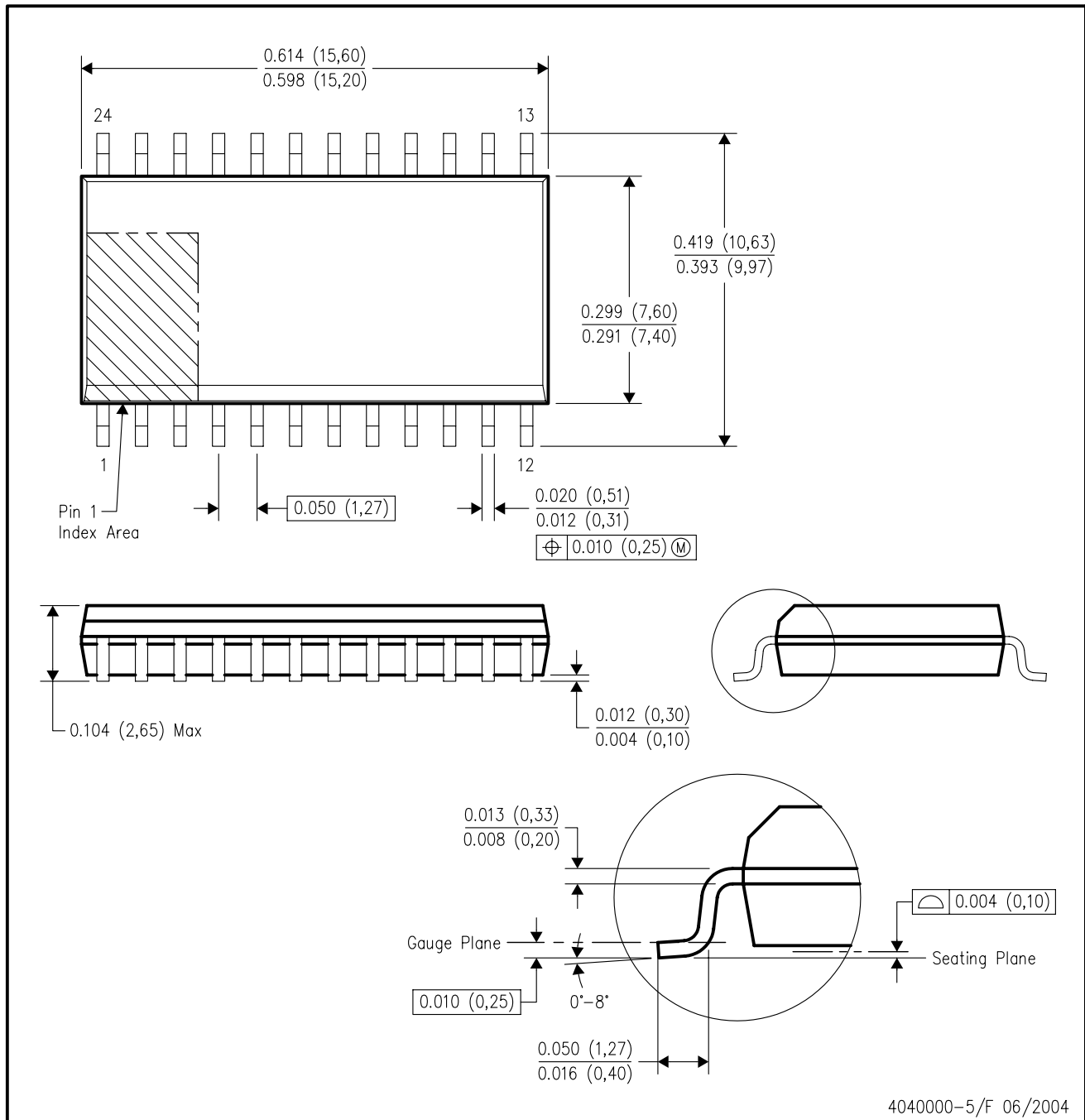
24 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE

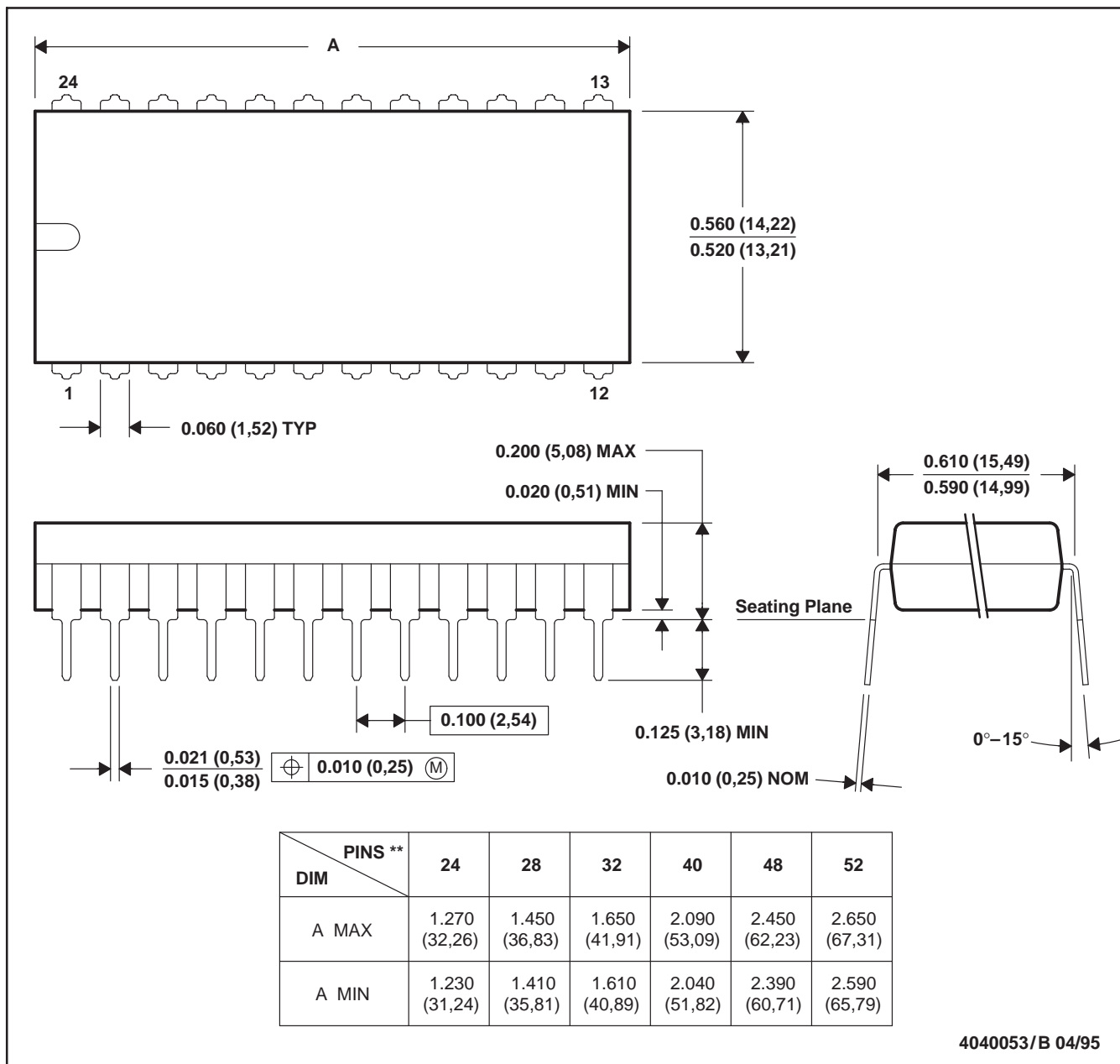


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

**N (R-PDIP-T\*\*)**

**PLASTIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN

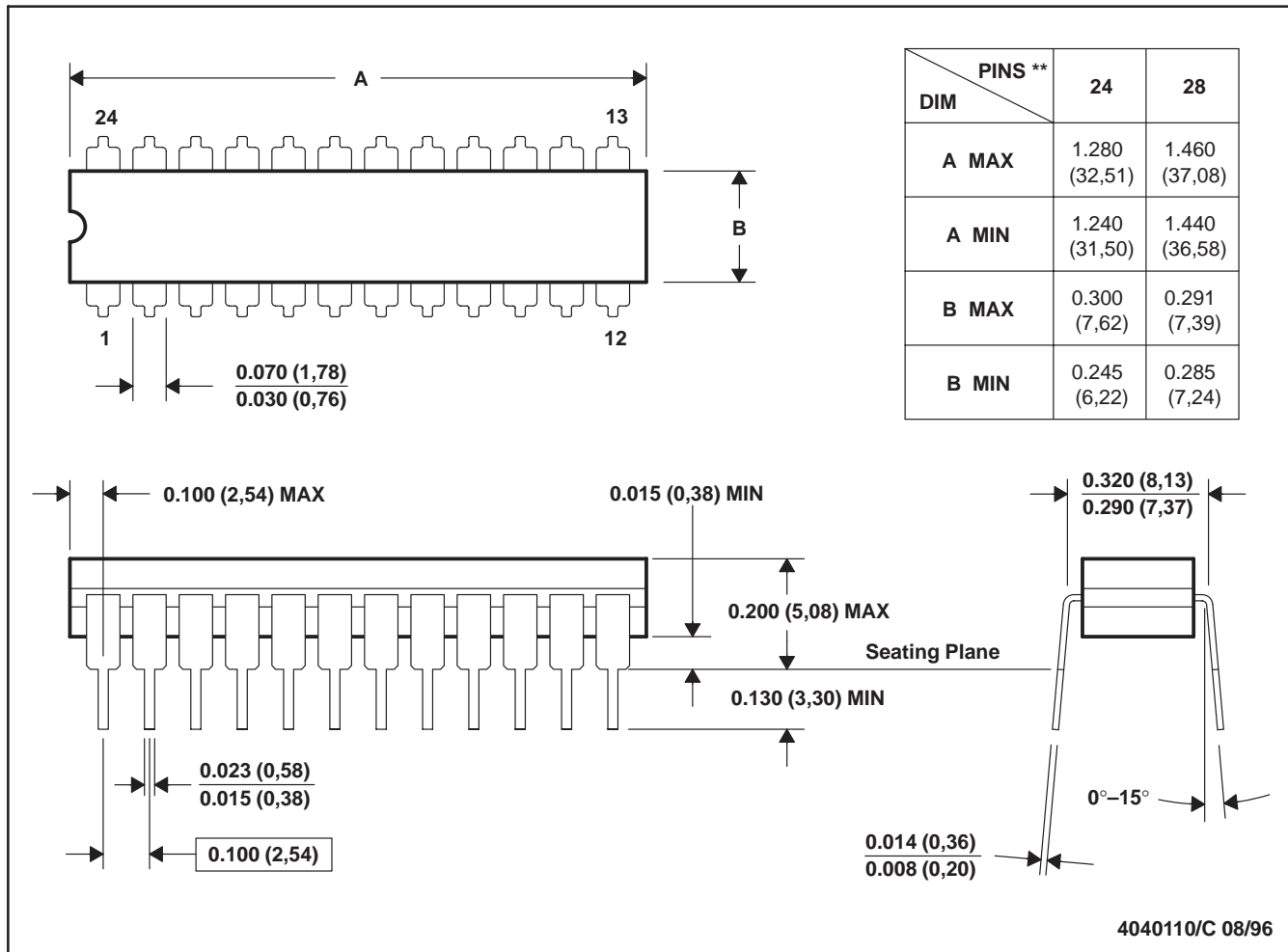


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-011  
 D. Falls within JEDEC MS-015 (32 pin only)

JT (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

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