

# SN54ALVTH32244, SN74ALVTH32244 2.5-V/3.3-V 32-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCES279 – SEPTEMBER 1999

- State-of-the-Art Advanced BiCMOS Technology (ABT) *Widebus*™ Design for 2.5-V and 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V  $V_{CC}$ )
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- High Drive ( $-24/24$  mA at 2.5-V  $V_{CC}$  and  $-32/64$  mA at 3.3-V  $V_{CC}$ )
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Use Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating
- Auto3-State Eliminates Bus Current Loading When Output Exceeds  $V_{CC} + 0.5$  V
- Flow-Through Architecture Facilitates Printed Circuit Board Layout
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- ESD Protection Exceeds JESD-22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Packaged in Plastic Fine-Pitch Ball Grid Array Package

NOTE: For tape and reel order entry:  
The GKER package is abbreviated to KR.

## description

The 'ALVTH32244 devices are 32-bit buffers/line drivers designed for 2.5-V or 3.3-V  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as eight 4-bit buffers, four 8-bit buffers, two 16-bit buffers, or one 32-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

When  $V_{CC}$  is between 0 and 1.2-V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2-V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ALVTH32244 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ALVTH32244 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

FUNCTION TABLE  
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z



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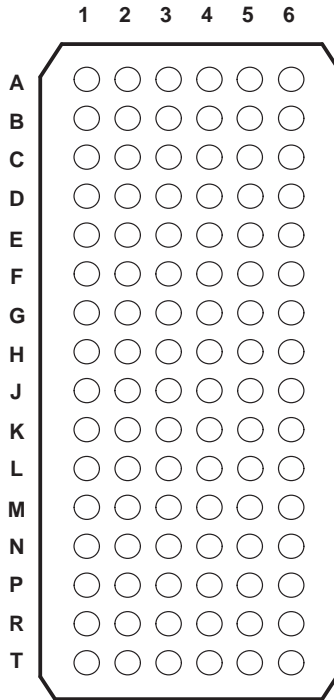


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**WITH 3-STATE OUTPUTS**

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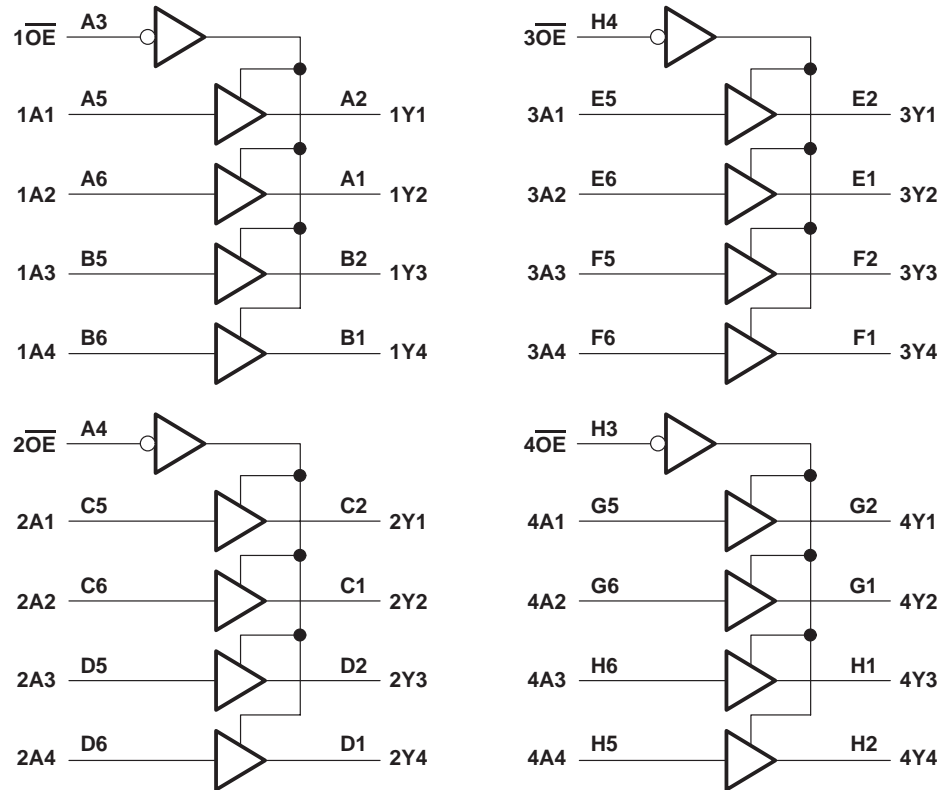
**GKE PACKAGE**  
**(TOP VIEW)**



**terminal assignments**

	1	2	3	4	5	6
A	1Y2	1Y1	$\overline{1OE}$	$\overline{2OE}$	1A1	1A2
B	1Y4	1Y3	GND	GND	1A3	1A4
C	2Y2	2Y1	1V <sub>CC</sub>	1V <sub>CC</sub>	2A1	2A2
D	2Y4	2Y3	GND	GND	2A3	2A4
E	3Y2	3Y1	GND	GND	3A1	3A2
F	3Y4	3Y3	1V <sub>CC</sub>	1V <sub>CC</sub>	3A3	3A4
G	4Y2	4Y1	GND	GND	4A1	4A2
H	4Y3	4Y4	$\overline{4OE}$	$\overline{3OE}$	4A4	4A3
J	5Y2	5Y1	$\overline{5OE}$	$\overline{6OE}$	5A1	5A2
K	5Y4	5Y3	GND	GND	5A3	5A4
L	6Y2	6Y1	2V <sub>CC</sub>	2V <sub>CC</sub>	6A1	6A2
M	6Y4	6Y3	GND	GND	6A3	6A4
N	7Y2	7Y1	GND	GND	7A1	7A2
P	7Y4	7Y3	2V <sub>CC</sub>	2V <sub>CC</sub>	7A3	7A4
R	8Y2	8Y1	GND	GND	8A1	8A2
T	8Y3	8Y4	$\overline{8OE}$	$\overline{7OE}$	8A4	8A3

logic diagram (positive logic)

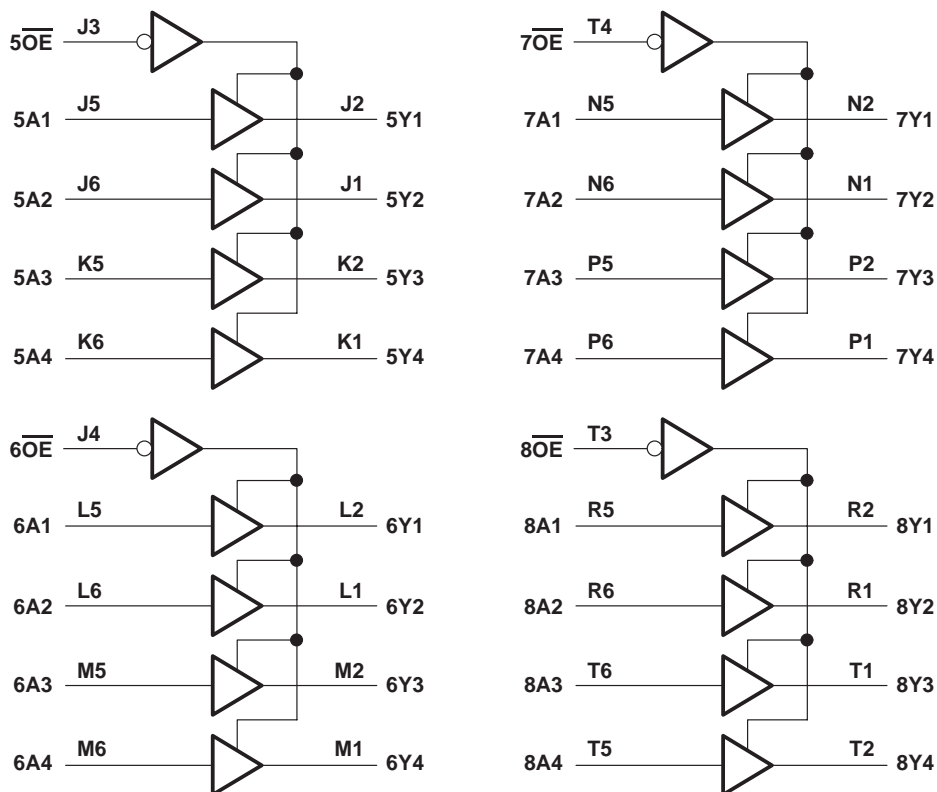


NOTE A: 1V<sub>CC</sub> is associated with these channels.

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**logic diagram (positive logic)**



NOTE A:  $2V_{CC}$  is associated with these channels.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Current into any output in the low state, $I_O$ : SN54ALVTH32244 .....	96 mA
SN74ALVTH32244 .....	128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54ALVTH32244 .....	48 mA
SN74ALVTH32244 .....	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3) .....	40°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (see Note 4)

		SN54ALVTH32244		SN74ALVTH32244		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.3	2.7	2.3	2.7	V
$V_{IH}$	High-level input voltage	1.7		1.7		V
$V_{IL}$	Low-level input voltage		0.7		0.7	V
$V_I$	Input voltage	0	5.5	0	5.5	V
$I_{OH}$	High-level output current		-6		-8	mA
$I_{OL}$	Low-level output current		6		8	mA
	Low-level output current; current duty cycle $\leq 50\%$ ; $f \geq 1\text{ kHz}$		18		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu\text{s/V}$
$T_A$	Operating free-air temperature	-55	125	-40	85	$^{\circ}\text{C}$

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (see Note 4)

		SN54ALVTH32244		SN74ALVTH32244		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	3	3.6	3	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	5.5	0	5.5	V
$I_{OH}$	High-level output current		-24		-32	mA
$I_{OL}$	Low-level output current		24		32	mA
	Low-level output current; current duty cycle $\leq 50\%$ ; $f \geq 1\text{ kHz}$		48		64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu\text{s/V}$
$T_A$	Operating free-air temperature	-55	125	-40	85	$^{\circ}\text{C}$

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54ALVTH32244, SN74ALVTH32244 2.5-V/3.3-V 32-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALVTH32244		SN74ALVTH32244		UNIT
				MIN	TYP†	MAX	MIN	
$V_{IK}$		$V_{CC} = 2.3\text{ V}$ , $I_I = -18\text{ mA}$		-1.2		-1.2		V
$V_{OH}$		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$		V
		$V_{CC} = 2.3\text{ V}$		1.8		1.8		
$V_{OL}$		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$ , $I_{OL} = 100\text{ }\mu\text{A}$		0.2		0.2		V
		$V_{CC} = 2.3\text{ V}$		$I_{OL} = 6\text{ mA}$		0.4		
				$I_{OL} = 8\text{ mA}$		0.4		
				$I_{OL} = 18\text{ mA}$		0.5		
		$I_{OL} = 24\text{ mA}$				0.5		
$I_I$	Control inputs	$V_{CC} = 2.7\text{ V}$ , $V_I = V_{CC}$ or GND		$\pm 1$		$\pm 1$		$\mu\text{A}$
		$V_{CC} = 0$ or $2.7\text{ V}$ , $V_I = 5.5\text{ V}$		10		10		
Data inputs	$V_{CC} = 2.7\text{ V}$		$V_I = V_{CC}$		1			
			$V_I = 0$		-5			
$I_{off}$		$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to $4.5\text{ V}$				$\pm 100$		$\mu\text{A}$
$I_{BHL}^\ddagger$		$V_{CC} = 2.3\text{ V}$ , $V_I = 0.7\text{ V}$		115		115		$\mu\text{A}$
$I_{BHH}^\S$		$V_{CC} = 2.3\text{ V}$ , $V_I = 1.7\text{ V}$		-10		-10		$\mu\text{A}$
$I_{BHLO}^\P$		$V_{CC} = 2.7\text{ V}$ , $V_I = 0$ to $V_{CC}$		300		300		$\mu\text{A}$
$I_{BHHO}^\#$		$V_{CC} = 2.7\text{ V}$ , $V_I = 0$ to $V_{CC}$		-300		-300		$\mu\text{A}$
$I_{EX}^\parallel$		$V_{CC} = 2.3\text{ V}$ , $V_O = 5.5\text{ V}$		125		125		$\mu\text{A}$
$I_{OZ(PU/PD)}^\star$		$V_{CC} \leq 1.2\text{ V}$ , $V_O = 0.5\text{ V}$ to $V_{CC}$ , $V_I = \text{GND}$ or $V_{CC}$ , $\overline{OE} = \text{don't care}$		$\pm 100$		$\pm 100$		$\mu\text{A}$
$I_{OZH}$		$V_{CC} = 2.7\text{ V}$		5		5		$\mu\text{A}$
		$V_O = 2.3\text{ V}$ , $V_I = 0.7\text{ V}$ or $1.7\text{ V}$						
$I_{OZL}$		$V_{CC} = 2.7\text{ V}$		-5		-5		$\mu\text{A}$
		$V_O = 0.5\text{ V}$ , $V_I = 0.7\text{ V}$ or $1.7\text{ V}$						
$I_{CC}$		$V_{CC} = 2.7\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND		Outputs high		0.04 0.1		mA
				Outputs low		2.3 4.5		
				Outputs disabled		0.04 0.1		
$C_i$		$V_{CC} = 2.5\text{ V}$ , $V_I = 2.5\text{ V}$ or 0		3		3		pF
$C_o$		$V_{CC} = 2.5\text{ V}$ , $V_O = 2.5\text{ V}$ or 0		6		6		pF

† All typical values are at  $V_{CC} = 2.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The bus-hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max.  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{IL}$  max.

§ The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

¶ An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.

# An external driver must sink at least  $I_{BHHO}$  to switch this node from high to low.

|| Current into an output in the high state when  $V_O > V_{CC}$

☆ High-impedance state during power up or power down

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electrical characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALVTH32244		SN74ALVTH32244		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
$V_{IK}$		$V_{CC} = 3 \text{ V}$ , $I_I = -18 \text{ mA}$			-1.2		V	
$V_{OH}$		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ , $I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$		$V_{CC} - 0.2$		V	
		$V_{CC} = 3 \text{ V}$	2		2			
$V_{OL}$		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ , $I_{OL} = 100 \mu\text{A}$	0.2		0.2		V	
		$V_{CC} = 3 \text{ V}$	$I_{OL} = 16 \text{ mA}$			0.4		
			$I_{OL} = 24 \text{ mA}$	0.5				
			$I_{OL} = 32 \text{ mA}$			0.5		
			$I_{OL} = 48 \text{ mA}$	0.55				
$I_{OL} = 64 \text{ mA}$			0.55					
$I_I$	Control inputs	$V_{CC} = 3.6 \text{ V}$ , $V_I = V_{CC} \text{ or GND}$	$\pm 1$		$\pm 1$		$\mu\text{A}$	
		$V_{CC} = 0 \text{ or } 3.6 \text{ V}$ , $V_I = 5.5 \text{ V}$	10		10			
	Data inputs	$V_{CC} = 3.6 \text{ V}$	$V_I = 5.5 \text{ V}$	20		20		
			$V_I = V_{CC}$	1		1		
		$V_I = 0$	-5		-5			
$I_{off}$		$V_{CC} = 0$ , $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$			$\pm 100$		$\mu\text{A}$	
$I_{BHL}^\ddagger$		$V_{CC} = 3 \text{ V}$ , $V_I = 0.8 \text{ V}$	75		75		$\mu\text{A}$	
$I_{BHH}^\S$		$V_{CC} = 3 \text{ V}$ , $V_I = 2 \text{ V}$	-75		-75		$\mu\text{A}$	
$I_{BHLO}^\P$		$V_{CC} = 3.6 \text{ V}$ , $V_I = 0 \text{ to } V_{CC}$	500		500		$\mu\text{A}$	
$I_{BHHO}^\#$		$V_{CC} = 3.6 \text{ V}$ , $V_I = 0 \text{ to } V_{CC}$	-500		-500		$\mu\text{A}$	
$I_{EX}^\parallel$		$V_{CC} = 3 \text{ V}$ , $V_O = 5.5 \text{ V}$	125		125		$\mu\text{A}$	
$I_{OZ}(\text{PU/PD})^\star$		$V_{CC} \leq 1.2 \text{ V}$ , $V_O = 0.5 \text{ V to } V_{CC}$ , $V_I = \text{GND or } V_{CC}$ , $\text{OE} = \text{don't care}$	$\pm 100$		$\pm 100$		$\mu\text{A}$	
$I_{OZH}$		$V_{CC} = 3.6 \text{ V}$ $V_O = 3 \text{ V}$ , $V_I = 0.8 \text{ V or } 2 \text{ V}$	5		5		$\mu\text{A}$	
$I_{OZL}$		$V_{CC} = 3.6 \text{ V}$ $V_O = 0.5 \text{ V}$ , $V_I = 0.8 \text{ V or } 2 \text{ V}$	-5		-5		$\mu\text{A}$	
$I_{CC}$		$V_{CC} = 3.6 \text{ V}$ , $I_O = 0$ , $V_I = V_{CC} \text{ or GND}$	Outputs high	0.07	0.1	0.07	0.1	mA
			Outputs low	3.2	5	3.2	5	
			Outputs disabled	0.07	0.1	0.07	0.1	
$\Delta I_{CC}^\square$		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$ , One input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC} \text{ or GND}$	0.4		0.4		mA	
$C_i$		$V_{CC} = 3.3 \text{ V}$ ,	3		3		pF	
$C_o$		$V_{CC} = 3.3 \text{ V}$ ,	6		6		pF	

† All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The bus-hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max.  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{IL}$  max.

§ The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

¶ An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.

# An external driver must sink at least  $I_{BHHO}$  to switch this node from high to low.

|| Current into an output in the high state when  $V_O > V_{CC}$

☆ High-impedance state during power up or power down

□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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switching characteristics over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$ ,  $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH32244		SN74ALVTH32244		UNIT
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	1	3.1	1	3	ns
t <sub>PHL</sub>			1	3.6	1	3.5	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Y	1.1	6	1.1	5.9	ns
t <sub>PZL</sub>			1.1	4.8	1.1	4.7	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Y	1.5	4.5	1.5	4.4	ns
t <sub>PLZ</sub>			1	3.5	1	3.4	

switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$ ,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 2)

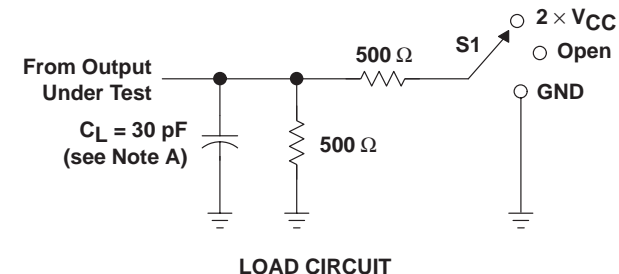
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH32244		SN74ALVTH32244		UNIT
			MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	1	2.6	1	2.4	ns
t <sub>PHL</sub>			1	2.6	1	2.5	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Y	1	3.9	1	3.8	ns
t <sub>PZL</sub>			1	3	1	2.9	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Y	1.5	4.3	1.5	4.2	ns
t <sub>PLZ</sub>			1.5	3.7	1.5	3.6	

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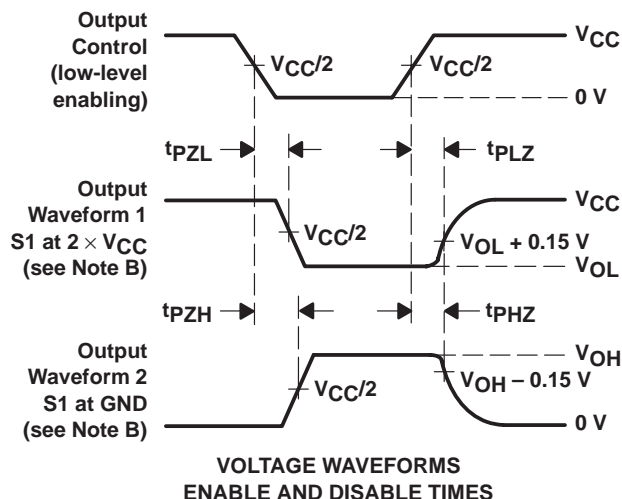
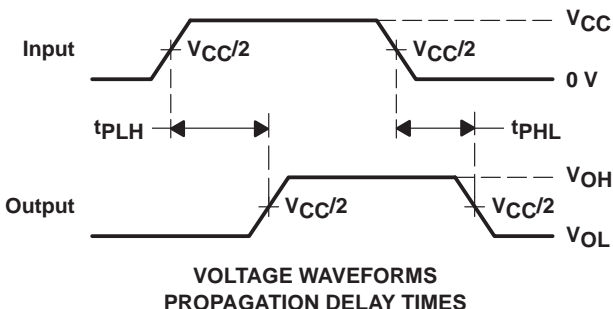
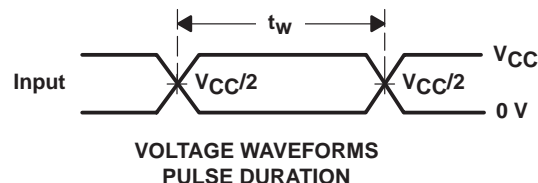
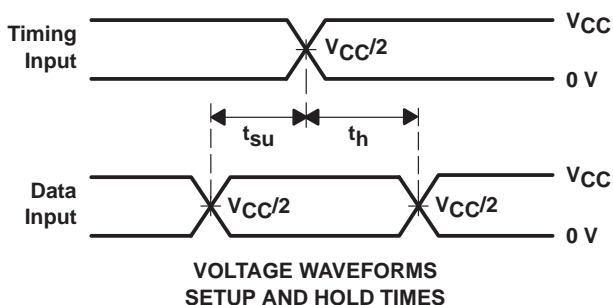


PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times$ $V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

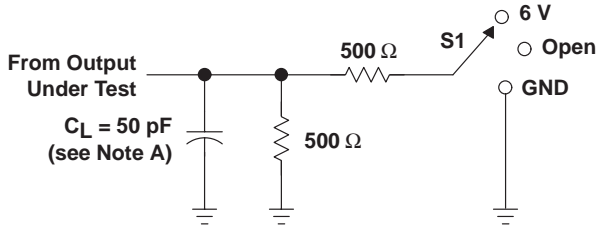
Figure 1. Load Circuit and Voltage Waveforms

**SN54ALVTH32244, SN74ALVTH32244**  
**2.5-V/3.3-V 32-BIT BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

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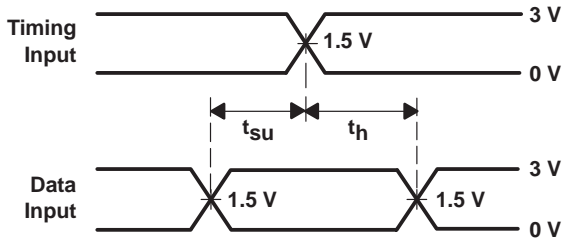
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

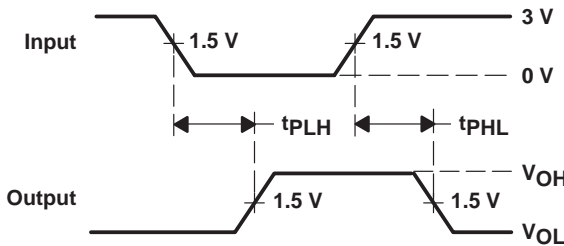


**LOAD CIRCUIT**

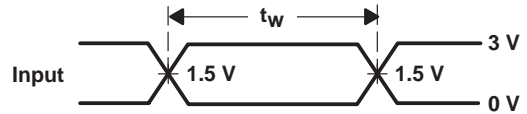
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



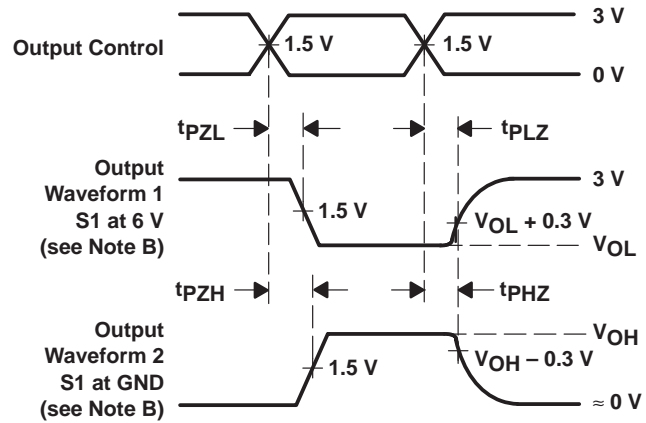
**VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES  
 INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
 PULSE DURATION**



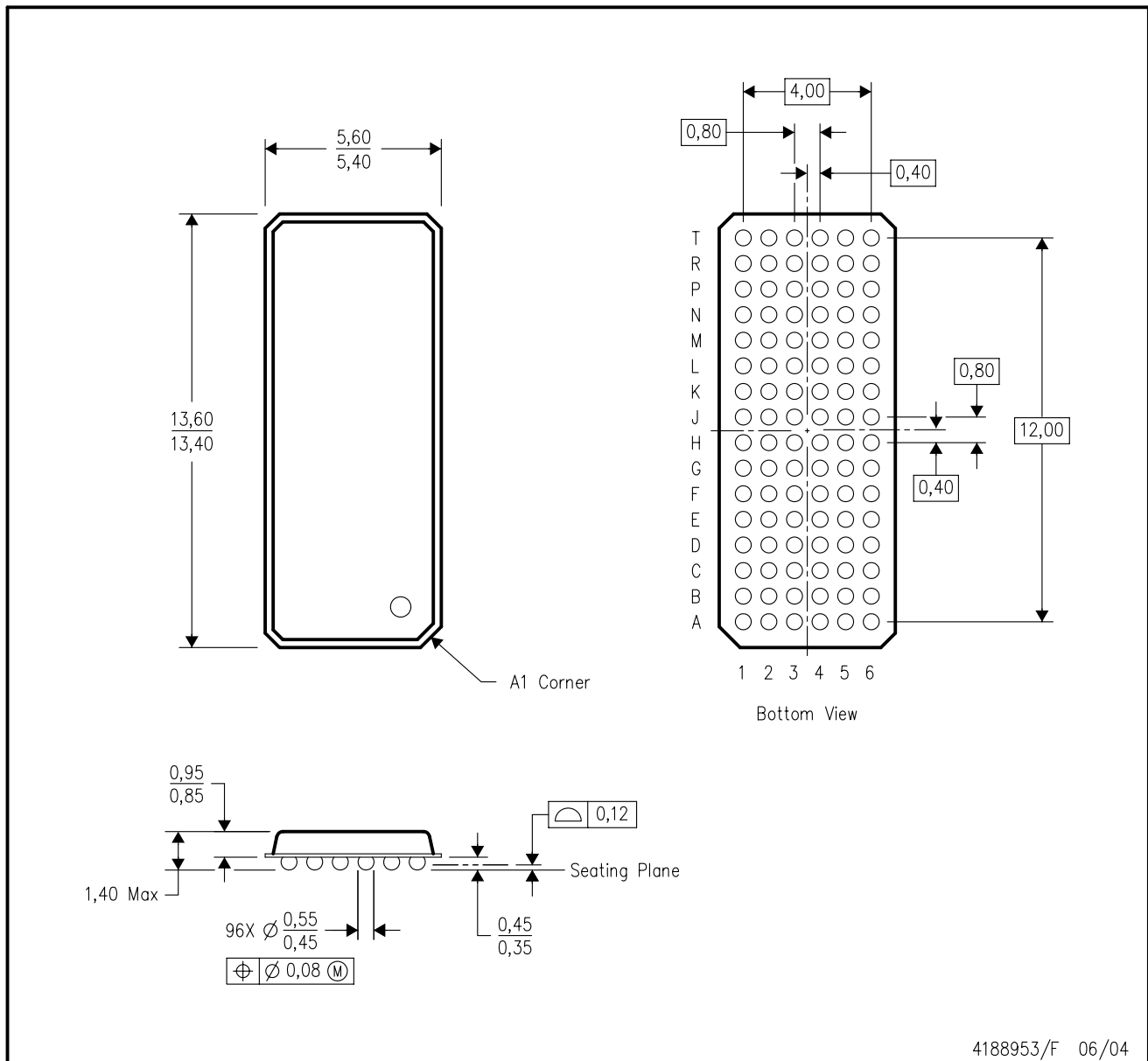
**VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES  
 LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

GKE (R-PBGA-N96)

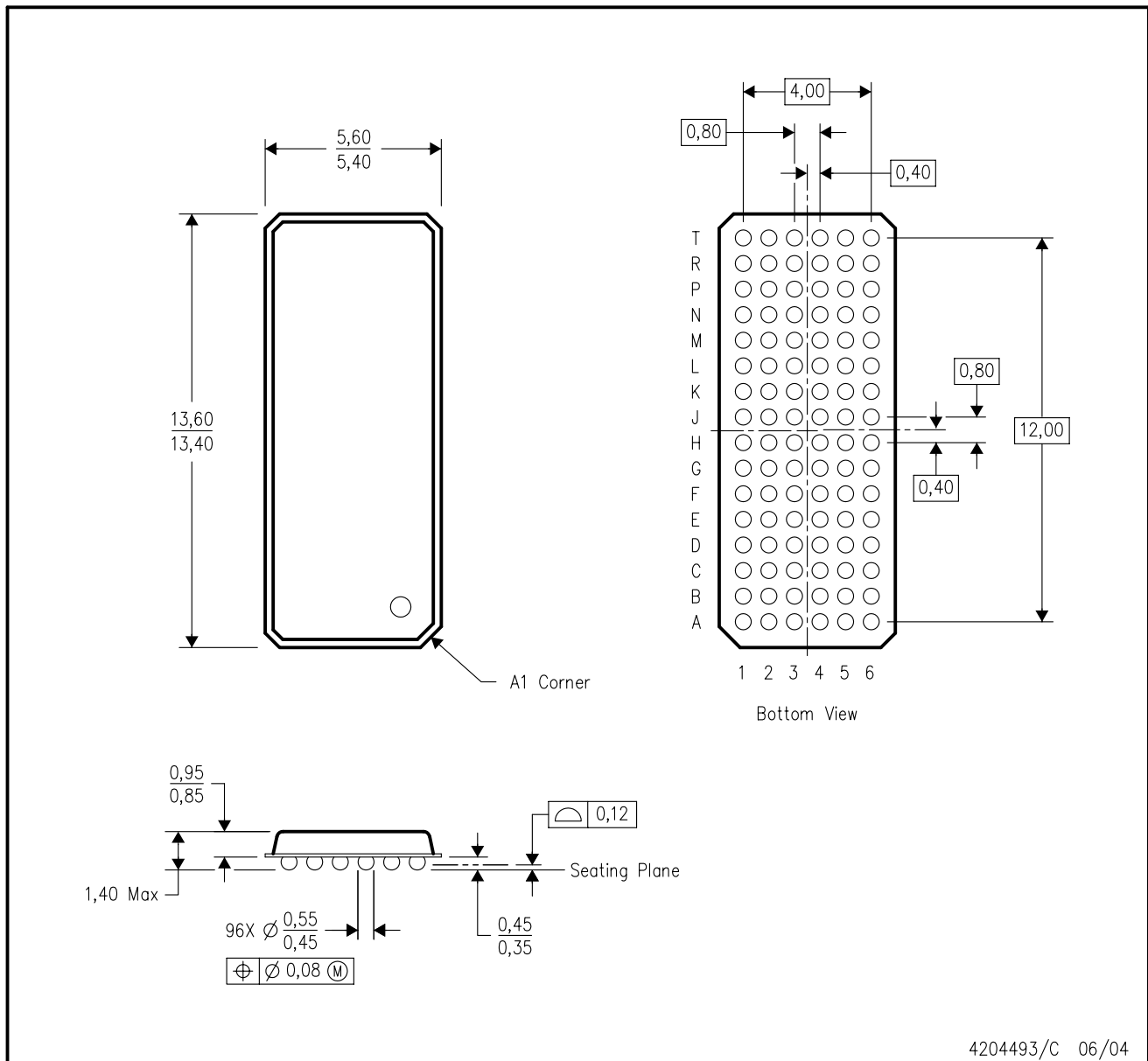
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-205 variation CC.
  - D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-205 variation CC.
  - D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

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		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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