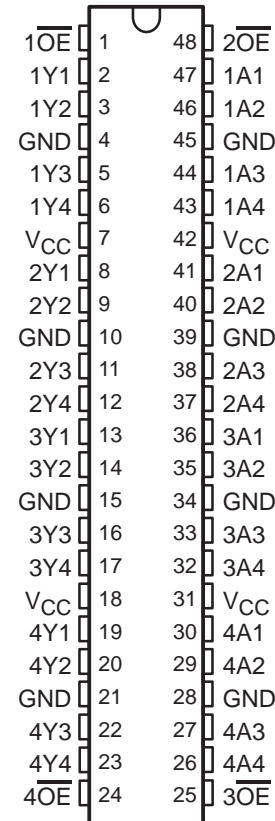


# SN54ALVTH162244, SN74ALVTH162244 2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCES074E – JUNE 1996 - REVISED JANUARY 1999

- State-of-the-Art Advanced BiCMOS Technology (ABT) *Widebus*™ Design for 2.5-V and 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 2.3-V to 3.6-V  $V_{CC}$ )
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- High-Impedance State During Power Up and Power Down Prevents Driver Conflict
- Uses Bus Hold on Data Inputs in Place of External Pullup/Pulldown Resistors to Prevent the Bus From Floating
- Output Ports Have Equivalent 30- $\Omega$  Series Resistors, So No External Resistors Are Required
- Auto3-State Eliminates Bus Current Loading When Output Exceeds  $V_{CC} + 0.5$  V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model; and Exceeds 1000 V Using Charged-Device Model, Robotic Method
- Flow-Through Architecture Facilitates Printed Circuit Board Layout
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Package

SN54ALVTH162244 . . . WD PACKAGE  
SN74ALVTH162244 . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



NOTE: For order entry:  
The DGG package is abbreviated to G, and  
the DGV package is abbreviated to V.

## description

The 'ALVTH162244 devices are 16-bit buffers/line drivers designed for low-voltage 2.5-V or 3.3-V  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated

# SN54ALVTH162244, SN74ALVTH162244

## 2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

SCES074E – JUNE 1996 - REVISED JANUARY 1999

#### description (continued)

These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When  $V_{CC}$  is between 0 and 1.2 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.2 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

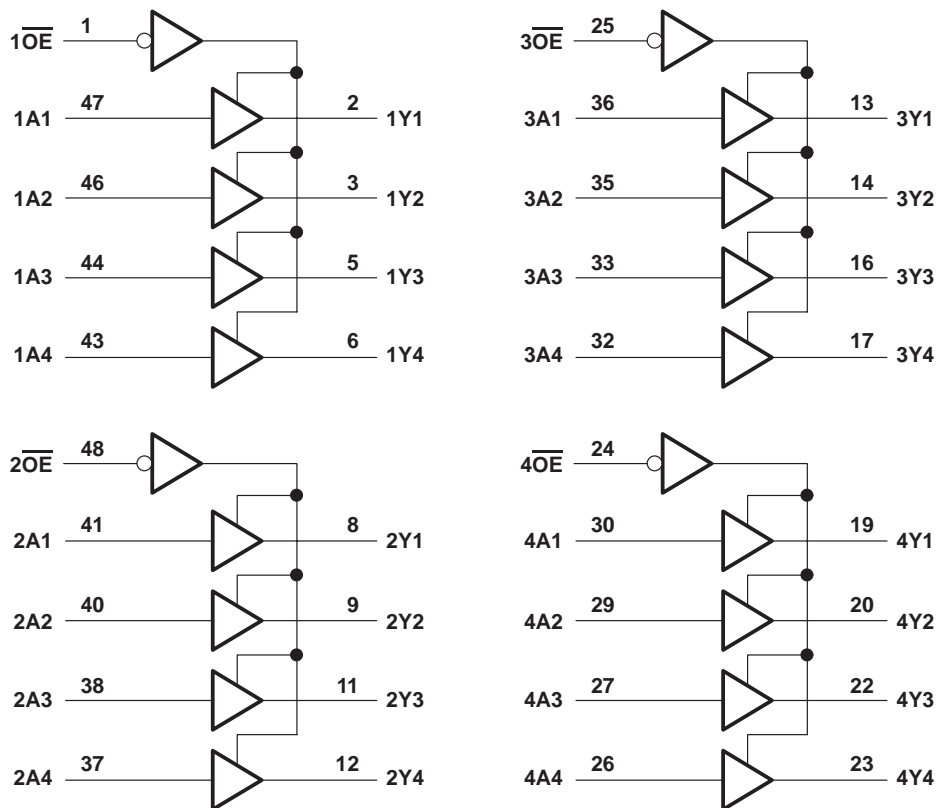
All outputs are designed to sink up to 12 mA and include equivalent 30- $\Omega$  resistors to reduce overshoot and undershoot.

The SN54ALVTH162244 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALVTH162244 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**FUNCTION TABLE**  
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

#### logic diagram (positive logic)





# SN54ALVTH162244, SN74ALVTH162244

## 2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

SCES074E – JUNE 1996 - REVISED JANUARY 1999

electrical characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALVTH162244		SN74ALVTH162244		UNIT
			MIN	TYP†	MAX	MIN	
$V_{IK}$	$V_{CC} = 2.3 \text{ V}$ , $I_I = -18 \text{ mA}$		-1.2		-1.2		V
$V_{OH}$	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ , $I_{OH} = -100 \mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$		V
	$V_{CC} = 2.3 \text{ V}$	$I_{OH} = -6 \text{ mA}$	1.7		1.7		
$V_{OL}$	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$ , $I_{OL} = 100 \mu\text{A}$		0.2		0.2		V
	$V_{CC} = 2.3 \text{ V}$	$I_{OL} = 8 \text{ mA}$	0.7		0.7		
		$I_{OL} = 12 \text{ mA}$			0.7		
$I_I$	Control inputs	$V_{CC} = 2.7 \text{ V}$ , $V_I = V_{CC} \text{ or GND}$	$\pm 1$		$\pm 1$		$\mu\text{A}$
		$V_{CC} = 0 \text{ or } 2.7 \text{ V}$ , $V_I = 5.5 \text{ V}$	10		10		
	Data inputs	$V_{CC} = 2.7 \text{ V}$ , $V_I = 5.5 \text{ V}$	10		10		
		$V_{CC} = 2.7 \text{ V}$ , $V_I = V_{CC}$	1		1		
	$V_{CC} = 2.7 \text{ V}$ , $V_I = 0$	-5		-5			
$I_{off}$	$V_{CC} = 0$ , $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$			$\pm 100$		$\mu\text{A}$	
$I_{BHL}^\ddagger$	$V_{CC} = 2.3 \text{ V}$ , $V_I = 0.7 \text{ V}$	115		115		$\mu\text{A}$	
$I_{BHH}^\S$	$V_{CC} = 2.3 \text{ V}$ , $V_I = 1.7 \text{ V}$	-10		-10		$\mu\text{A}$	
$I_{BHLO}^\P$	$V_{CC} = 2.7 \text{ V}$ , $V_I = 0 \text{ to } V_{CC}$	300		300		$\mu\text{A}$	
$I_{BHHO}^\#$	$V_{CC} = 2.7 \text{ V}$ , $V_I = 0 \text{ to } V_{CC}$	-300		-300		$\mu\text{A}$	
$I_{EX}^\parallel$	$V_{CC} = 2.3 \text{ V}$ , $V_O = 5.5 \text{ V}$	125		125		$\mu\text{A}$	
$I_{OZ(PU/PD)}^\star$	$V_{CC} \leq 1.2 \text{ V}$ , $V_O = 0.5 \text{ V to } V_{CC}$ , $V_I = \text{GND or } V_{CC}$ , $\overline{OE} = \text{don't care}$		$\pm 100$		$\pm 100$		$\mu\text{A}$
$I_{OZH}$	$V_{CC} = 2.7 \text{ V}$	$V_O = 2.3 \text{ V}$ , $V_I = 0.7 \text{ V or } 1.7 \text{ V}$	5		5		$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 2.7 \text{ V}$	$V_O = 0.5 \text{ V}$ , $V_I = 0.7 \text{ V or } 1.7 \text{ V}$	-5		-5		$\mu\text{A}$
$I_{CC}$	$V_{CC} = 2.7 \text{ V}$ , $I_O = 0$ , $V_I = V_{CC} \text{ or GND}$	Outputs high	0.04	0.1	0.04	0.1	mA
		Outputs low	2.3	4.5	2.3	4.5	
		Outputs disabled	0.04	0.1	0.04	0.1	
$C_i$	$V_{CC} = 2.5 \text{ V}$ , $V_I = 2.5 \text{ V or } 0$	3		3		pF	
$C_o$	$V_{CC} = 2.5 \text{ V}$ , $V_O = 2.5 \text{ V or } 0$	6		6		pF	

† All typical values are at  $V_{CC} = 2.5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The bus-hold circuit can sink at least the minimum low sustaining current at  $V_{IL} \text{ max}$ .  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{IL} \text{ max}$ .

§ The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IH} \text{ min}$ .  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH} \text{ min}$ .

¶ An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.

# An external driver must sink at least  $I_{BHHO}$  to switch this node from high to low.

|| Current into an output in the high state when  $V_O > V_{CC}$

☆ High-impedance state during power up or power down

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ALVTH162244, SN74ALVTH162244  
2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS

SCES074E – JUNE 1996 - REVISED JANUARY 1999

electrical characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALVTH162244		SN74ALVTH162244		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
$V_{IK}$		$V_{CC} = 3\text{ V}$ , $I_I = -18\text{ mA}$			-1.2		-1.2	V
$V_{OH}$		$V_{CC} = 3\text{ V to } 3.6\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$		$V_{CC}-0.2$			V
		$V_{CC} = 3\text{ V}$ , $I_{OH} = -8\text{ mA}$	2					
		$V_{CC} = 3\text{ V}$ , $I_{OH} = -12\text{ mA}$			2			
$V_{OL}$		$V_{CC} = 3\text{ V to } 3.6\text{ V}$ , $I_{OL} = 100\text{ }\mu\text{A}$	0.2		0.2			V
		$V_{CC} = 3\text{ V}$ , $I_{OL} = 8\text{ mA}$	0.8					
		$V_{CC} = 3\text{ V}$ , $I_{OL} = 12\text{ mA}$			0.8			
$I_I$	Control inputs	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$ or GND	$\pm 1$		$\pm 1$			$\mu\text{A}$
		$V_{CC} = 0$ or $3.6\text{ V}$ , $V_I = 5.5\text{ V}$	10		10			
	Data inputs	$V_{CC} = 3.6\text{ V}$ , $V_I = 5.5\text{ V}$	10		10			
		$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$	1		1			
		$V_{CC} = 3.6\text{ V}$ , $V_I = 0$	-5		-5			
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to $4.5\text{ V}$			$\pm 100$			$\mu\text{A}$	
$I_{BHL}^\ddagger$	$V_{CC} = 3\text{ V}$ , $V_I = 0.8\text{ V}$	75		75			$\mu\text{A}$	
$I_{BHH}^\S$	$V_{CC} = 3\text{ V}$ , $V_I = 2\text{ V}$	-75		-75			$\mu\text{A}$	
$I_{BHLO}^\parallel$	$V_{CC} = 3.6\text{ V}$ , $V_I = 0$ to $V_{CC}$	500		500			$\mu\text{A}$	
$I_{BHHO}^\#$	$V_{CC} = 3.6\text{ V}$ , $V_I = 0$ to $V_{CC}$	-500		-500			$\mu\text{A}$	
$I_{EX}^\parallel$	$V_{CC} = 3\text{ V}$ , $V_O = 5.5\text{ V}$	125		125			$\mu\text{A}$	
$I_{OZ(PU/PD)}^\star$	$V_{CC} \leq 1.2\text{ V}$ , $V_O = 0.5\text{ V to } V_{CC}$ , $V_I = \text{GND or } V_{CC}$ , $\overline{OE} = \text{don't care}$	$\pm 100$		$\pm 100$			$\mu\text{A}$	
$I_{OZH}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$ , $V_I = 0.8\text{ V or } 2\text{ V}$	5		5			$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$ , $V_I = 0.8\text{ V or } 2\text{ V}$	-5		-5			$\mu\text{A}$	
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND	Outputs high	0.07	0.1	0.07	0.1	mA	
		Outputs low	3.2	5	3.2	5		
		Outputs disabled	0.07	0.1	0.07	0.1		
$\Delta I_{CC}^\square$	$V_{CC} = 3\text{ V to } 3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND	0.4		0.4			mA	
$C_i$	$V_{CC} = 3.3\text{ V}$ , $V_I = 3.3\text{ V or } 0$	3		3			pF	
$C_o$	$V_{CC} = 3.3\text{ V}$ , $V_O = 3.3\text{ V or } 0$	6		6			pF	

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The bus-hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max.  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{IL}$  max.

§ The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

¶ An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.

# An external driver must sink at least  $I_{BHHO}$  to switch this node from high to low.

|| Current into an output in the high state when  $V_O > V_{CC}$

☆ High-impedance state during power up or power down

□ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

**SN54ALVTH162244, SN74ALVTH162244**  
**2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

SCES074E – JUNE 1996 - REVISED JANUARY 1999

switching characteristics over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$ ,  $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH162244		SN74ALVTH162244		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	1	4.3	1	4.2	ns
$t_{PHL}$			1.4	3.8	1.5	3.7	
$t_{PZH}$	$\overline{OE}$	Y	1.3	6.9	1.4	6.8	ns
$t_{PZL}$			1.3	5.2	1.4	5.1	
$t_{PHZ}$	$\overline{OE}$	Y	1	4.7	1	4.6	ns
$t_{PLZ}$			1	3.6	1	3.5	

switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$ ,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALVTH162244		SN74ALVTH162244		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	1	3.4	1	3.3	ns
$t_{PHL}$			1	3.4	1	3.3	
$t_{PZH}$	$\overline{OE}$	Y	1.4	5	1.5	4.9	ns
$t_{PZL}$			1.3	3.4	1.4	3.3	
$t_{PHZ}$	$\overline{OE}$	Y	1.4	5	1.5	4.9	ns
$t_{PLZ}$			1.4	4.4	1.5	4.3	

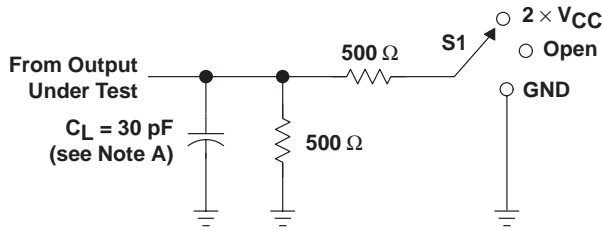
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

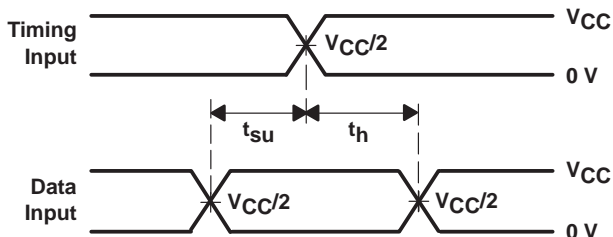
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

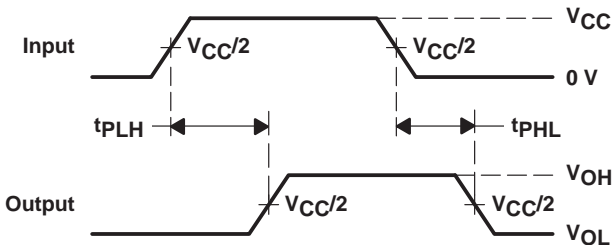


LOAD CIRCUIT

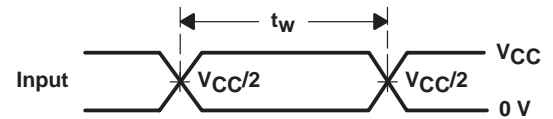
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



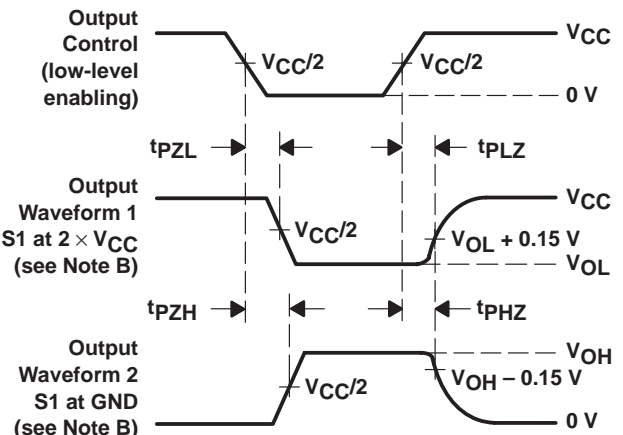
VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
 PULSE DURATION



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

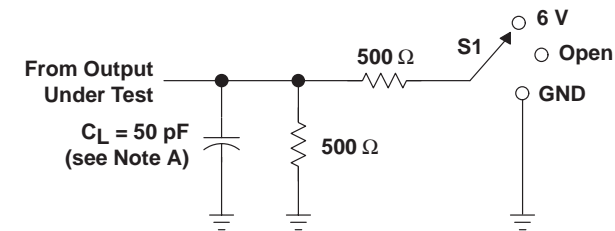
Figure 1. Load Circuit and Voltage Waveforms

**SN54ALVTH162244, SN74ALVTH162244**  
**2.5-V/3.3-V 16-BIT BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

SCES074E – JUNE 1996 - REVISED JANUARY 1999

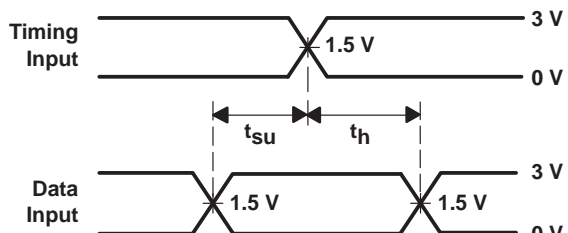
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

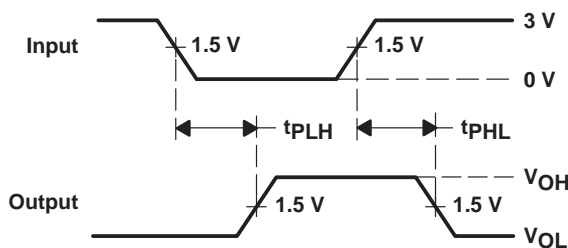


**LOAD CIRCUIT**

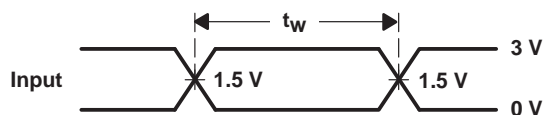
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



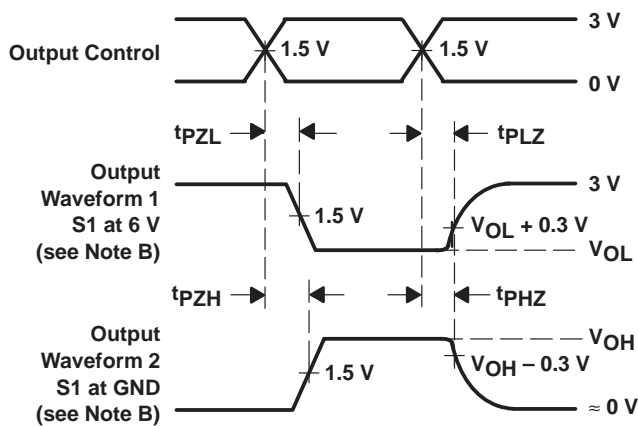
**VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES  
 INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
 PULSE DURATION**



**VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES  
 LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.