

## FEATURES

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65-V to 3.6-V  $V_{CC}$
- Max  $t_{pd}$  of 5 ns at 3.3-V  $V_{CC}$
- $\pm 24$ -mA Output Drive at 3.3-V  $V_{CC}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

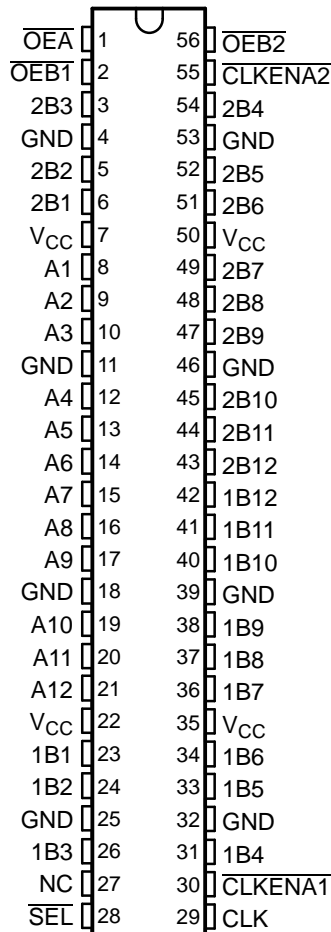
## DESCRIPTION/ORDERING INFORMATION

This 12-bit to 24-bit registered bus exchanger is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74ALVCH16269 is used in applications in which two separate ports must be multiplexed onto, or demultiplexed from, a single port. The device is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable ( $\overline{CLKENA}$ ) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select ( $\overline{SEL}$ ) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, extending the period during which the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables ( $\overline{OEA}$ ,  $\overline{OEB1}$ ,  $\overline{OEB2}$ ).

DGG OR DL PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP - DL	Tube	SN74ALVCH16269DL	ALVCH16269
		Tape and reel	SN74ALVCH16269DLR	
	TSSOP - DGG	Tape and reel	SN74ALVCH16269DGGR	ALVCH16269
	VFBGA - GQL	Tape and reel	SN74ALVCH16269KR	VH269
	VFBGA - ZQL (Pb-free)		74ALVCH16269ZQLR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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# SN74ALVCH16269

## 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

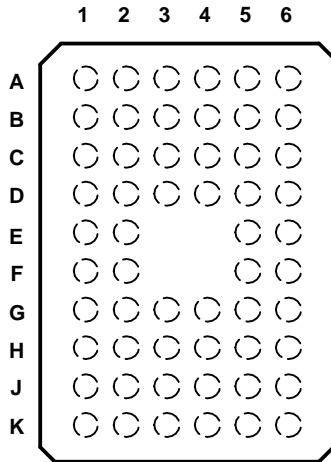
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### DESCRIPTION/ORDERING INFORMATION (CONTINUED)

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible, and  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to  $\overline{OE}$  being routed through a register, the active state of the outputs cannot be determined before the arrival of the first clock pulse.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

**GQL OR ZQL PACKAGE  
(TOP VIEW)**



**TERMINAL ASSIGNMENTS<sup>(1)</sup>**

	1	2	3	4	5	6
<b>A</b>	2B3	$\overline{OEB1}$	$\overline{OEA}$	$\overline{OEB2}$	$\overline{CLKENA2}$	2B4
<b>B</b>	2B1	2B2	GND	GND	2B5	2B6
<b>C</b>	A2	A1	$V_{CC}$	$V_{CC}$	2B7	2B8
<b>D</b>	A4	A3	GND	GND	2B9	2B10
<b>E</b>	A6	A5			2B11	2B12
<b>F</b>	A7	A8			1B11	1B12
<b>G</b>	A9	A10	GND	GND	1B9	1B10
<b>H</b>	A11	A12	$V_{CC}$	$V_{CC}$	1B7	1B8
<b>J</b>	1B1	1B2	GND	GND	1B5	1B6
<b>K</b>	1B3	NC	$\overline{SEL}$	CLK	$\overline{CLKENA1}$	1B4

(1) NC - No internal connection

## FUNCTION TABLES

### OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	$\overline{OE\bar{A}}$	$\overline{OE\bar{B}}$	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

### A-TO-B STORAGE ( $\overline{OE\bar{B}} = L$ )

INPUTS				OUTPUTS	
$\overline{CLKENA1}$	$\overline{CLKENA2}$	CLK	A	1B	2B
L	H	↑	L	L	2B <sub>0</sub> <sup>(1)</sup>
L	H	↑	H	H	2B <sub>0</sub> <sup>(1)</sup>
L	L	↑	L	L	L
L	L	↑	H	H	H
H	L	↑	L	1B <sub>0</sub> <sup>(1)</sup>	L
H	L	↑	H	1B <sub>0</sub> <sup>(1)</sup>	H
H	H	X	X	1B <sub>0</sub> <sup>(1)</sup>	2B <sub>0</sub> <sup>(1)</sup>

- (1) Output level before the indicated steady-state input conditions were established

### B-TO-A STORAGE ( $\overline{OE\bar{A}} = L$ )

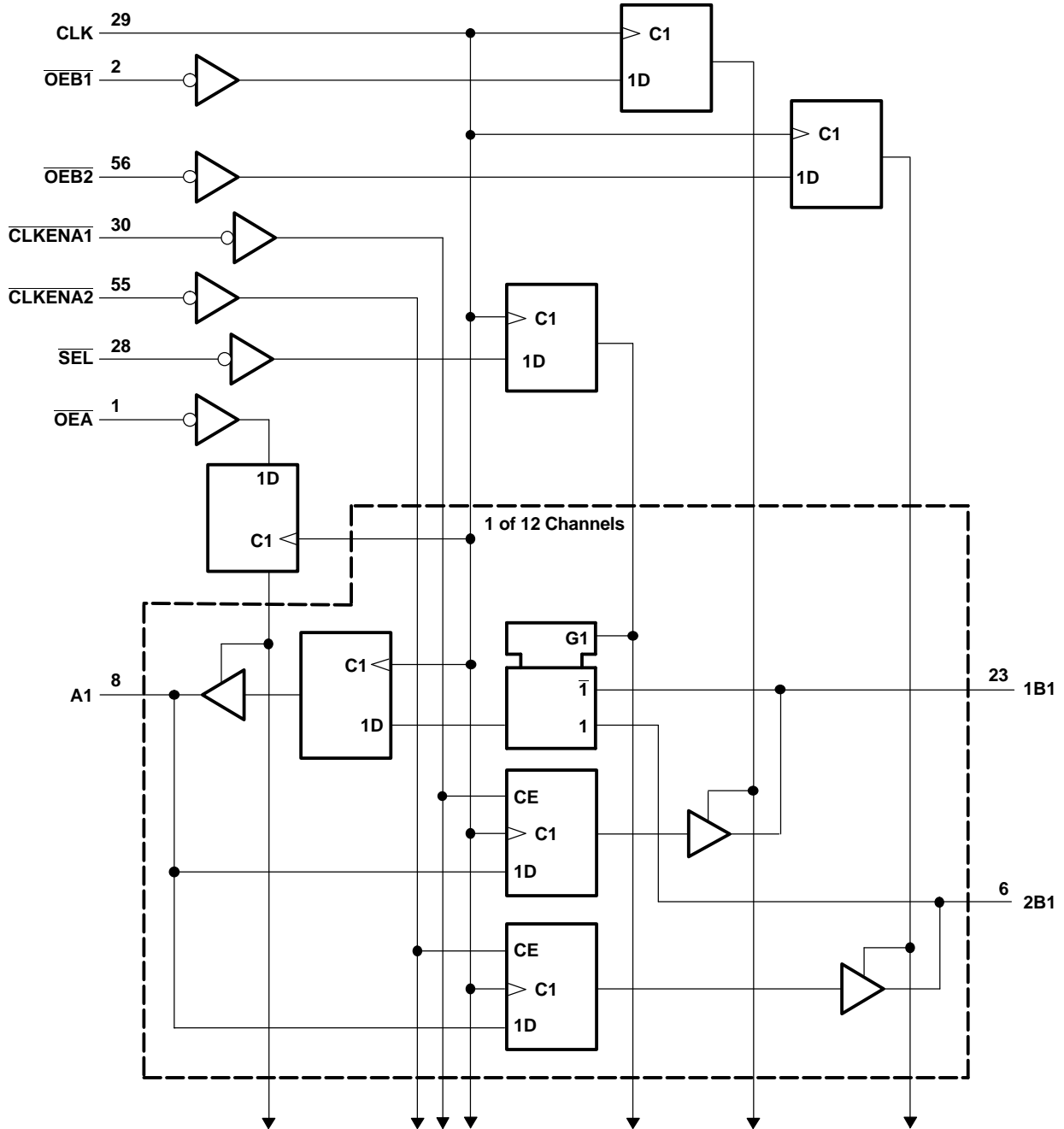
INPUTS				OUTPUT
CLK	$\overline{SEL}$	1B	2B	A
X	H	X	X	A <sub>0</sub> <sup>(1)</sup>
X	L	X	X	A <sub>0</sub> <sup>(1)</sup>
↑	H	L	X	L
↑	H	H	X	H
↑	L	X	L	L
↑	L	X	H	H

- (1) Output level before the indicated steady-state input conditions were established

# SN74ALVCH16269 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

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## LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG and DL packages.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	4.6	V
V <sub>I</sub>	Input voltage range	Except I/O ports <sup>(2)</sup>		V
		-0.5	V <sub>CC</sub> + 0.5	
V <sub>O</sub>	Output voltage range <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50
				mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50
				mA
I <sub>O</sub>	Continuous output current		±50	mA
	Continuous current through each V <sub>CC</sub> or GND		±100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	DGG package		81
		DL package		74
		GQL/ZQL package		42
				°C/W
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V, maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.65	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		V
		V <sub>CC</sub> = 2.3 V to 2.7 V		
		V <sub>CC</sub> = 2.7 V to 3.6 V		
		0.65 × V <sub>CC</sub>		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		V
		V <sub>CC</sub> = 2.3 V to 2.7 V		
		V <sub>CC</sub> = 2.7 V to 3.6 V		
			0.35 × V <sub>CC</sub>	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		mA
		V <sub>CC</sub> = 2.3 V		
		V <sub>CC</sub> = 2.7 V		
		V <sub>CC</sub> = 3 V		
			-4	
			-12	
			-12	
			-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		mA
		V <sub>CC</sub> = 2.3 V		
		V <sub>CC</sub> = 2.7 V		
		V <sub>CC</sub> = 3 V		
			4	
			12	
			12	
			24	
Δt/Δv	Input transition rise or fall rate		10	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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## 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

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### ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2			V
	I <sub>OH</sub> = -4 mA	1.65 V	1.2			
	I <sub>OH</sub> = -6 mA	2.3 V	2			
	I <sub>OH</sub> = -12 mA	2.3 V	1.7			
		2.7 V	2.2			
		3 V	2.4			
I <sub>OH</sub> = -24 mA	3 V	2				
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2	V
	I <sub>OL</sub> = 4 mA	1.65 V			0.45	
	I <sub>OL</sub> = 6 mA	2.3 V			0.4	
	I <sub>OL</sub> = 12 mA	2.3 V			0.7	
		2.7 V			0.4	
	I <sub>OL</sub> = 24 mA	3 V			0.55	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V			±5	μA
I <sub>I(hold)</sub>	V <sub>I</sub> = 0.58 V	1.65 V	25			μA
	V <sub>I</sub> = 1.07 V	1.65 V	-25			
	V <sub>I</sub> = 0.7 V	2.3 V	45			
	V <sub>I</sub> = 1.7 V	2.3 V	-45			
	V <sub>I</sub> = 0.8 V	3 V	75			
	V <sub>I</sub> = 2 V	3 V	-75			
	V <sub>I</sub> = 0 to 3.6 V <sup>(2)</sup>	3.6 V			±500	
I <sub>OZ</sub> <sup>(3)</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			±10	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			40	μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V			750	μA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	3.5		pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	9		pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

## TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	(1)		135		135		135		MHz
$t_w$	Pulse duration, CLK high or low	(1)		3.3		3.3		3.3		ns
$t_{\text{su}}$	Setup time	A data before CLK $\uparrow$		(1)		2		1.7		ns
		B data before CLK $\uparrow$		(1)		2.2		1.8		
		$\overline{\text{SEL}}$ before CLK $\uparrow$		(1)		1.6		1.3		
		$\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ before CLK $\uparrow$		(1)		1		0.9		
		$\overline{\text{OE}}$ before CLK $\uparrow$		(1)		1.5		1.3		
$t_h$	Hold time	A data after CLK $\uparrow$		(1)		0.7		0.6		ns
		B data after CLK $\uparrow$		(1)		0.7		0.6		
		$\overline{\text{SEL}}$ after CLK $\uparrow$		(1)		1.1		0.7		
		$\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ after CLK $\uparrow$		(1)		1		1.1		
		$\overline{\text{OE}}$ after CLK $\uparrow$		(1)		0.8		0.8		

(1) This information was not available at the time of publication.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			(1)		135		135		135		MHz
$t_{\text{pd}}$	CLK	B	(1)		1	8.2	7.3		1	6.2	ns
		A	(1)		1	6.4	5.8		1	5	
$t_{\text{en}}$	CLK	B	(1)		1	7.9	6.7		1	6.1	ns
		A	(1)		1	7.6	6.2		1	5.9	
$t_{\text{dis}}$	CLK	B	(1)		1	8.1	6.9		1	6.1	ns
		A	(1)		1	7.5	6.8		1	5.6	

(1) This information was not available at the time of publication.

## OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
$C_{\text{pd}}$	Power dissipation capacitance per exchanger	All outputs enabled	(1)	87	120	pF
		All outputs disabled	(1)	80.5	118	

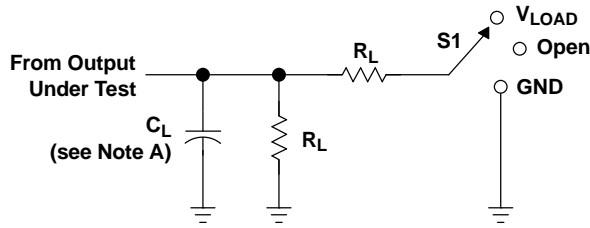
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## 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

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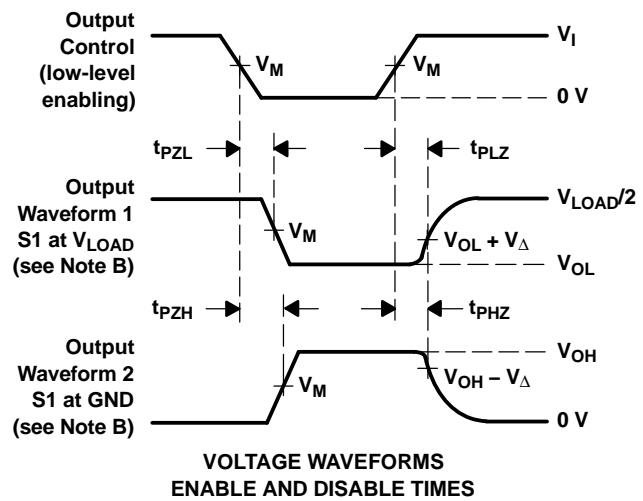
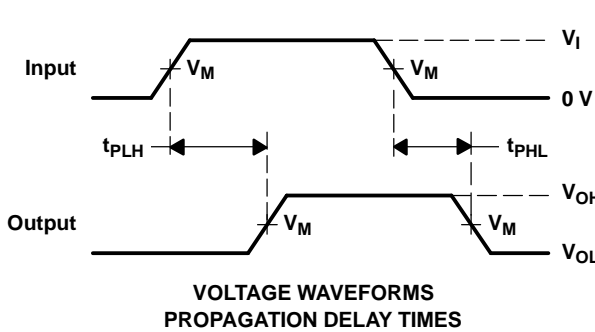
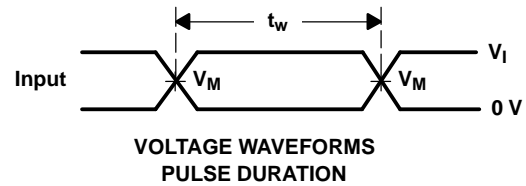
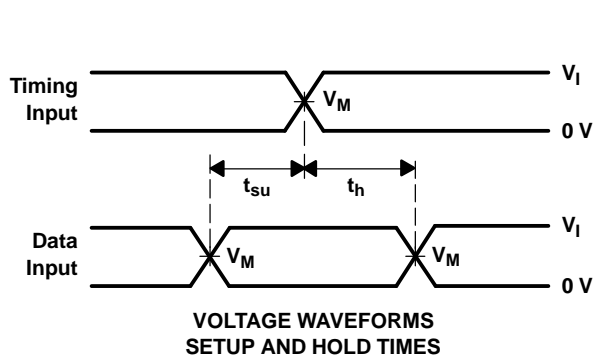
### PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUT		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
1.8 V	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5 V \pm 0.2 V$	$V_{CC}$	$\leq 2$ ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3 V \pm 0.3 V$	2.7 V	$\leq 2.5$ ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V

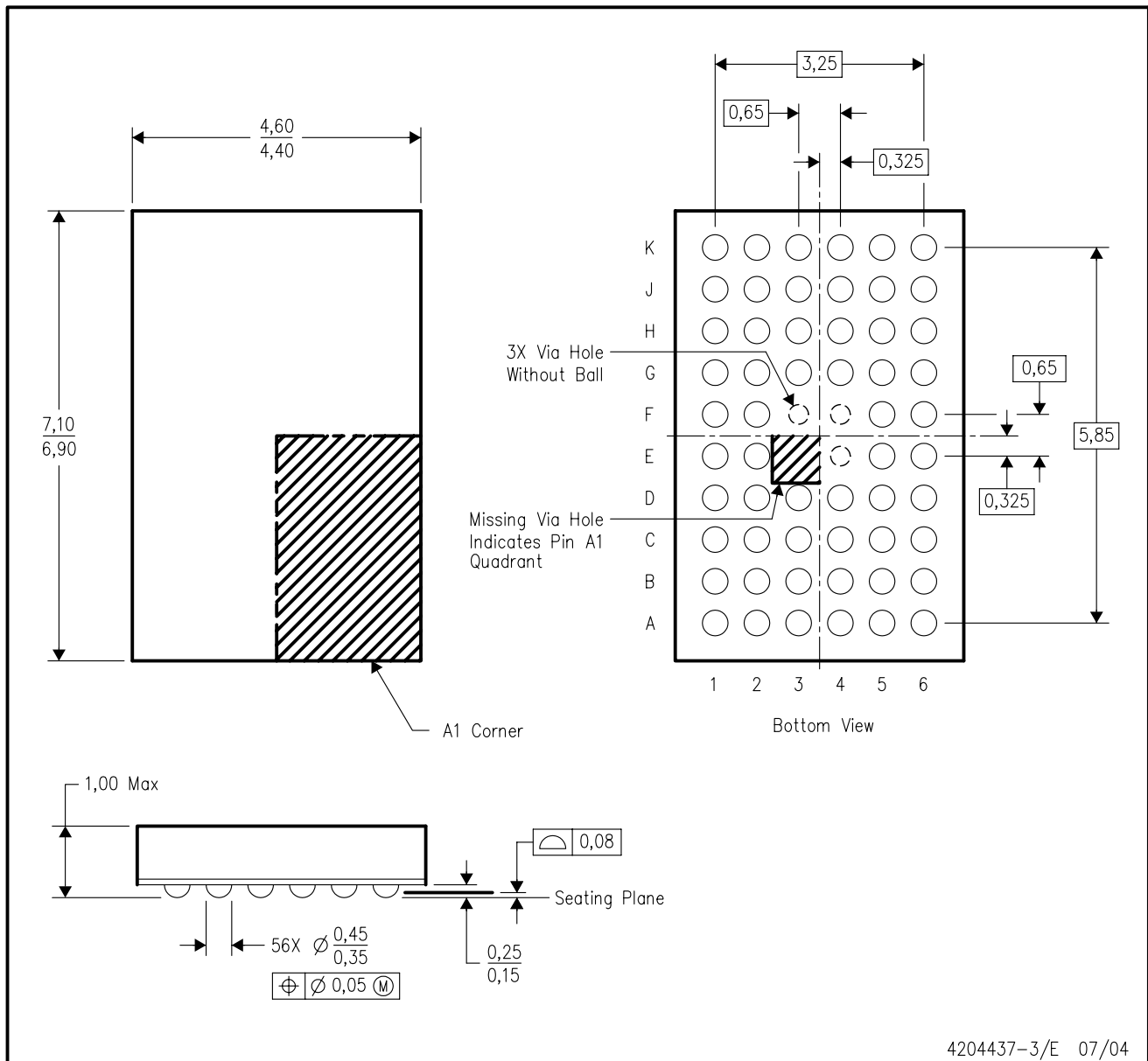


- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

ZQL (R-PBGA-N56)

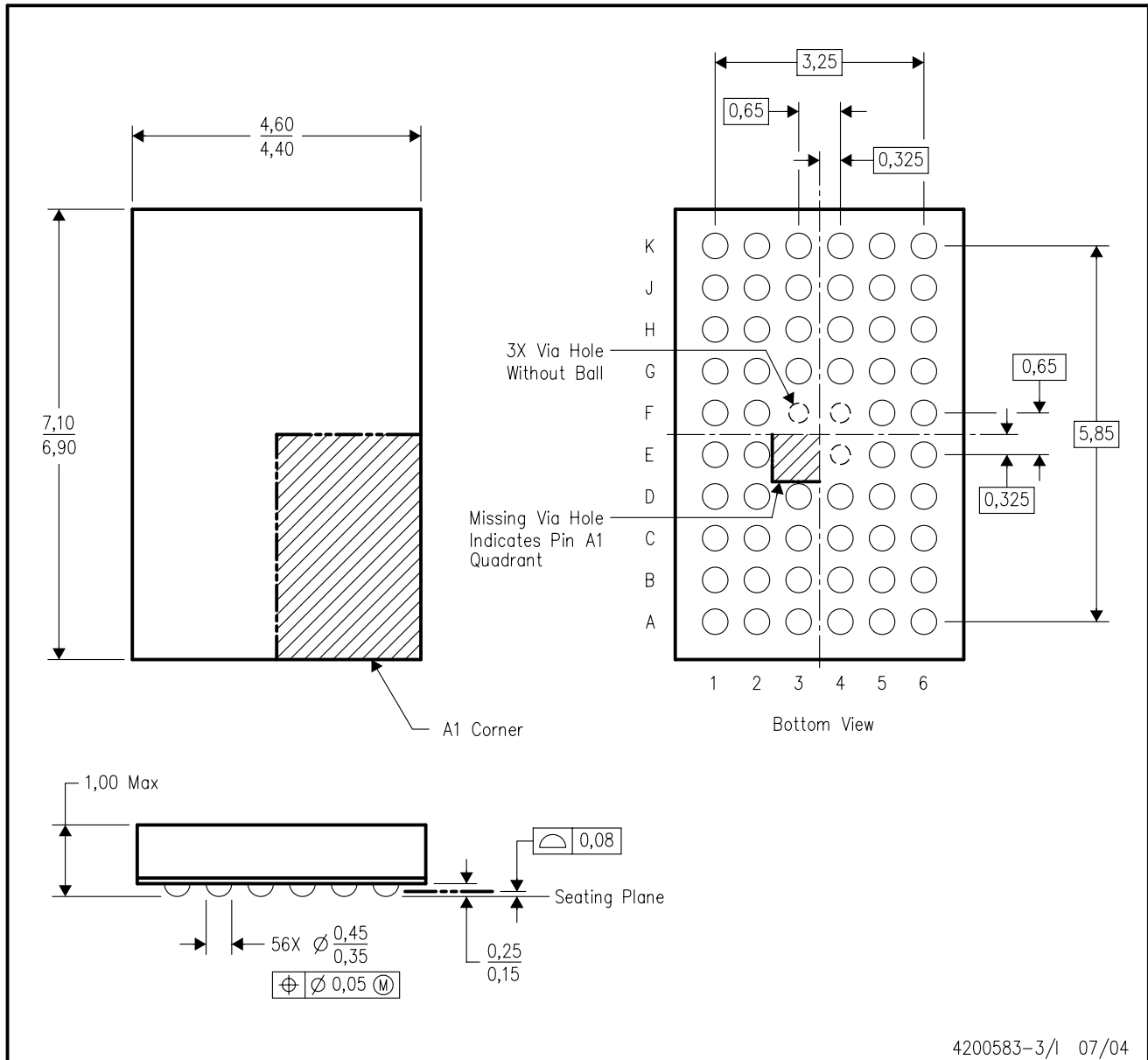
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225 variation BA.
  - D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-225 variation BA.
  - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
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