

FEATURES

- Member of the Texas Instruments Widebus™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- B-Port Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Thin-Shrink Small-Outline (DGG) and Plastic Shrink Small-Outline (DL) Packages

NOTE: For tape-and-reel order entry: The DGGR package is abbreviated to GR.

DESCRIPTION

This 12-bit to 24-bit multiplexed D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH162260 is used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing address and data information in microprocessor or bus-interface applications. This device also is useful in memory-interleaving applications.

Three 12-bit I/O ports (A1-A12, 1B1-1B12, and 2B1-2B12) are available for address and/or data transfer. The output-enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OE A}$) inputs control the bus transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A-to-B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

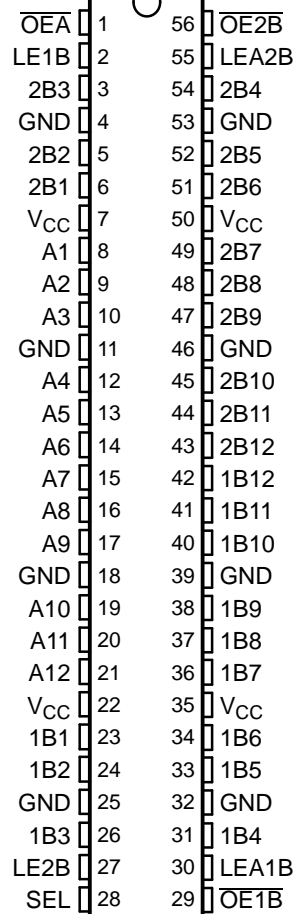
The B outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162260 is characterized for operation from -40°C to 85°C.

**DGG OR DL PACKAGE
(TOP VIEW)**



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SN74ALVCH162260
12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH
WITH 3-STATE OUTPUTS

SCAS570I—MARCH 1996—REVISED AUGUST 2004

FUNCTION TABLES

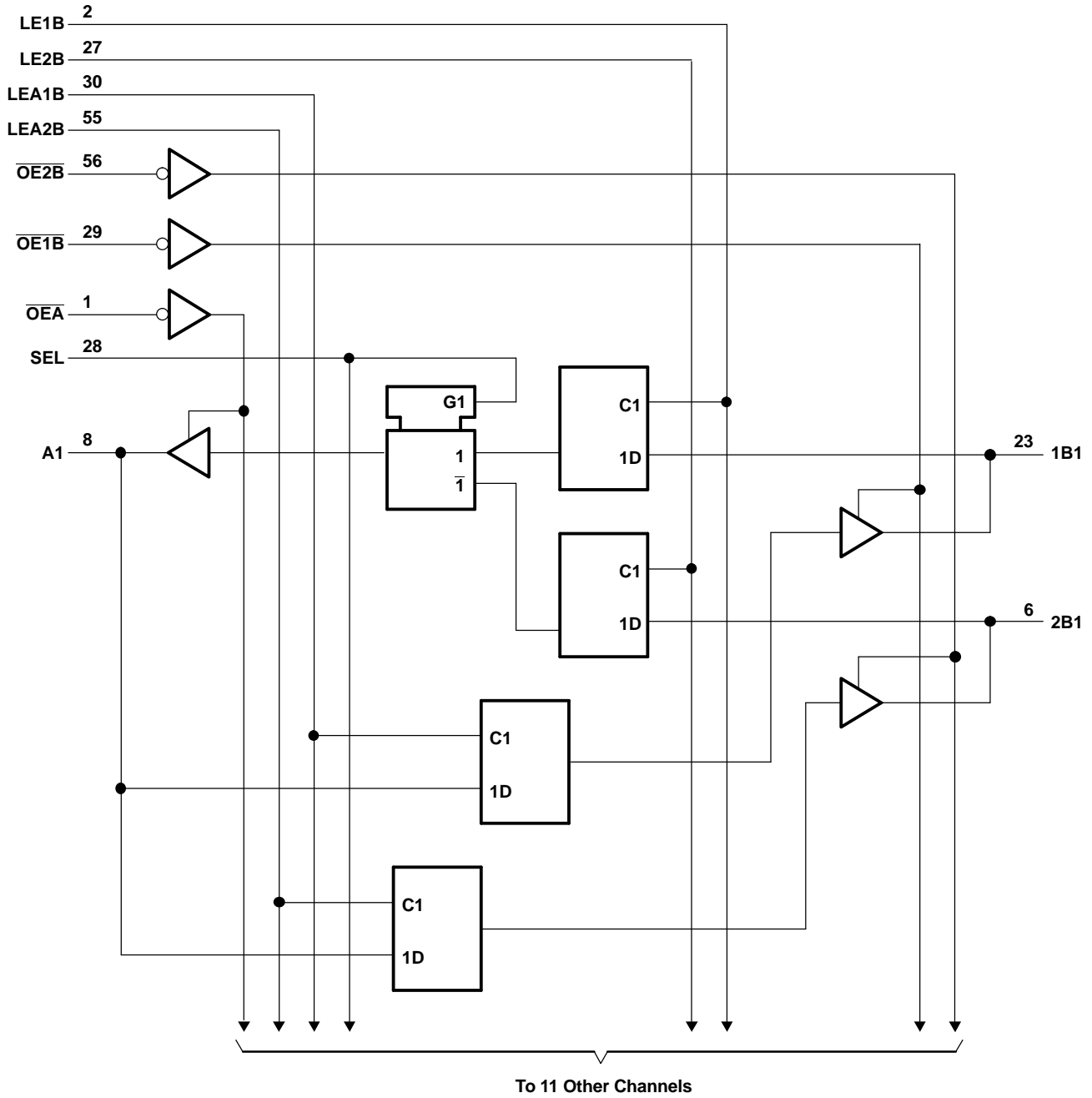
B TO A
($\overline{OE}B = H$)

INPUTS						OUTPUT
1B	2B	SEL	LE1B	LE2B	$\overline{OE}A$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A ₀
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A ₀
X	X	X	X	X	H	Z

A TO B
($\overline{OE}A = H$)

INPUTS					OUTPUTS	
A	LEA1B	LEA2B	$\overline{OE}1B$	$\overline{OE}2B$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	2B ₀
L	H	L	L	L	L	2B ₀
H	L	H	L	L	1B ₀	H
L	L	H	L	L	1B ₀	L
X	L	L	L	L	1B ₀	2B ₀
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

LOGIC DIAGRAM (POSITIVE LOGIC)



SN74ALVCH162260

12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range	Except I/O ports ⁽²⁾		V
		-0.5	4.6	
V_O	Output voltage range ⁽²⁾⁽³⁾	I/O ports ⁽²⁾⁽³⁾		V
		-0.5	$V_{CC} + 0.5$	
I_{IK}	Input clamp current	$V_I < 0$		mA
I_{OK}	Output clamp current	$V_O < 0$		mA
I_O	Continuous output current			mA
	Continuous current through each V_{CC} or GND			mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGG package		°C/W
		DGV package		
		DL package		
T_{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.65	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2	
V_{IL}	Low-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7	
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0.8	
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	v
I_{OH}	High-level output current (A port)	$V_{CC} = 1.65\text{ V}$	-4	mA
		$V_{CC} = 2.3\text{ V}$	-12	
		$V_{CC} = 2.7\text{ V}$	-12	
		$V_{CC} = 3\text{ V}$	-24	
	High-level output current (B port)	$V_{CC} = 1.65\text{ V}$	-2	
		$V_{CC} = 2.3\text{ V}$	-6	
		$V_{CC} = 2.7\text{ V}$	-8	
		$V_{CC} = 3\text{ V}$	-12	
I_{OL}	Low-level output current (A port)	$V_{CC} = 1.65\text{ V}$	4	mA
		$V_{CC} = 2.3\text{ V}$	12	
		$V_{CC} = 2.7\text{ V}$	12	
		$V_{CC} = 3\text{ V}$	24	
	Low-level output current (B port)	$V_{CC} = 1.65\text{ V}$	2	
		$V_{CC} = 2.3\text{ V}$	6	
		$V_{CC} = 2.7\text{ V}$	8	
		$V_{CC} = 3\text{ V}$	12	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
T_A	Operating free-air temperature	-40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74ALVCH162260

12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH

WITH 3-STATE OUTPUTS

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ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	A port	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2			V
		I _{OH} = -4 mA	1.65 V	1.2			
		I _{OH} = -6 mA	2.3 V	2			
		I _{OH} = -12 mA	2.3 V	1.7			
			2.7 V	2.2			
			3 V	2.4			
	I _{OH} = -24 mA	3 V	2				
	B port	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2			
		I _{OH} = -2 mA	1.65 V	1.2			
		I _{OH} = -4 mA	2.3 V	1.9			
		I _{OH} = -6 mA	2.3 V	1.7			
			3 V	2.4			
		I _{OH} = -8 mA	2.7 V	2			
		I _{OH} = -12 mA	3 V	2			
V _{OL}	A port	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
		I _{OL} = 4 mA	1.65 V			0.45	
		I _{OL} = 6 mA	2.3 V			0.4	
		I _{OL} = 12 mA	2.3 V			0.7	
			2.7 V			0.4	
		I _{OL} = 24 mA	3 V			0.55	
	B port	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	
		I _{OL} = 2 mA	1.65 V			0.45	
		I _{OL} = 4 mA	2.3 V			0.4	
		I _{OL} = 6 mA	2.3 V			0.55	
			3 V			0.55	
		I _{OL} = 8 mA	2.7 V			0.6	
		I _{OL} = 12 mA	3 V			0.8	
		I _I	V _I = V _{CC} or GND	3.6 V			
I _{I(hold)}	V _I = 0.58 V	1.65 V	25		μA		
	V _I = 1.07 V		-25				
	V _I = 0.7 V	2.3 V	45				
	V _I = 1.7 V		-45				
	V _I = 0.8 V	3 V	75				
	V _I = 2 V		-75				
	V _I = 0 to 3.6 V ⁽²⁾	3.6 V	±500				
I _{OZ} ⁽³⁾	V _O = V _{CC} or GND	3.6 V			±10	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			40	μA	
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μA	
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V	3.5		pF	
C _{io}	A or B ports	V _O = V _{CC} or GND	3.3 V	4.5		pF	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

		$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	(1)		150		150		150		MHz
t_w	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	(1)		3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B high or low	(1)		1.4		1.1		1.1		ns
t_h	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B high or low	(1)		1.6		1.9		1.5		ns

(1) This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			(1)		150		150		150		MHz
t_{pd}	A	B	(1)		1	5.9	5.8		1.2	4.9	ns
	B	A	(1)		1	5.7	5.1		1.2	4.3	
	LE	A	(1)		1	5.6	5.2		1	4.4	
		B	(1)		1	6.1	5.9		1	5	
t_{en}	$\overline{\text{OE}}$	A	(1)		1	6.7	6.4		1	5.4	ns
		B	(1)		1	7.2	7.1		1	6	
t_{dis}	$\overline{\text{OE}}$	A	(1)		1	5.7	5		1.3	4.6	ns
		B	(1)		1	6.2	5.5		1.3	5.1	

(1) This information was not available at the time of publication.

OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	All outputs enabled	(1)	37	41	pF
		All outputs disabled	(1)	4	7	

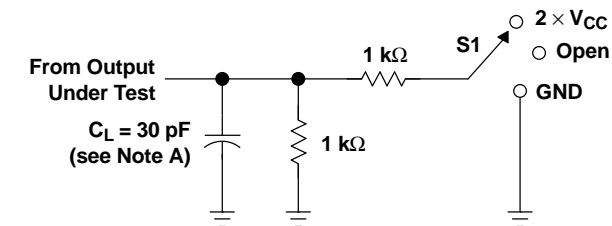
(1) This information was not available at the time of publication.

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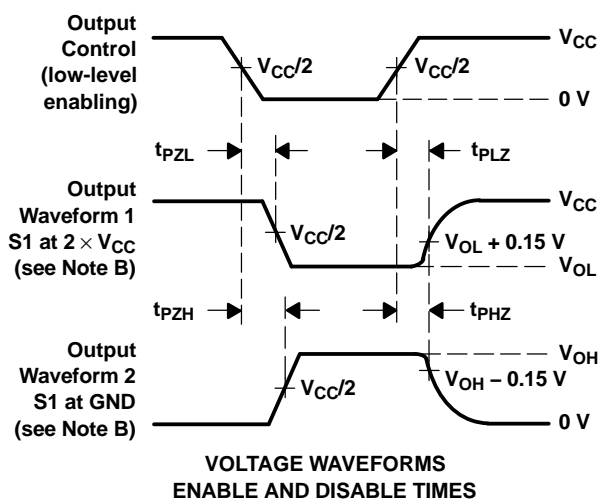
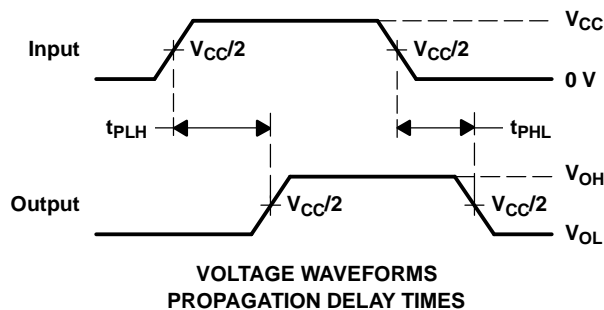
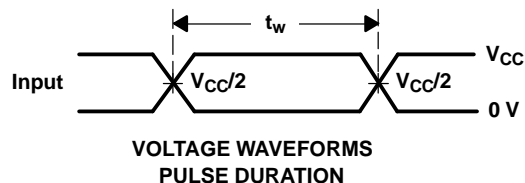
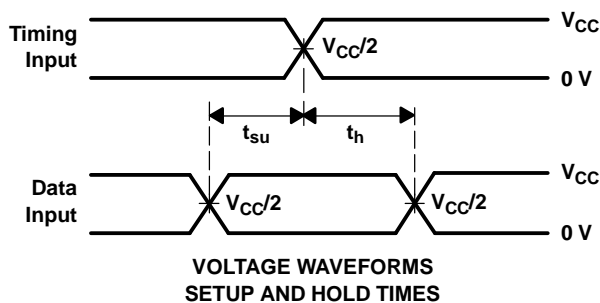
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V}$



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

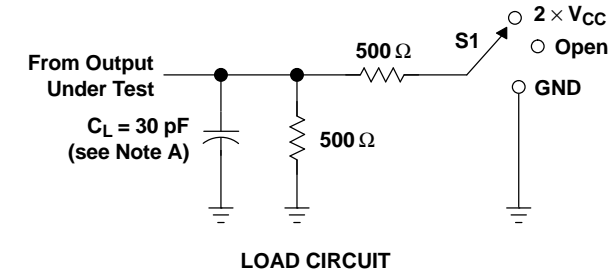


- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

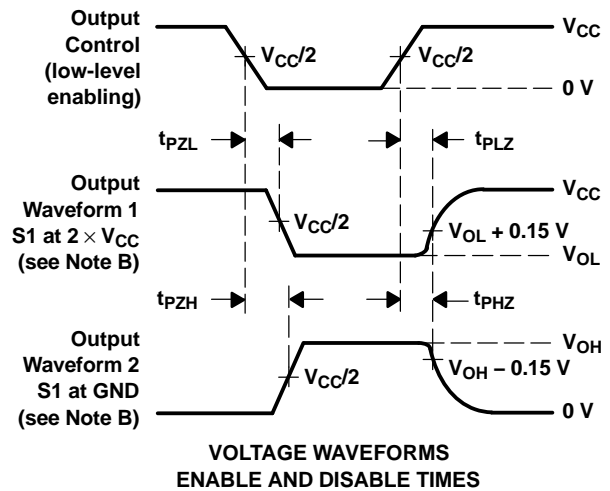
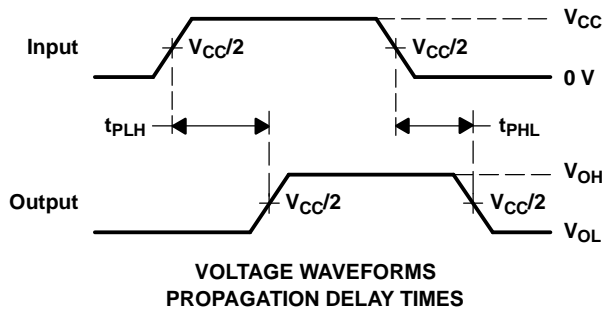
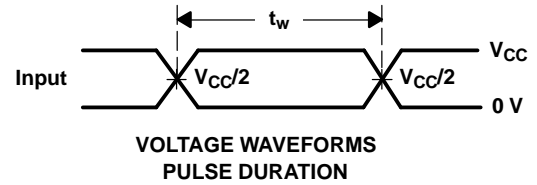
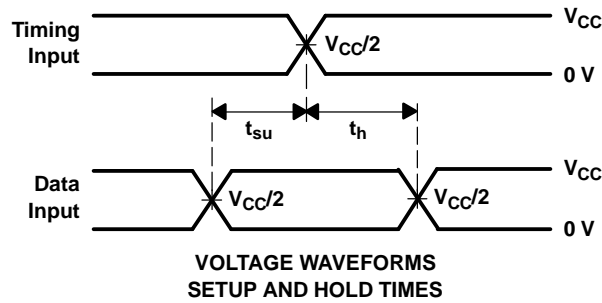
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 \times V_{CC}
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
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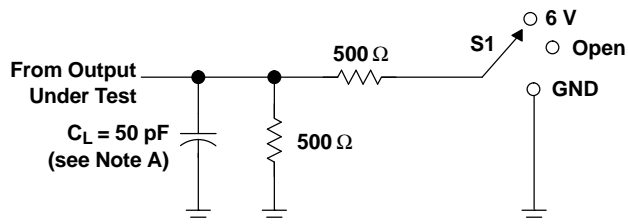
Figure 2. Load Circuit and Voltage Waveforms

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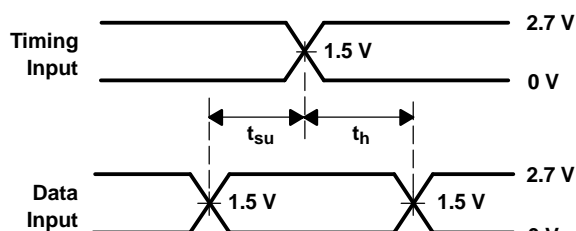
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V}$ AND $3.3\text{ V} \pm 0.3\text{ V}$

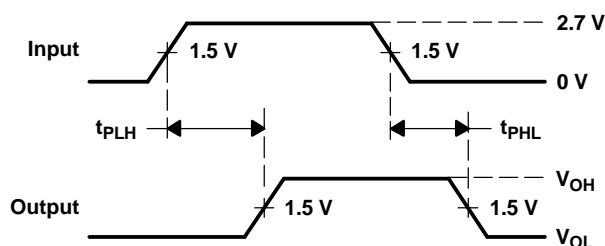


LOAD CIRCUIT

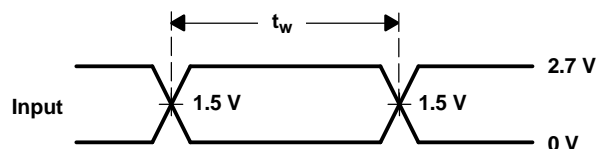
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



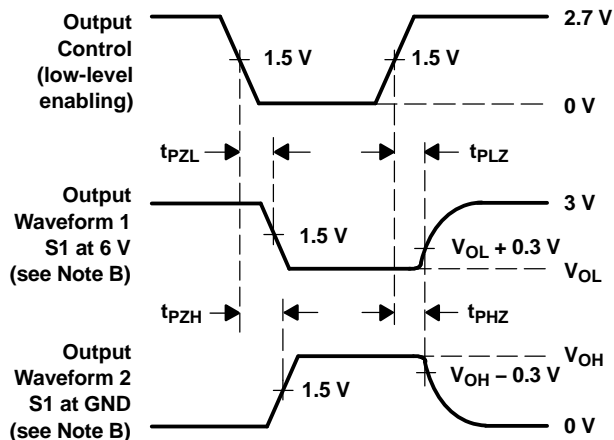
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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