

FEATURES

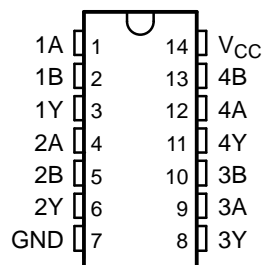
- Operates From 1.65-V to 3.6-V V_{CC}
- Max t_{pd} of 2.9 ns at 3.3-V V_{CC}
- ± 24 -mA Output Drive at 3.3-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

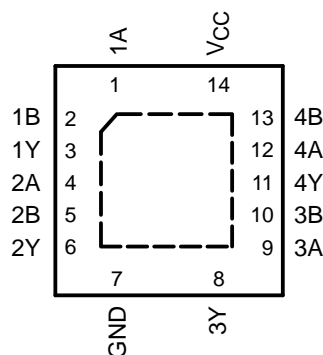
This quadruple 2-input positive-AND gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The device performs the Boolean function $Y = A \cdot B$ or $Y = \overline{A + B}$ in positive logic.

D, DGV, NS, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



ORDERING INFORMATION

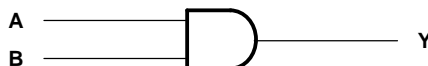
T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN - RGY	Tape and reel	SN74ALVC08RGYR	VA08
	SOIC - D	Tube	SN74ALVC08D	ALVC08
		Tape and reel	SN74ALVC08DR	
	SOP - NS	Tape and reel	SN74ALVC08NSR	ALVC08
	TSSOP - PW	Tape and reel	SN74ALVC08PWR	VA08
TVSOP - DGV	Tape and reel	SN74ALVC08DGVR	VA08	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each gate)

INPUTS		OUTPUT Y
A	B	
H	H	H
L	X	L
X	L	L

LOGIC DIAGRAM, EACH GATE (POSITIVE LOGIC)



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SN74ALVC08 QUADRUPLE 2-INPUT POSITIVE-AND GATE

SCES101H–JULY 1997–REVISED JULY 2004

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	-0.5	4.6	V
V_O	Output voltage range ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current		±50	mA
	Continuous current through V_{CC} or GND		±100	mA
θ_{JA}	Package thermal impedance	D package ⁽⁴⁾	86	°C/W
		DGV package ⁽⁴⁾	127	
		NS package ⁽⁴⁾	76	
		PW package ⁽⁴⁾	113	
		RGY package ⁽⁵⁾	47	
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V, maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.65	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2	
V_{IL}	Low-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7	
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0.8	
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65\text{ V}$	-4	mA
		$V_{CC} = 2.3\text{ V}$	-12	
		$V_{CC} = 2.7\text{ V}$	-12	
		$V_{CC} = 3\text{ V}$	-24	
I_{OL}	Low-level output current	$V_{CC} = 1.65\text{ V}$	4	mA
		$V_{CC} = 2.3\text{ V}$	12	
		$V_{CC} = 2.7\text{ V}$	12	
		$V_{CC} = 3\text{ V}$	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		5	ns/V
T_A	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{OH}	I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2			V	
	I _{OH} = -4 mA	1.65 V	1.2				
	I _{OH} = -6 mA	2.3 V	2				
	I _{OH} = -12 mA		2.3 V	1.7			
			2.7 V	2.2			
			3 V	2.4			
I _{OH} = -24 mA	3 V	2					
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V	
	I _{OL} = 4 mA	1.65 V			0.45		
	I _{OL} = 6 mA	2.3 V			0.4		
	I _{OL} = 12 mA		2.3 V				0.7
			2.7 V				0.4
	I _{OL} = 24 mA	3 V			0.55		
I _I	V _I = V _{CC} or GND	3.6 V			±5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			10	μA	
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			750	μA	
C _i	V _I = V _{CC} or GND	3.3 V		4.5		pF	

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

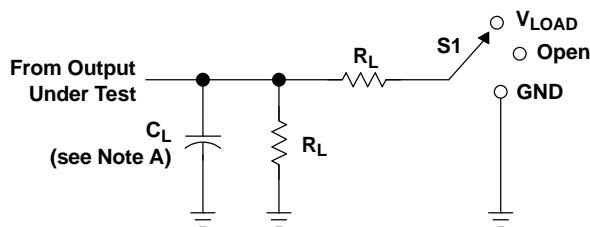
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	Y	1.2	5.3	1	3.2		3	1.2	2.9	ns

OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
		TYP	TYP	TYP	
C _{pd} Power dissipation capacitance per gate	C _L = 0 pF, f = 10 MHz	24	25	26	pF

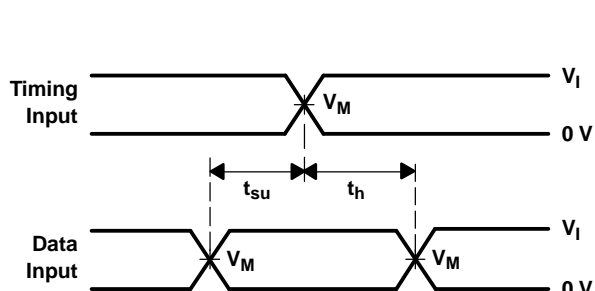
PARAMETER MEASUREMENT INFORMATION



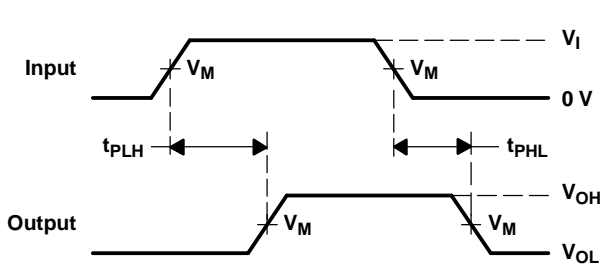
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

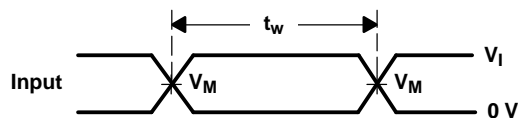
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8 V \pm 0.15 V$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5 V \pm 0.2 V$	V_{CC}	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3 V \pm 0.3 V$	2.7 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



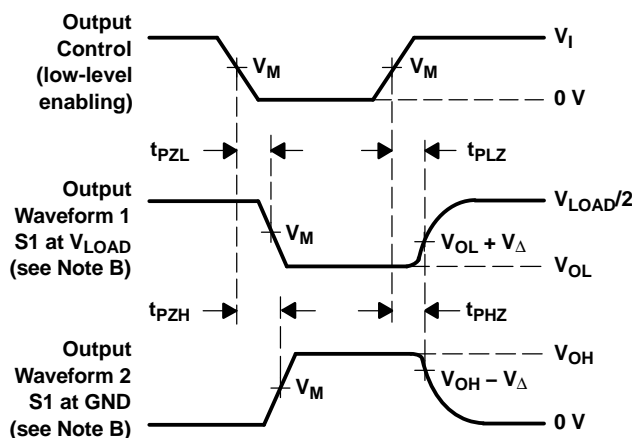
**VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
 PULSE DURATION**



**VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES**

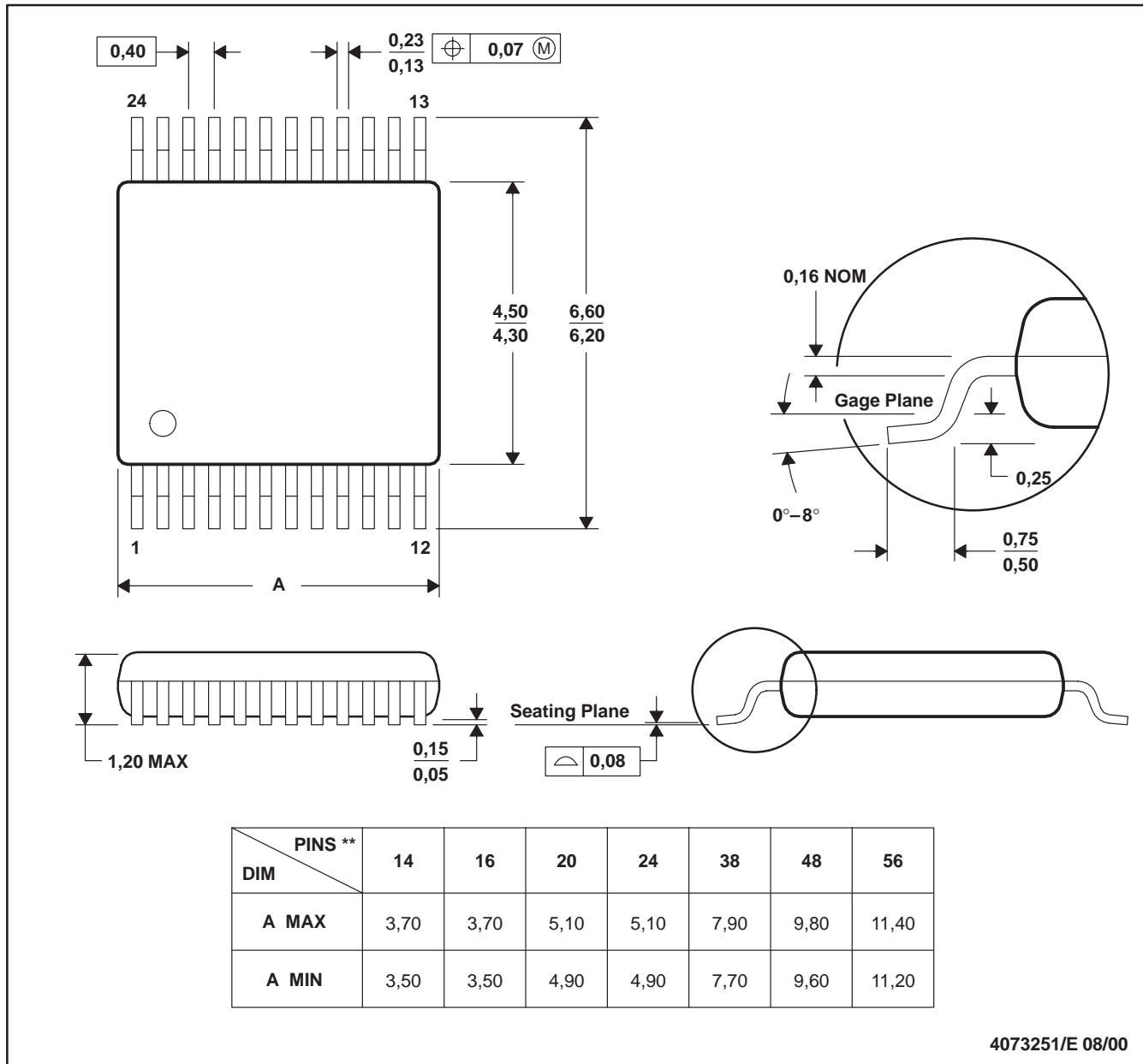
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

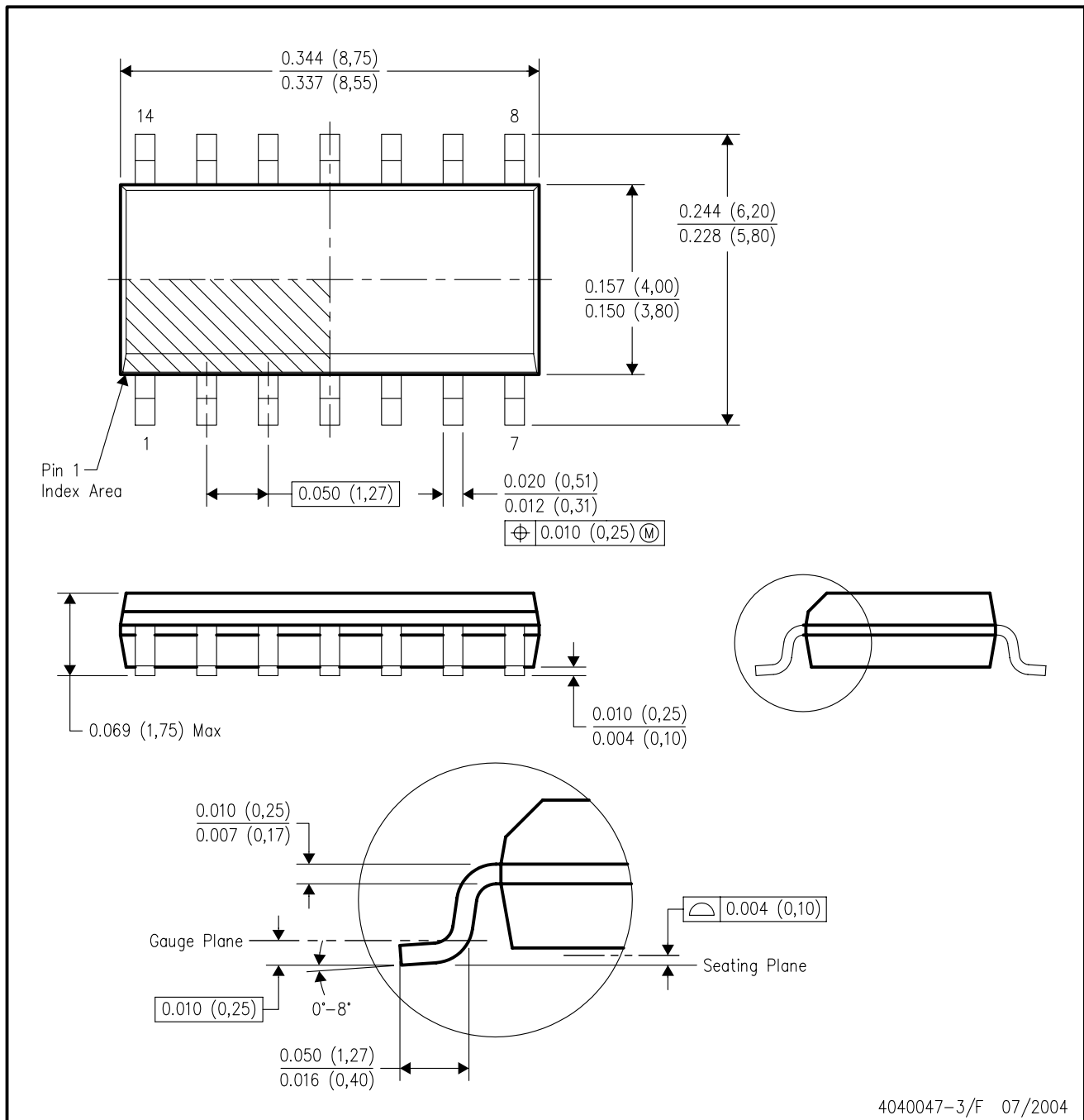
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

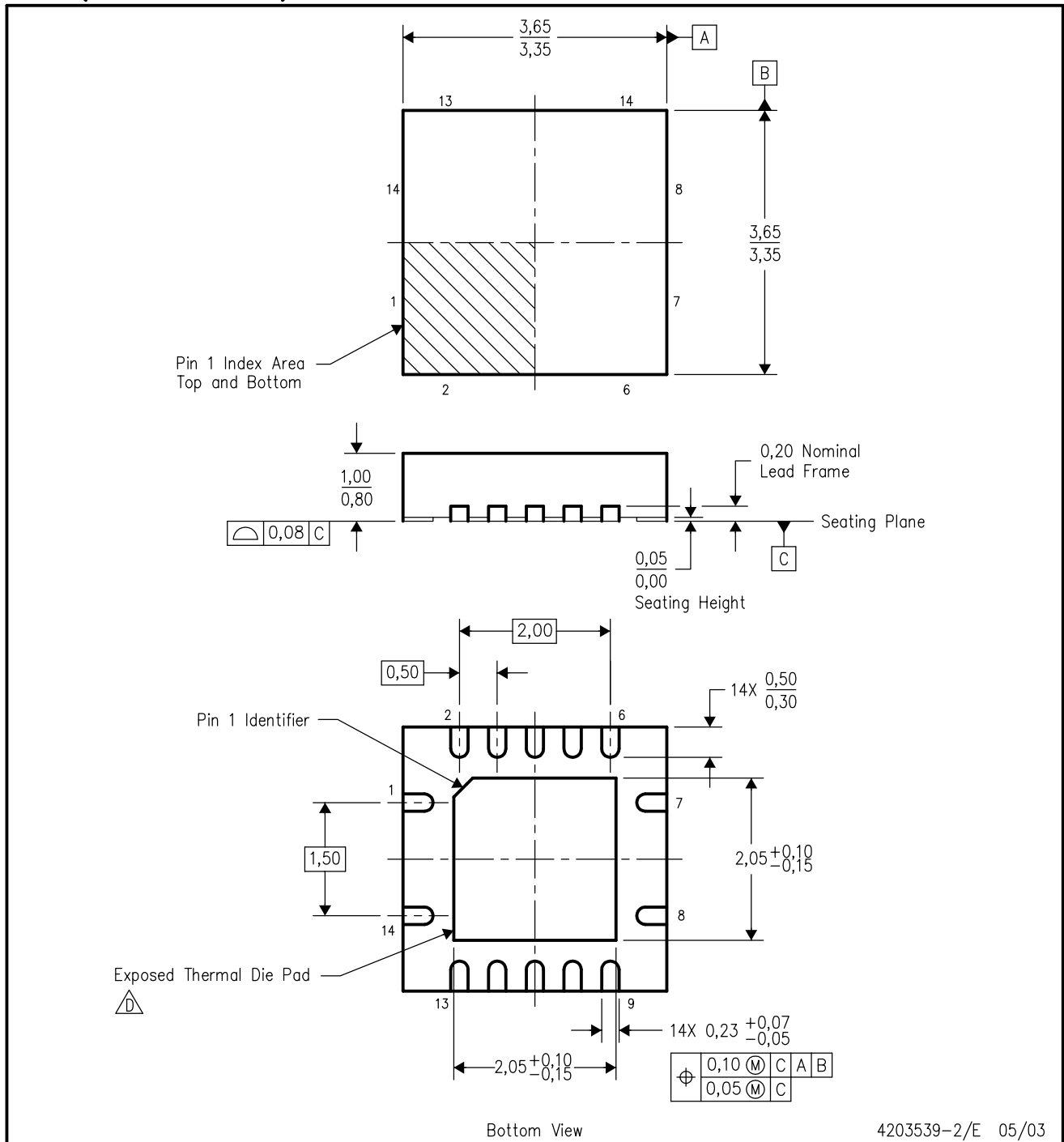
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



Bottom View

4203539-2/E 05/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - △ The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - E. Package complies to JEDEC MO-241 variation BA.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265