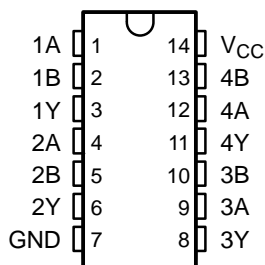


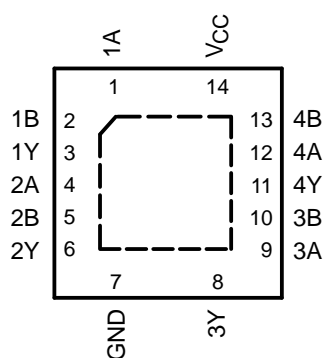
**FEATURES**

- Operates From 1.65 V to 3.6 V
- Max  $t_{pd}$  of 3 ns at 3.3 V
- $\pm 24$ -mA Output Drive at 3.3 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

**D, DGV, NS, OR PW PACKAGE (TOP VIEW)**



**RGY PACKAGE (TOP VIEW)**



**DESCRIPTION/ORDERING INFORMATION**

This quadruple 2-input positive-NAND gate is designed for 1.65-V to 3.6-V  $V_{CC}$  operation. The SN74ALVC00 performs the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

**ORDERING INFORMATION**

| $T_A$         | PACKAGE <sup>(1)</sup> |                | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|----------------|-----------------------|------------------|
| -40°C to 85°C | QFN - RGY              | Tape and reel  | SN74ALVC00RGYR        | VA00             |
|               | SOIC - D               | Tube           | SN74ALVC00D           | ALVC00           |
|               |                        | Tape and reel  | SN74ALVC00DR          |                  |
|               | SOP - NS               | Tape and reel  | SN74ALVC00NSR         | ALVC00           |
|               | TSSOP - PW             | Tape and reel  | SN74ALVC00PWR         | VA00             |
| TVSOP - DGV   | Tape and reel          | SN74ALVC00DGVR | VA00                  |                  |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE (each gate)**

| INPUTS |   | OUTPUT<br>Y |
|--------|---|-------------|
| A      | B |             |
| H      | H | L           |
| L      | X | H           |
| X      | L | H           |

**LOGIC DIAGRAM, EACH GATE (POSITIVE LOGIC)**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN74ALVC00 QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCES115G–JULY 1997–REVISED AUGUST 2004

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|               |  | MIN                        | MAX            | UNIT |
|---------------|--|----------------------------|----------------|------|
| $V_{CC}$      | Supply voltage range                       | -0.5                       | 4.6            | V    |
| $V_I$         | Input voltage range <sup>(2)</sup>         | -0.5                       | 4.6            | V    |
| $V_O$         | Output voltage range <sup>(2)(3)</sup>     | -0.5                       | $V_{CC} + 0.5$ | V    |
| $I_{IK}$      | Input clamp current                        | $V_I < 0$                  | -50            | mA   |
| $I_{OK}$      | Output clamp current                       | $V_O < 0$                  | -50            | mA   |
| $I_O$         | Continuous output current                  |                            | $\pm 50$       | mA   |
|               | Continuous current through $V_{CC}$ or GND |                            | $\pm 100$      | mA   |
| $\theta_{JA}$ | Package thermal impedance                  | D package <sup>(4)</sup>   | 86             | °C/W |
|               |  | DGV package <sup>(4)</sup> | 127            |      |
|               |  | NS package <sup>(4)</sup>  | 76             |      |
|               |  | PW package <sup>(4)</sup>  | 113            |      |
|               |  | RGY package <sup>(5)</sup> | 47             |      |
| $T_{stg}$     | Storage temperature range                  | -65                        | 150            | °C   |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 4.6 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

|                     |                                    | MIN                                       | MAX                  | UNIT |
|---------------------|------------------------------------|---|----------------------|------|
| $V_{CC}$            | Supply voltage                     | 1.65                                      | 3.6                  | V    |
| $V_{IH}$            | High-level input voltage           | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | $0.65 \times V_{CC}$ | V    |
|                     |                                    | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$   | 1.7                  |      |
|                     |                                    | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$   | 2                    |      |
| $V_{IL}$            | Low-level input voltage            | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | $0.35 \times V_{CC}$ | V    |
|                     |                                    | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$   | 0.7                  |      |
|                     |                                    | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$   | 0.8                  |      |
| $V_I$               | Input voltage                      | 0   | 3.6                  | V    |
| $V_O$               | Output voltage                     | 0   | $V_{CC}$             | V    |
| $I_{OH}$            | High-level output current          | $V_{CC} = 1.65\text{ V}$                  | -4                   | mA   |
|                     |                                    | $V_{CC} = 2.3\text{ V}$                   | -12                  |      |
|                     |                                    | $V_{CC} = 2.7\text{ V}$                   | -12                  |      |
|                     |                                    | $V_{CC} = 3\text{ V}$                     | -24                  |      |
| $I_{OL}$            | Low-level output current           | $V_{CC} = 1.65\text{ V}$                  | 4                    | mA   |
|                     |                                    | $V_{CC} = 2.3\text{ V}$                   | 12                   |      |
|                     |                                    | $V_{CC} = 2.7\text{ V}$                   | 12                   |      |
|                     |                                    | $V_{CC} = 3\text{ V}$                     | 24                   |      |
| $\Delta t/\Delta v$ | Input transition rise or fall rate |   | 5                    | ns/V |
| $T_A$               | Operating free-air temperature     | -40                                       | 85                   | °C   |

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                | TEST CONDITIONS  | V <sub>CC</sub> | MIN                   | TYP <sup>(1)</sup> | MAX  | UNIT |     |
|--------------------------|--|-----------------|-----------------------|--------------------|------|------|-----|
| V <sub>OH</sub>          | I <sub>OH</sub> = -100 μA  | 1.65 V to 3.6 V | V <sub>CC</sub> - 0.2 |                    |      | V    |     |
|                          | I <sub>OH</sub> = -4 mA  | 1.65 V          | 1.2                   |                    |      |      |     |
|                          | I <sub>OH</sub> = -6 mA  | 2.3 V           | 2                     |                    |      |      |     |
|                          | I <sub>OH</sub> = -12 mA   |                 | 2.3 V                 | 1.7                |      |      |     |
|                          |  |                 | 2.7 V                 | 2.2                |      |      |     |
|                          |  |                 | 3 V                   | 2.4                |      |      |     |
| I <sub>OH</sub> = -24 mA | 3 V  | 2               |                       |                    |      |      |     |
| V <sub>OL</sub>          | I <sub>OL</sub> = 100 μA   | 1.65 V to 3.6 V |                       |                    | 0.2  | V    |     |
|                          | I <sub>OL</sub> = 4 mA   | 1.65 V          |                       |                    | 0.45 |      |     |
|                          | I <sub>OL</sub> = 6 mA   | 2.3 V           |                       |                    | 0.4  |      |     |
|                          | I <sub>OL</sub> = 12 mA  |                 | 2.3 V                 |                    |      |      | 0.7 |
|                          |  |                 | 2.7 V                 |                    |      |      | 0.4 |
|                          | I <sub>OL</sub> = 24 mA  | 3 V             |                       |                    | 0.55 |      |     |
| I <sub>I</sub>           | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.6 V           |                       |                    | ±5   | μA   |     |
| I <sub>CC</sub>          | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                  | 3.6 V           |                       |                    | 10   | μA   |     |
| ΔI <sub>CC</sub>         | One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND | 3 V to 3.6 V    |                       |                    | 750  | μA   |     |
| C <sub>i</sub>           | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           |                       | 4.5                |      | pF   |     |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

### SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

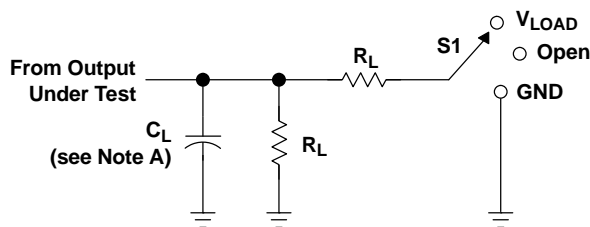
| PARAMETER       | FROM (INPUT) | TO (OUTPUT) | V <sub>CC</sub> = 1.8 V ± 0.15 V |     | V <sub>CC</sub> = 2.5 V ± 0.2 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V ± 0.3 V |     | UNIT |
|-----------------|--------------|-------------|----------------------------------|-----|---------------------------------|-----|-------------------------|-----|---------------------------------|-----|------|
|                 |              |             | MIN                              | MAX | MIN                             | MAX | MIN                     | MAX | MIN                             | MAX |      |
| t <sub>pd</sub> | A or B       | Y           | 1                                | 4.4 | 1                               | 2.8 | 3.2                     |     | 1                               | 3   | ns   |

### OPERATING CHARACTERISTICS

T<sub>A</sub> = 25°C

| PARAMETER       | TEST CONDITIONS                        | V <sub>CC</sub> = 1.8 V           | V <sub>CC</sub> = 2.5 V | V <sub>CC</sub> = 3.3 V | UNIT |    |
|-----------------|--|-----------------------------------|-------------------------|-------------------------|------|----|
|                 |  | TYP                               | TYP                     | TYP                     |      |    |
| C <sub>pd</sub> | Power dissipation capacitance per gate | C <sub>L</sub> = 0 pF, f = 10 MHz | 20                      | 21                      | 23   | pF |

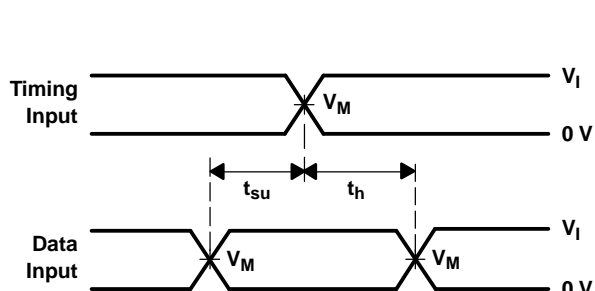
**PARAMETER MEASUREMENT INFORMATION**



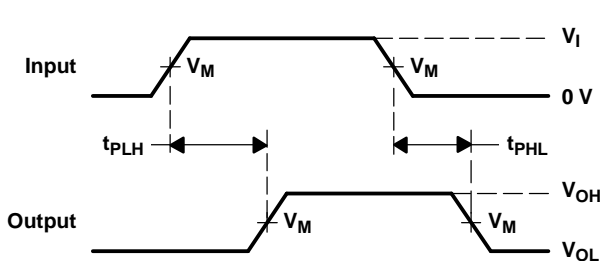
**LOAD CIRCUIT**

| TEST              | S1         |
|-------------------|------------|
| $t_{pd}$          | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

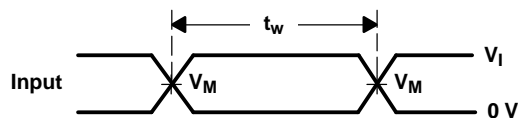
| $V_{CC}$                         | INPUT    |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| 2.7 V                            | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |



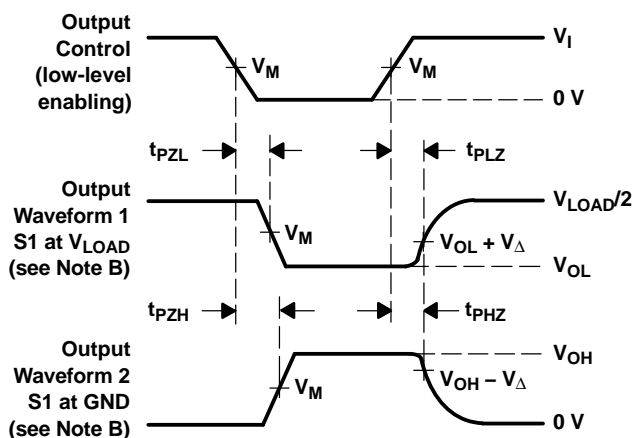
**VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
 PULSE DURATION**



**VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74ALVC00D      | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ALVC00                  | <a href="#">Samples</a> |
| SN74ALVC00DE4    | ACTIVE        | SOIC         | D               | 14   | 50          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ALVC00                  | <a href="#">Samples</a> |
| SN74ALVC00DGVR   | ACTIVE        | TVSOP        | DGV             | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | VA00                    | <a href="#">Samples</a> |
| SN74ALVC00DR     | ACTIVE        | SOIC         | D               | 14   | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ALVC00                  | <a href="#">Samples</a> |
| SN74ALVC00NSR    | ACTIVE        | SO           | NS              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ALVC00                  | <a href="#">Samples</a> |
| SN74ALVC00PWR    | ACTIVE        | TSSOP        | PW              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | VA00                    | <a href="#">Samples</a> |
| SN74ALVC00PWRE4  | ACTIVE        | TSSOP        | PW              | 14   | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | VA00                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74ALVC00 :**

- Automotive: [SN74ALVC00-Q1](#)
- Enhanced Product: [SN74ALVC00-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

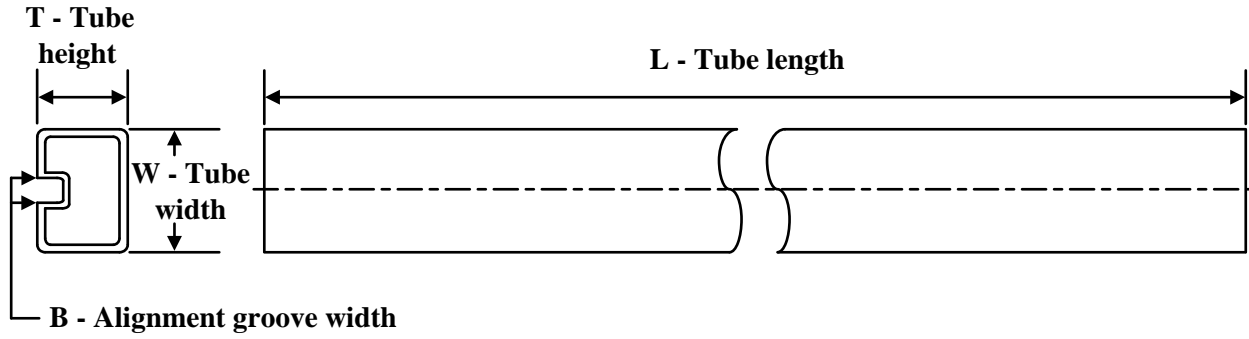

\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALVC00DGVR | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74ALVC00DR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74ALVC00NSR  | SO           | NS              | 14   | 2000 | 330.0              | 16.4               | 8.2     | 10.5    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74ALVC00PWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALVC00DGVR | TVSOP        | DGV             | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74ALVC00DR   | SOIC         | D               | 14   | 2500 | 356.0       | 356.0      | 35.0        |
| SN74ALVC00NSR  | SO           | NS              | 14   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74ALVC00PWR  | TSSOP        | PW              | 14   | 2000 | 356.0       | 356.0      | 35.0        |

**TUBE**


\*All dimensions are nominal

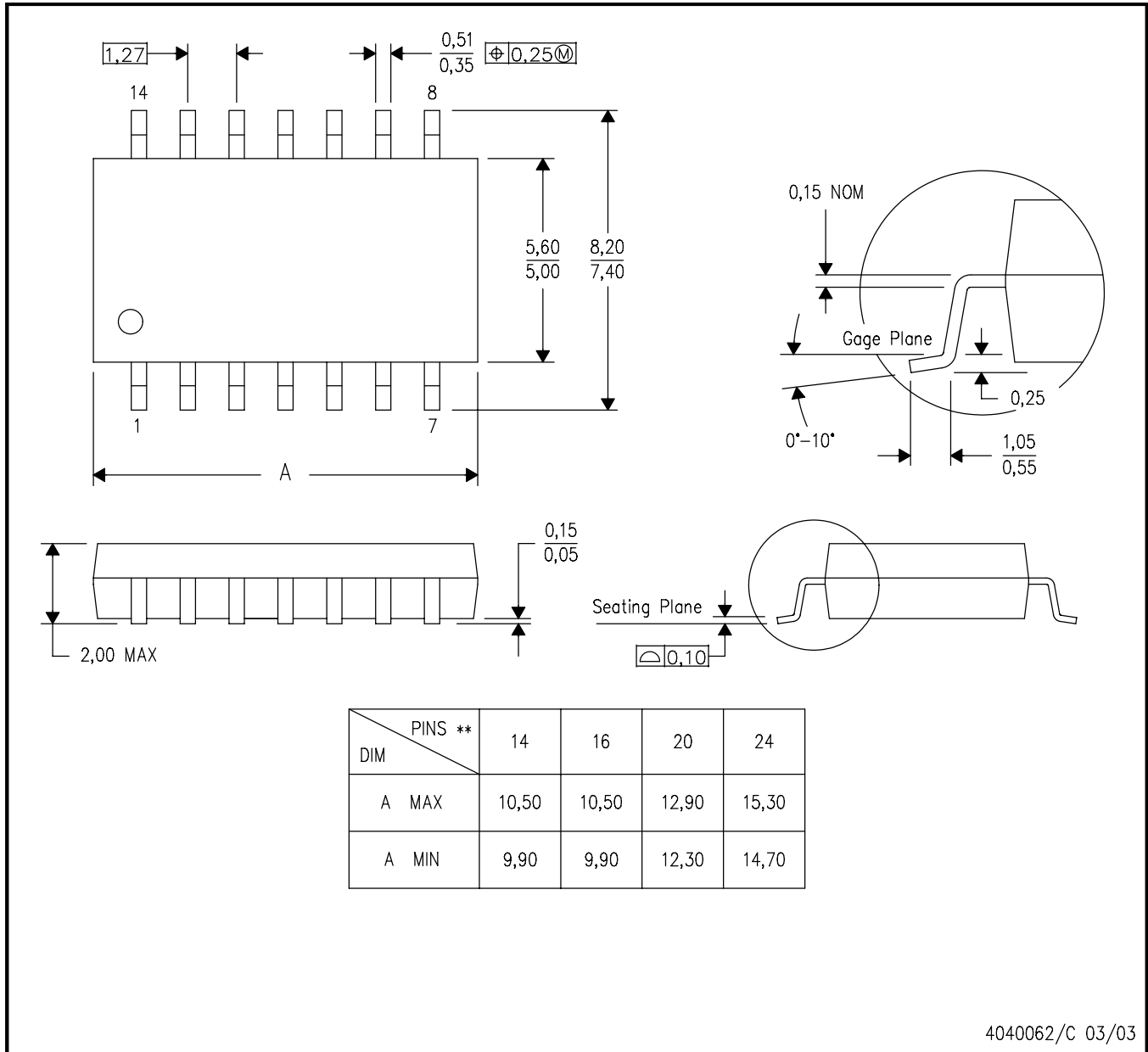
| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74ALVC00D   | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74ALVC00DE4 | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

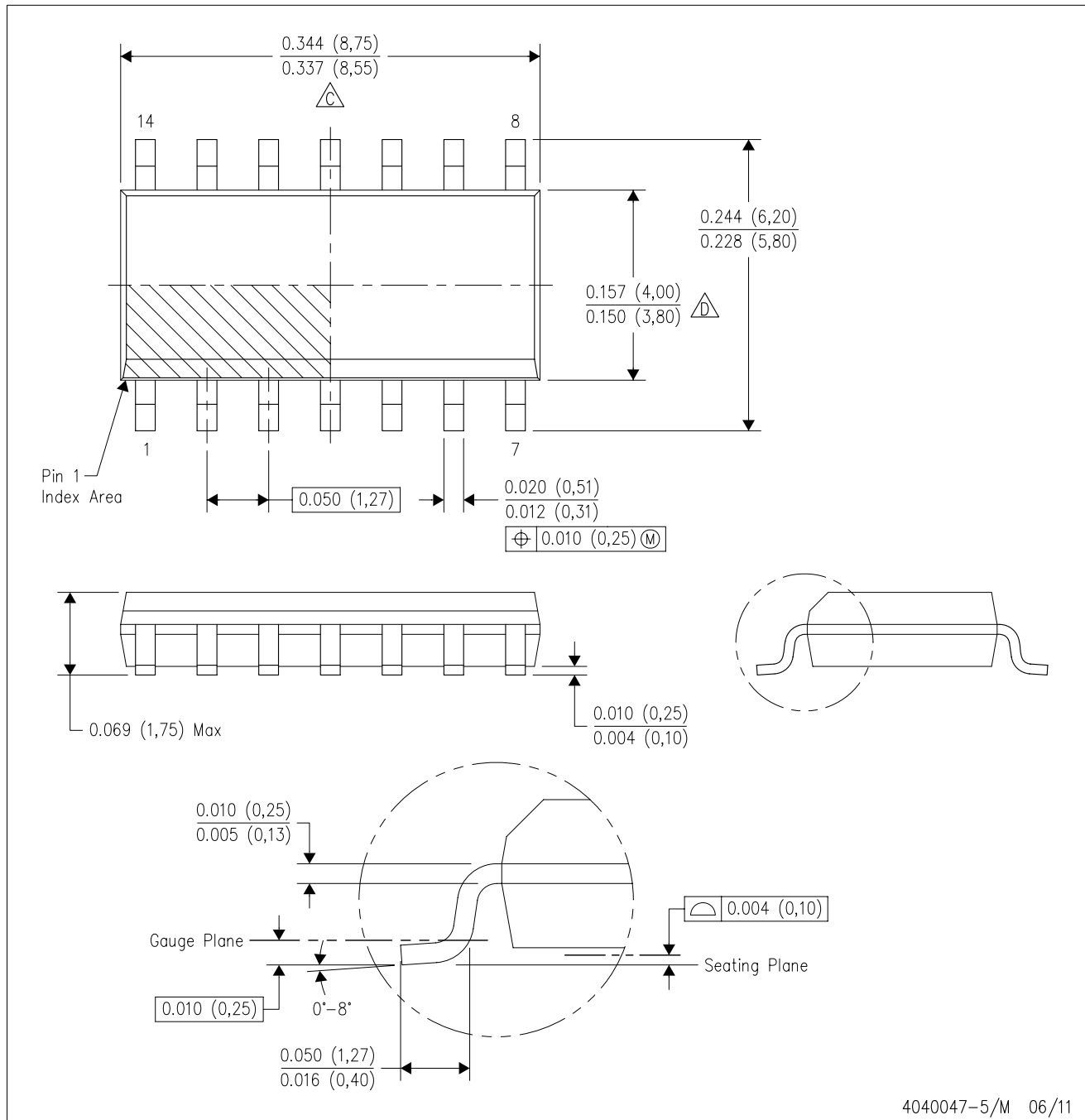


4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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