

# SN74ALS994

## 10-BIT D-TYPE TRANSPARENT READ-BACK LATCH

SDAS237A – OCTOBER 1984 – REVISED JANUARY 1995

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- True Logic Outputs
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

### description

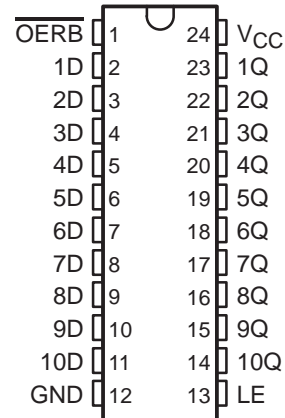
This 10-bit latch is designed specifically for storing the contents of the input data bus and providing the capability of reading back the stored data onto the input data bus.

The ten latches are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs.

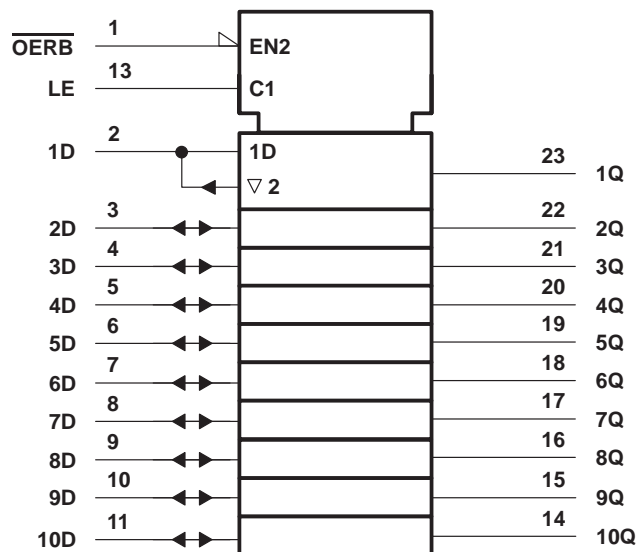
Read back is provided through the output-enable ( $\overline{\text{OERB}}$ ) input. When  $\overline{\text{OERB}}$  is taken low, the data present at the output of the data latches passes back onto the input data bus. When  $\overline{\text{OERB}}$  is taken high, the output of the data latches is isolated from the D inputs.  $\overline{\text{OERB}}$  does not affect the internal operation of the latches; however, precautions should be taken to avoid a bus conflict.

The SN74ALS994 is characterized for operation from 0°C to 70°C.

DW OR NT PACKAGE  
(TOP VIEW)



### logic symbol†

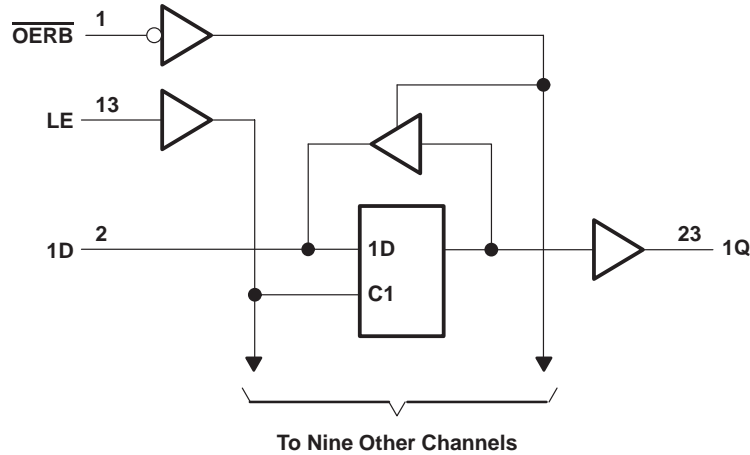


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

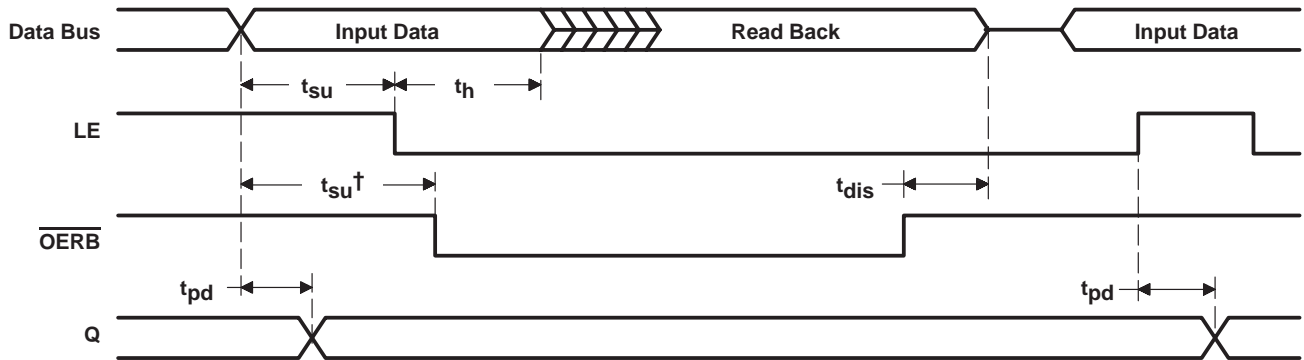
# SN74ALS994 10-BIT D-TYPE TRANSPARENT READ-BACK LATCH

SDAS237A – OCTOBER 1984 – REVISED JANUARY 1995

## logic diagram (positive logic)



## timing diagram



† This setup time ensures that the read-back circuit will not create a conflict on the input data bus.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$ ( $\overline{OERB}$ and LE)	7 V
Voltage applied to D inputs	5.5 V
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# SN74ALS994

## 10-BIT D-TYPE TRANSPARENT READ-BACK LATCH

SDAS237A – OCTOBER 1984 – REVISED JANUARY 1995

### recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current	Q		-2.6	mA
		D		-0.4	
$I_{OL}$	Low-level output current	Q		24	mA
		D		8	
$t_w$	Pulse duration, LE high	10			ns
$t_{su}$	Setup time	Data before LE↓	10		ns
		Data before $\overline{OERB}$ ↓†	10		
$t_h$	Hold time, data after LE↓	5			ns
$T_A$	Operating free-air temperature	0		70	°C

† This setup time ensures that the read-back circuit will not create a conflict on the input data bus.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	All outputs	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ ,	$I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			V
	Q	$V_{CC} = 4.5\text{ V}$ ,	$I_{OH} = -2.6\text{ mA}$	2.4	3.2		
$V_{OL}$	D	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$	0.25	0.4	V	
			$I_{OL} = 8\text{ mA}$	0.35	0.5		
	Q	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$	0.25	0.4		
			$I_{OL} = 24\text{ mA}$	0.35	0.5		
$I_I$	$\overline{OERB}$ , LE	$V_{CC} = 5.5\text{ V}$	$V_I = 7\text{ V}$		0.1	mA	
	D inputs		$V_I = 5.5\text{ V}$		0.1		
$I_{IH}$	$\overline{OERB}$ , LE	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$		20	$\mu\text{A}$	
	D inputs§				20		
$I_{IL}$	$\overline{OERB}$ , LE	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$		-0.1	mA	
	D inputs§				-0.1		
$I_{O}^{\parallel}$		$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.25\text{ V}$	-30		-112	mA
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ ,	$\overline{OERB}$ high	Q outputs high	30	50	mA
			Q outputs low		52	82	

‡ All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ For I/O ports ( $Q_A$  thru  $Q_H$ ), the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



# SN74ALS994

## 10-BIT D-TYPE TRANSPARENT READ-BACK LATCH

SDAS237A – OCTOBER 1984 – REVISED JANUARY 1995

### switching characteristics (see Figure 1)

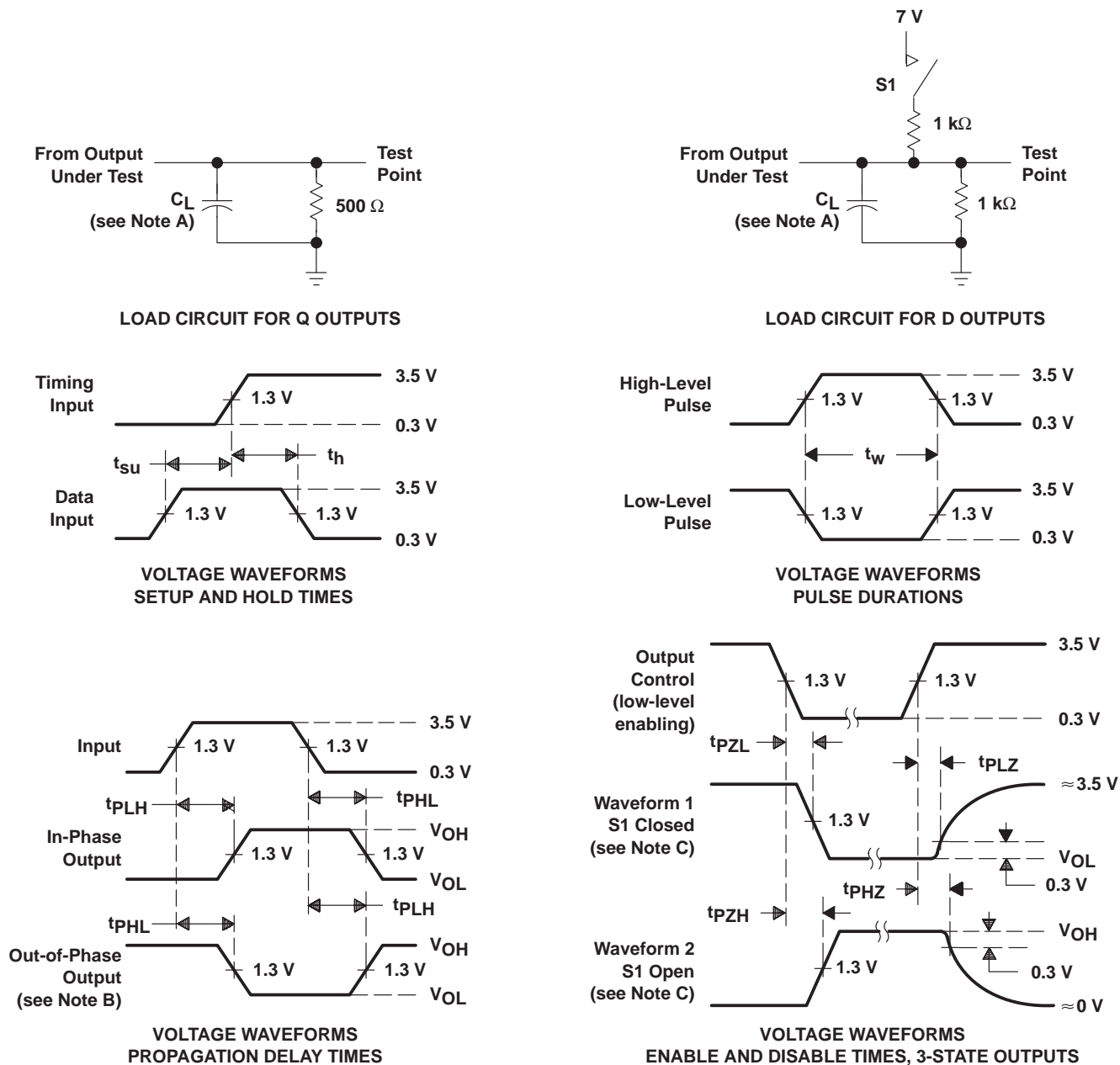
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, T <sub>A</sub> = MIN to MAX†		UNIT
			MIN	MAX	
t <sub>PLH</sub>	D	Q	3	14	ns
t <sub>PHL</sub>			4	18	
t <sub>PLH</sub>	LE	Q	6	21	ns
t <sub>PHL</sub>			8	27	
t <sub>en</sub> ‡	$\overline{\text{OERB}}$	D	4	21	ns
t <sub>dis</sub> §			2	16	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ t<sub>en</sub> = t<sub>PZH</sub> or t<sub>PZL</sub>

§ t<sub>dis</sub> = t<sub>PHZ</sub> or t<sub>PLZ</sub>

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. When measuring propagation delay times of 3-state outputs, switch S1 is open.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.

**Figure 1. Load Circuits and Voltage Waveforms**



## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.