

SN54ALS873B, SN54AS873A, SN74ALS873B, SN74AS873A DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS036D – APRIL 1982 – REVISED AUGUST 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

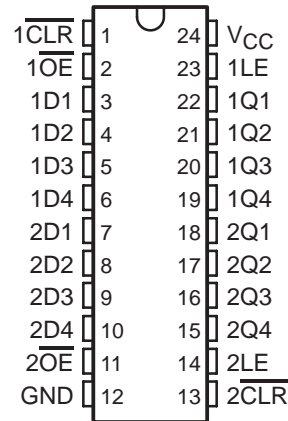
description

These dual 4-bit D-type latches feature 3-state outputs designed specifically for bus driving. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

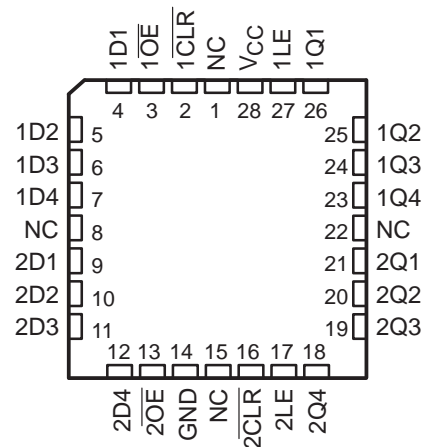
The dual 4-bit latches are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs in true form, according to the function table. When LE is low, the outputs are latched. When the clear (CLR) input goes low, the Q outputs go low independently of LE. The outputs are in the high-impedance state when the output-enable (\overline{OE}) input is at a high logic level.

The SN54ALS873B and SN54AS873A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS873B and SN74AS873A are characterized for operation from 0°C to 70°C .

SN54ALS873B, SN54AS873A . . . JT PACKAGE
SN74ALS873B, SN74AS873A . . . DW OR NT PACKAGE
(TOP VIEW)



SN54ALS873B, SN54AS873A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each latch)

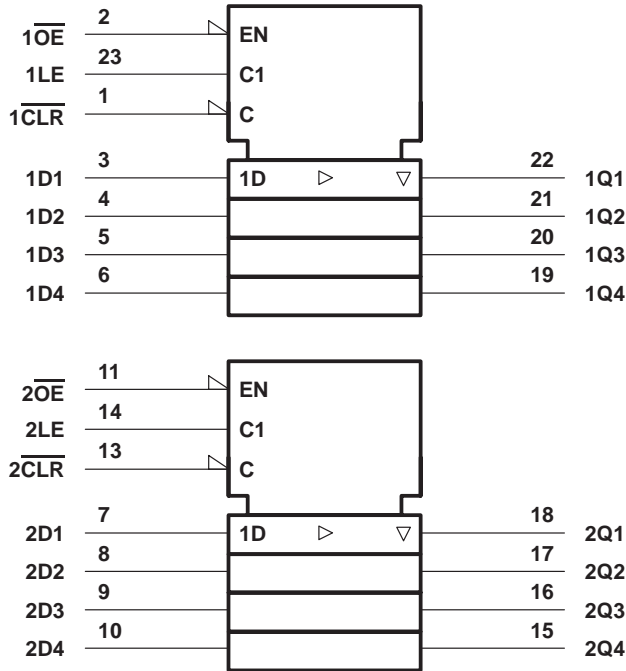
| INPUTS | | | | OUTPUT Q |
|-----------------|------------------|----|---|-------------|
| \overline{OE} | \overline{CLR} | LE | D | |
| L | L | X | X | L |
| L | H | H | H | H |
| L | H | H | L | L |
| L | H | L | X | Q_0 |
| H | X | X | X | Z |

SN54ALS873B, SN54AS873A, SN74ALS873B, SN74AS873A

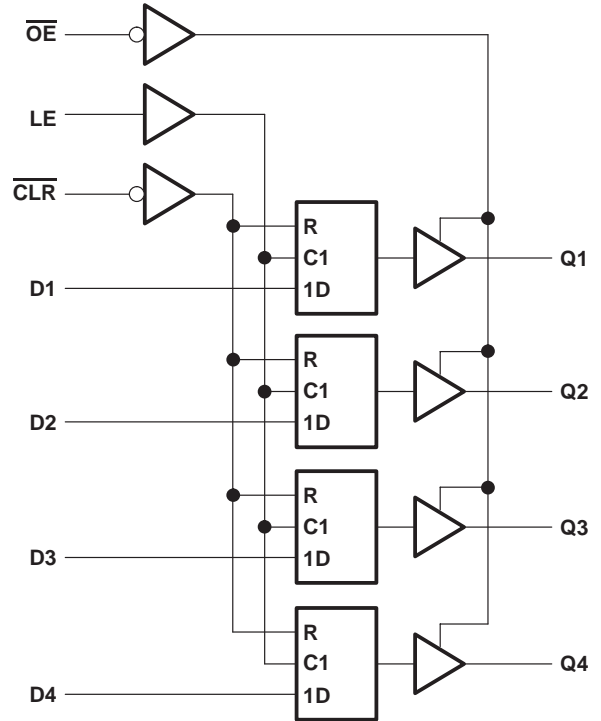
DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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logic symbol†



logic diagram (each quad latch, positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Voltage applied to a disabled 3-state output | 5.5 V |
| Operating free-air temperature range, T_A : SN54ALS873B | -55°C to 125°C |
| SN74ALS873B | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | SN54ALS873B | | | SN74ALS873B | | | UNIT |
|--------------------------------------|-------------|-----|-----|-------------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} Low-level input voltage | | | 0.7 | | | 0.8 | V |
| I_{OH} High-level output current | | | -1 | | | -2.6 | mA |
| I_{OL} Low-level output current | | | 12 | | | 24 | mA |
| T_A Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |



SN54ALS873B, SN54AS873A, SN74ALS873B, SN74AS873A DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54ALS873B | | SN74ALS873B | | UNIT |
|-----------------|---|---------------------------|--------------|------|--------------|------|---------------|
| | | | MIN | TYP† | MAX | MIN | |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, | $I_I = -18\text{ mA}$ | -1.2 | | -1.2 | | V |
| V_{OH} | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, | $I_{OH} = -0.4\text{ mA}$ | $V_{CC} - 2$ | | $V_{CC} - 2$ | | V |
| | $V_{CC} = 4.5\text{ V}$ | $I_{OH} = -1\text{ mA}$ | 2.4 | 3.3 | 2.4 | 3.2 | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 12\text{ mA}$ | 0.25 | 0.4 | 0.25 | 0.4 | V |
| | | $I_{OL} = 24\text{ mA}$ | | | 0.35 | 0.5 | |
| I_{OZH} | $V_{CC} = 5.5\text{ V}$, | $V_O = 2.7\text{ V}$ | 20 | | 20 | | μA |
| I_{OZL} | $V_{CC} = 5.5\text{ V}$, | $V_O = 0.4\text{ V}$ | -20 | | -20 | | μA |
| I_I | $V_{CC} = 5.5\text{ V}$, | $V_I = 7\text{ V}$ | 0.1 | | 0.1 | | mA |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, | $V_I = 2.7\text{ V}$ | 20 | | 20 | | μA |
| I_{IL} | $V_{CC} = 5.5\text{ V}$, | $V_I = 0.4\text{ V}$ | -0.2 | | -0.2 | | mA |
| $I_{O\ddagger}$ | $V_{CC} = 5.5\text{ V}$, | $V_O = 2.25\text{ V}$ | -20 | -112 | -30 | -112 | mA |
| I_{CC} | $V_{CC} = 5.5\text{ V}$ | Outputs high | 11 | 21 | 11 | 21 | mA |
| | | Outputs low | 16 | 29 | 16 | 29 | |
| | | Outputs disabled | 20 | 31 | 20 | 31 | |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | SN54ALS873B | | SN74ALS873B | | UNIT |
|----------|-----------------------------|-----------------------------|-----|-------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration | $\overline{\text{CLR}}$ low | 15 | 15 | ns | |
| | | LE high | 10 | 10 | | |
| t_{su} | Setup time, data before LE↓ | 10 | | 10 | | ns |
| t_h | Hold time, data after LE↓ | 7 | | 7 | | ns |



SN54ALS873B, SN54AS873A, SN74ALS873B, SN74AS873A

DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX† | | | | UNIT |
|------------------|--------------|-------------|--|-----|-------------|-----|------|
| | | | SN54ALS873B | | SN74ALS873B | | |
| | | | MIN | MAX | MIN | MAX | |
| t _{PLH} | D | Q | 2 | 23 | 2 | 14 | ns |
| t _{PHL} | | | 2 | 17 | 2 | 14 | |
| t _{PLH} | LE | Q | 8 | 31 | 8 | 22 | ns |
| t _{PHL} | | | 8 | 26 | 8 | 21 | |
| t _{PHL} | CLR | Q | 6 | 27 | 6 | 20 | ns |
| t _{PZH} | OE | Q | 4 | 24 | 4 | 18 | ns |
| t _{PZL} | | | 4 | 23 | 4 | 18 | |
| t _{PHZ} | OE | Q | 2 | 12 | 2 | 10 | ns |
| t _{PLZ} | | | 2 | 30 | 2 | 15 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|----------------|
| Supply voltage, V _{CC} | 7 V |
| Input voltage, V _I | 7 V |
| Voltage applied to a disabled 3-state output | 5.5 V |
| Operating free-air temperature range, T _A : SN54AS873A | -55°C to 125°C |
| SN74AS873A | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | SN54AS873A | | | SN74AS873A | | | UNIT |
|---|------------|-----|-----|------------|-----|-----|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V _{IH} High-level input voltage | 2 | | | 2 | | | V |
| V _{IL} Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I _{OH} High-level output current | | | -12 | | | -15 | mA |
| I _{OL} Low-level output current | | | 32 | | | 48 | mA |
| T _A Operating free-air temperature | -55 | | 125 | 0 | | 70 | °C |



SN54ALS873B, SN54AS873A, SN74ALS873B, SN74AS873A DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54AS873A | | | SN74AS873A | | | UNIT |
|----------------|---|--------------------------|--------------|------|------|--------------|------|-----|---------------|
| | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, | $I_I = -18\text{ mA}$ | -1.2 | | | -1.2 | | | V |
| V_{OH} | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, | $I_{OH} = -2\text{ mA}$ | $V_{CC} - 2$ | | | $V_{CC} - 2$ | | | V |
| | $V_{CC} = 4.5\text{ V}$ | $I_{OH} = -12\text{ mA}$ | 2.4 | 3.2 | | | | | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 32\text{ mA}$ | 0.25 | | 0.5 | | | | V |
| | | $I_{OL} = 48\text{ mA}$ | | | 0.35 | | 0.5 | | |
| I_{OZH} | $V_{CC} = 5.5\text{ V}$, | $V_O = 2.7\text{ V}$ | 50 | | | 50 | | | μA |
| I_{OZL} | $V_{CC} = 5.5\text{ V}$, | $V_O = 0.4\text{ V}$ | -50 | | | -50 | | | μA |
| I_I | $V_{CC} = 5.5\text{ V}$, | $V_I = 7\text{ V}$ | 0.1 | | | 0.1 | | | mA |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, | $V_I = 2.7\text{ V}$ | 20 | | | 20 | | | μA |
| I_{IL} | $V_{CC} = 5.5\text{ V}$, | $V_I = 0.4\text{ V}$ | -0.5 | | | -0.5 | | | mA |
| I_O^\ddagger | $V_{CC} = 5.5\text{ V}$, | $V_O = 2.25\text{ V}$ | -30 | -112 | | -30 | -112 | | mA |
| I_{CC} | $V_{CC} = 5.5\text{ V}$ | Outputs high | 68 | 110 | | 68 | 110 | | mA |
| | | Outputs low | 67 | 109 | | 67 | 109 | | |
| | | Outputs disabled | 80 | 129 | | 80 | 129 | | |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

| | | SN54AS873A | | SN74AS873A | | UNIT |
|------------|-----------------------------|------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| t_w^* | Pulse duration | CLR low | | 5 | 5 | ns |
| | | LE high | | 6 | 5 | |
| t_{su}^* | Setup time, data before LE↓ | 2 | | 2 | ns | |
| t_h^* | Hold time, data after LE↓ | 4.5 | | 4.5 | ns | |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



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DUAL 4-BIT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

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switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX† | | | | UNIT |
|------------------|-------------------------|----------------|--|------|------------|------|------|
| | | | SN54AS873A | | SN74AS873A | | |
| | | | MIN | MAX | MIN | MAX | |
| t _{PLH} | D | Q | 3 | 12.5 | 3 | 9.5 | ns |
| t _{PHL} | | | 3 | 8.5 | 3 | 7.5 | |
| t _{PLH} | LE | Q | 6 | 15.5 | 6 | 13 | ns |
| t _{PHL} | | | 4 | 9 | 4 | 7.5 | |
| t _{PHL} | $\overline{\text{CLR}}$ | Q | 3 | 10.5 | 3 | 9 | ns |
| t _{PZH} | $\overline{\text{OE}}$ | Q | 2 | 8 | 2 | 6.5 | ns |
| t _{PZL} | | | 4 | 11 | 4 | 10.5 | |
| t _{PHZ} | $\overline{\text{OE}}$ | Q | 2 | 8 | 2 | 7.5 | ns |
| t _{PLZ} | | | 2 | 8.5 | 2 | 7.5 | |

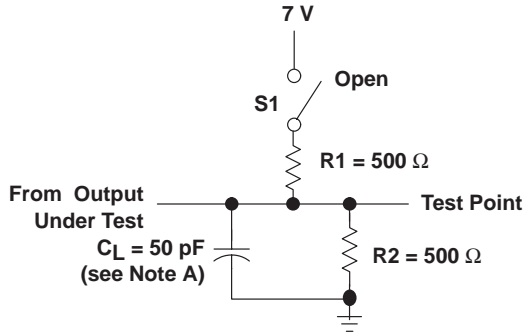
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS873B, SN54AS873A, SN74ALS873B, SN74AS873A DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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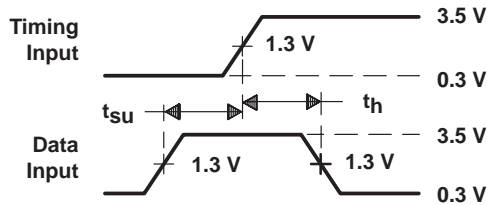
PARAMETER MEASUREMENT INFORMATION



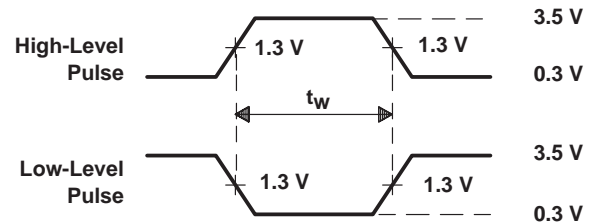
LOAD CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION TABLE

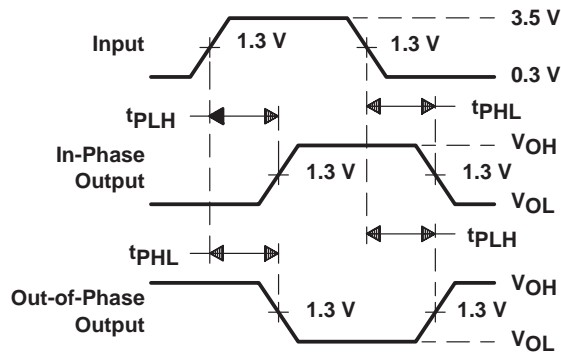
| TEST | S1 |
|-----------|--------|
| t_{PLH} | Open |
| t_{PHL} | Open |
| t_{PZH} | Open |
| t_{PZL} | Closed |
| t_{PHZ} | Open |
| t_{PLZ} | Closed |



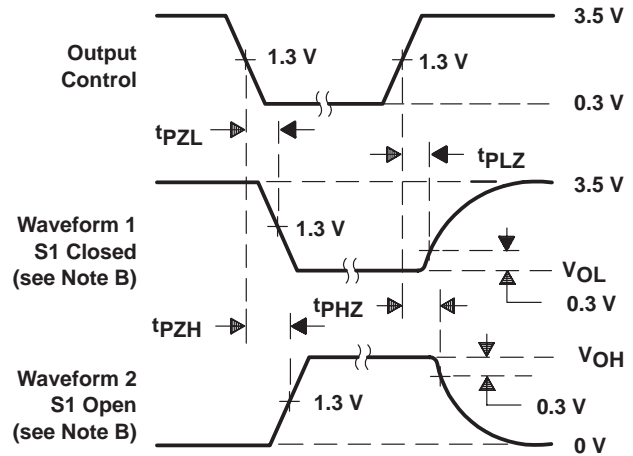
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|----------------------------------|
| 84032013A | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type | Purchase Samples |
| 8403201KA | OBSOLETE | CFP | W | 24 | | TBD | Call TI | Call TI | Samples Not Available |
| 8403201LA | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 | N / A for Pkg Type | Purchase Samples |
| SN74ALS873BDW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| SN74ALS873BDWE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| SN74ALS873BDWG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| SN74ALS873BDWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| SN74ALS873BDWRE4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| SN74ALS873BDWRG4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | Purchase Samples |
| SN74ALS873BNT | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | Purchase Samples |
| SN74ALS873BNT3 | OBSOLETE | PDIP | NT | 24 | | TBD | Call TI | Call TI | Samples Not Available |
| SN74ALS873BNTE4 | ACTIVE | PDIP | NT | 24 | 15 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | Purchase Samples |
| SN74AS873ADW | OBSOLETE | SOIC | DW | 24 | | TBD | Call TI | Call TI | Samples Not Available |
| SN74AS873ADWR | OBSOLETE | SOIC | DW | 24 | | TBD | Call TI | Call TI | Samples Not Available |
| SN74AS873ANT | OBSOLETE | PDIP | NT | 24 | | TBD | Call TI | Call TI | Samples Not Available |
| SNJ54ALS873BFK | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type | Purchase Samples |
| SNJ54ALS873BJT | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 | N / A for Pkg Type | Purchase Samples |
| SNJ54AS873AFK | OBSOLETE | LCCC | FK | 28 | | TBD | Call TI | Call TI | Samples Not Available |
| SNJ54AS873AJT | OBSOLETE | CDIP | JT | 24 | | TBD | Call TI | Call TI | Samples Not Available |
| SNJ54AS873AW | OBSOLETE | CFP | W | 24 | | TBD | Call TI | Call TI | Samples Not Available |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54ALS873B, SN54AS873A, SN74ALS873B, SN74AS873A :

● Catalog: [SN74ALS873B](#), [SN74AS873A](#)

● Military: [SN54ALS873B](#), [SN54AS873A](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ALS873BDWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ALS873BDWR | SOIC | DW | 24 | 2000 | 346.0 | 346.0 | 41.0 |

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN

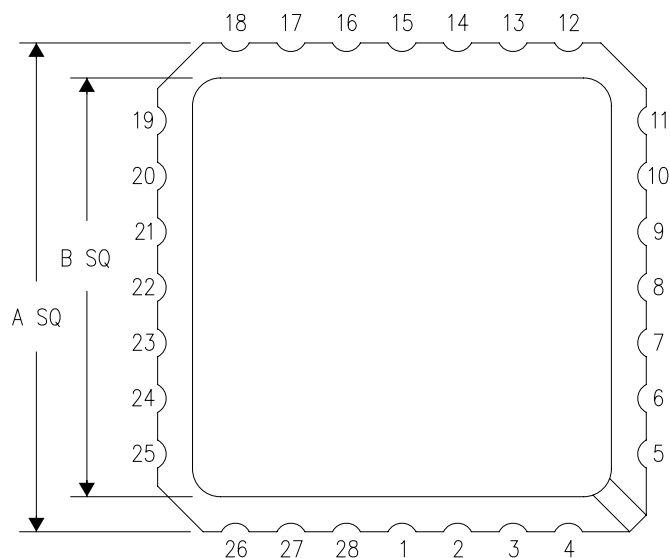


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



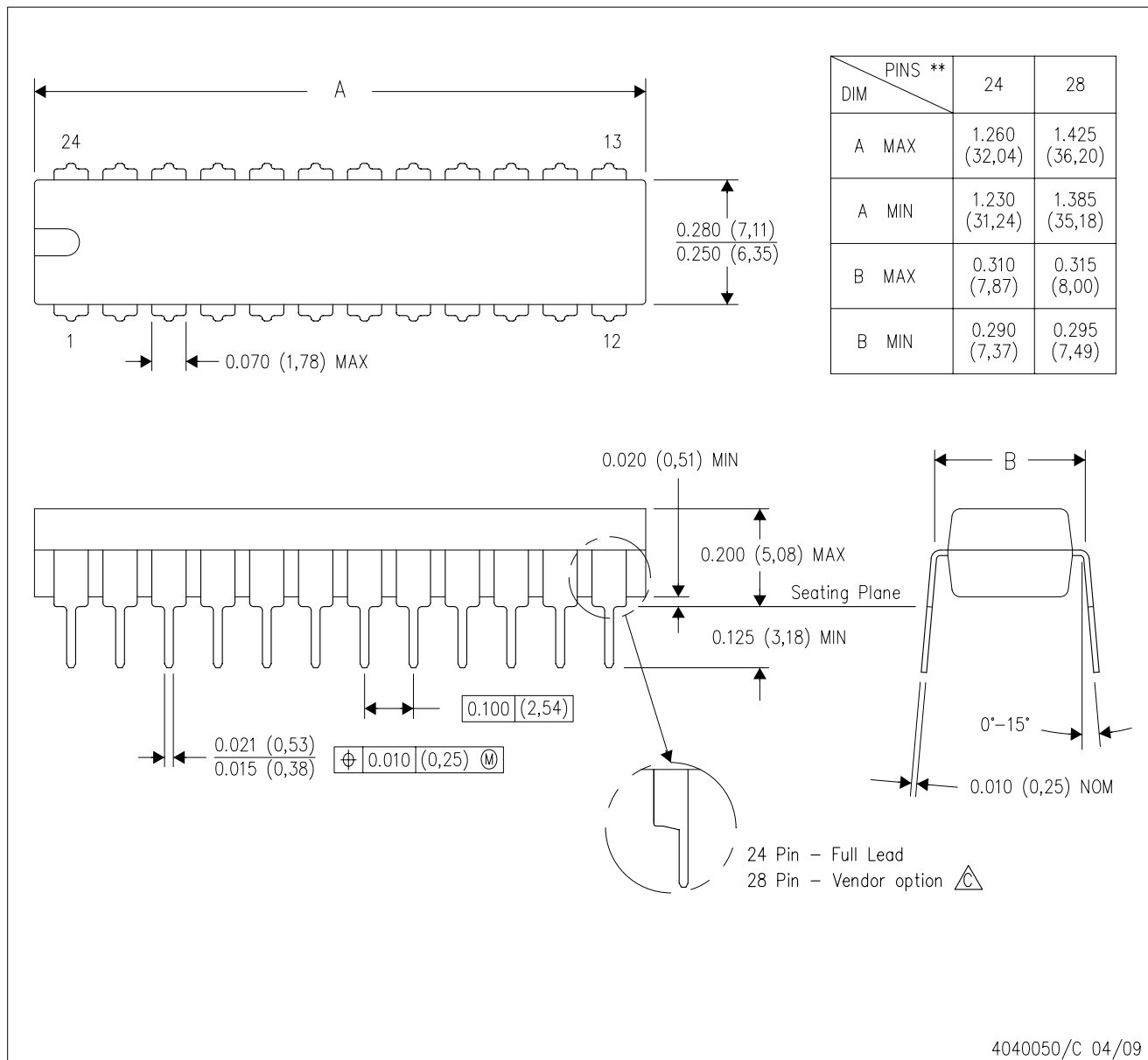
4040140/D 01/11


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

MECHANICAL DATA

NT (R-PDIP-T**) 24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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