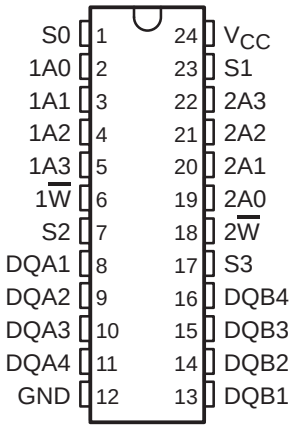
- **3-State Buffer-Type Outputs Drive Bus Lines Directly**
- **Each Register File Has Individual Write-Enable Controls and Address Lines**
- **Designed Specifically for Multibus Architecture and Overlapping File Operations**
- **Prioritized B-Input Port Prevents Write Conflicts During Dual-Input Mode**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs**

**DW OR NT PACKAGE**
**(TOP VIEW)**




## description

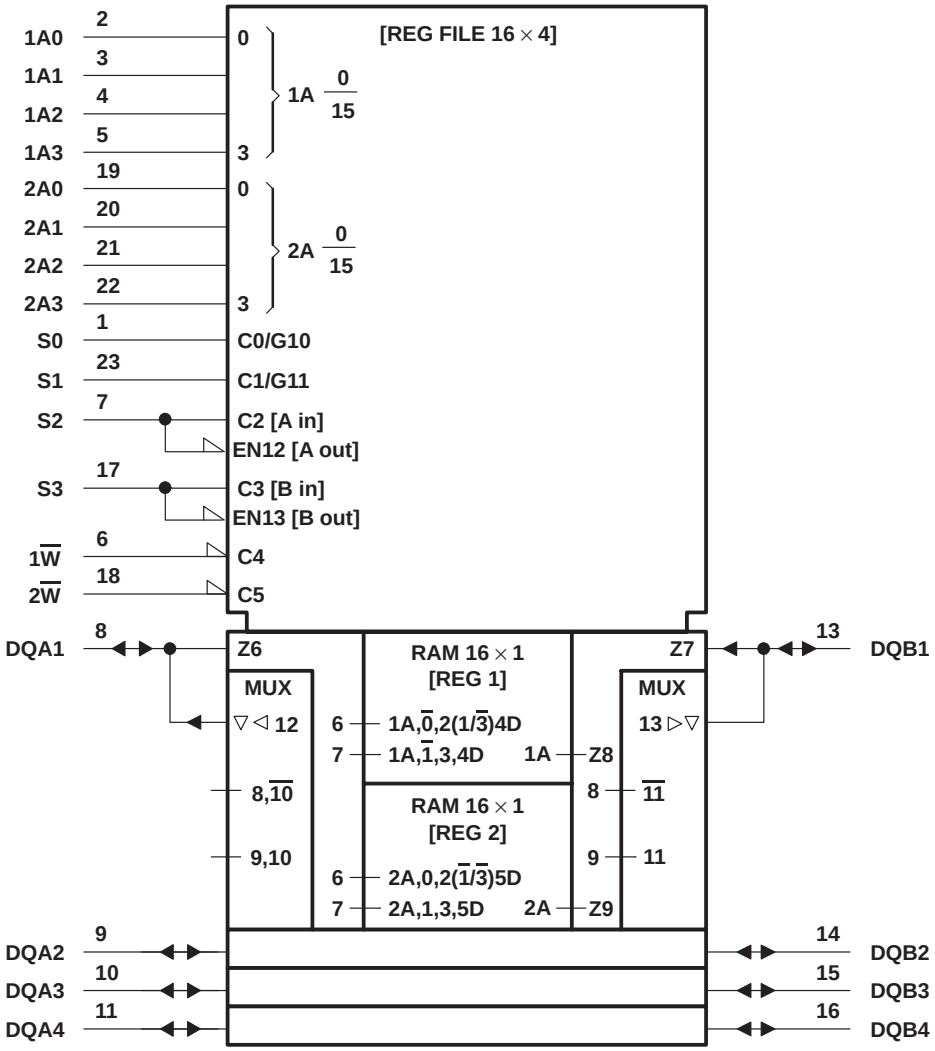
This device features two 16-word by 4-bit register files. Each register file has individual write-enable ($1\overline{W}$, $2\overline{W}$) controls and address lines. This device has two 4-bit data I/O ports (DQA1–DQA4 and DQB1–DQB4). The data I/O ports can output to bus A and bus B, receive input from bus A and bus B, receive input from bus A and output to bus B, or output to bus A and receive input from bus B. To prevent writing conflicts in the dual-input mode, the B-input port takes priority. Two select (S0 and S1) lines control which port has access to which register. S2 determines whether the A ports are in the input or the output modes and S3 does likewise for the B ports. The address lines (1A0–1A3 or 2A0–2A3) are decoded by an internal 1-of-16 decoder to select which register word is to be accessed. All outputs are 3-state buffer-type outputs designed specifically to drive bus lines directly.

The SN74ALS870 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

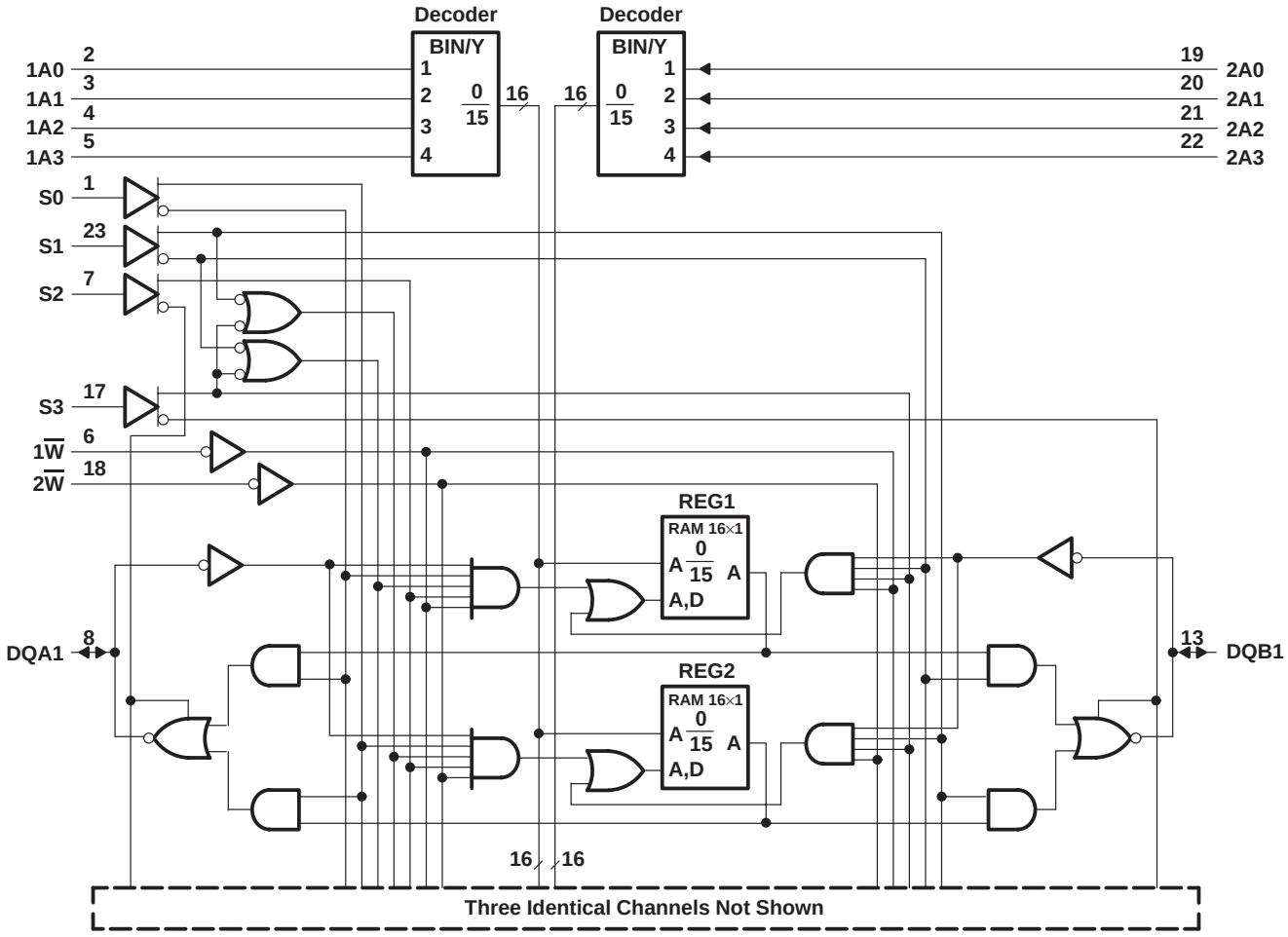
| FILE SELECT | | | INPUT/OUTPUT | | |
|---|---|---|---|---|---|
| **S0** | **S1** | **FILE SEL** | **S2** | **S3** | **I/O SEL** |
| L | L | 1R to A, 1R to B | L | L | A out, B out |
| H | L | 2R to A, 1R to B | | | |
| L | H | 1R to A, 2R to B | | | |
| H | H | 2R to A, 2R to B | | | |
| L | L | A to 1R, 1R to B | H | L | A in, B out |
| H | L | A to 2R, 1R to B | | | |
| L | H | A to 1R, 2R to B | | | |
| H | H | A to 2R, 2R to B | | | |
| L | L | 1R to A, B to 1R | L | H | A out, B in |
| H | L | 2R to A, B to 1R | | | |
| L | H | 1R to A, B to 2R | | | |
| H | H | 2R to A, B to 2R | | | |
| L | L | B to 1R | H | H | A in, B in |
| H | L | A to 2R, B to 1R | | | |
| L | H | A to 1R, B to 2R | | | |
| H | H | B to 2R | | | |

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, $T_A$ . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | –2.6 | mA |
| $I_{OL}$ | Low-level output current | | | | 24 | mA |
| $t_w$ | Pulse duration, write | | 12 | | | ns |
| $t_{su}$ | Setup time | Address before write↓ | 5 | | | ns |
| | | Data before write↑ | 15 | | | |
| | | Select before write↓ | 12 | | | |
| $t_h$ | Hold time | Address before write↓ | 0 | | | ns |
| | | Data before write↑ | 0 | | | |
| | | Select before write↓ | 12 | | | |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –0.4 mA | $V_{CC}$ –2 | | | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –2.6 mA | 2.4 | 3.2 | | |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 24 mA | | 0.35 | 0.5 | V |
| $I_I$ | Control inputs | $V_{CC}$ = 5.5 V | $V_I$ = 7 V | | | 0.1 | mA |
| | DQA and DQB ports | | $V_I$ = 5.5 V | | | 0.2 | |
| $I_{IH}$ | $1\overline{W}$ and $2\overline{W}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| | Other control inputs | | | | | 40 | |
| | DQA and DQB ports‡ | | | | | 50 | |
| $I_{IL}$ | Control inputs | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –0.2 | mA |
| | DQA and DQB ports‡ | | | | | –0.2 | |
| $I_O$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | –30 | | –112 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | | | 80 | 110 | mA |

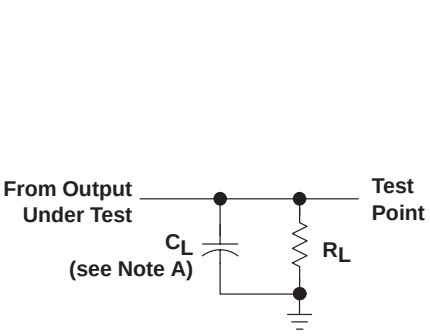
† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ For I/O ports, the parameters $I_{IH}$ and $I_{IL}$ include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

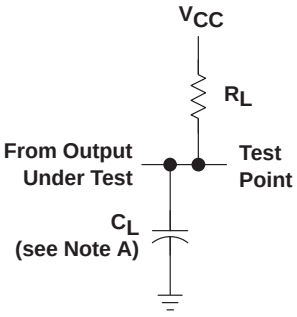
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{a(A)}$ | Any A | Any DQ | 3 | 19 | ns |
| $t_{a(S)}$ | S0 | Any DQA | 3 | 15 | ns |
| | S1 | Any DQB | 3 | 15 | |
| $t_{dis}$ | S2 | Any DQA | 3 | 14 | ns |
| | S3 | Any DQB | 3 | 14 | |
| $t_{en}$ | S2 | Any DQA | 3 | 17 | ns |
| | S3 | Any DQB | 3 | 17 | |
| $t_{pd}$ | $\overline{W}$ | Any DQ | 5 | 23 | ns |
| | DQA | DQB | 5 | 26 | |
| | DQB | DQA | 5 | 26 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

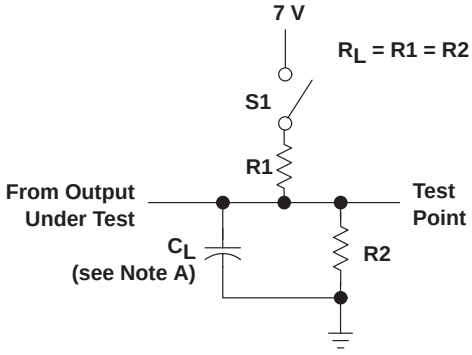
## PARAMETER MEASUREMENT INFORMATION
## SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



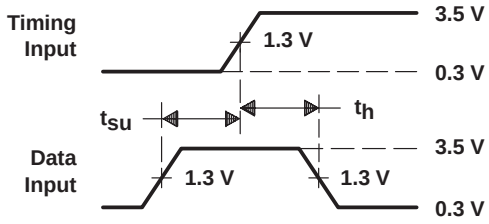

LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



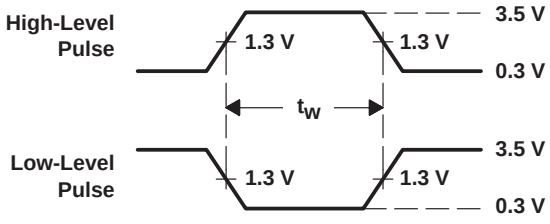

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



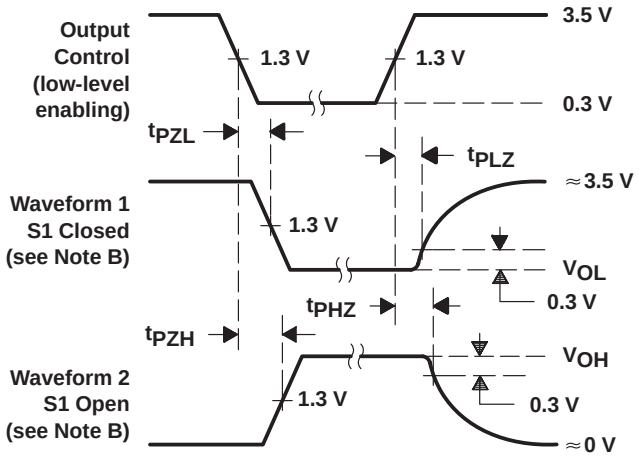

LOAD CIRCUIT
FOR 3-STATE OUTPUTS



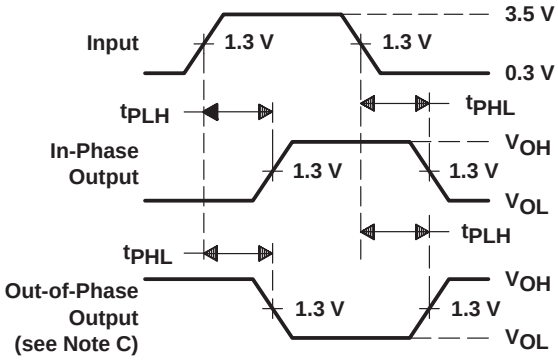

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

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