

Distributed by:

JAMECO[®]
ELECTRONICS

www.Jameco.com ♦ 1-800-831-4242

The content and copyrights of the attached
material are the property of its owner.

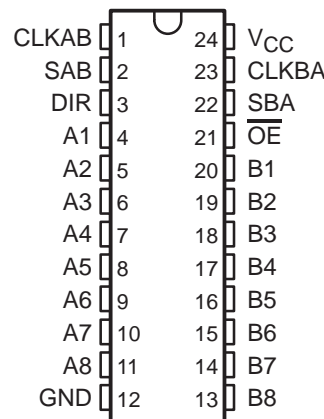
Jameco Part Number 833459

SN54ALS646, SN54ALS648, SN54AS646 SN74ALS646A, SN74ALS648A, SN74AS646, SN74AS648 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS039F – DECEMBER 1983 – REVISED JANUARY 1995

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True or Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

SN54ALS646, SN54ALS648, SN54AS646 . . . JT PACKAGE
SN74ALS646A, SN74ALS648A, SN74AS646,
SN74AS648 . . . DW OR NT PACKAGE
(TOP VIEW)



DEVICE	OUTPUT	LOGIC
SN54ALS646, SN74ALS646A, 'AS646	3 state	True
SN54ALS648, SN74ALS648A, SN74AS648	3 state	Inverting

description

These devices consist of bus-transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Output-enable (\overline{OE}) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either or both registers.

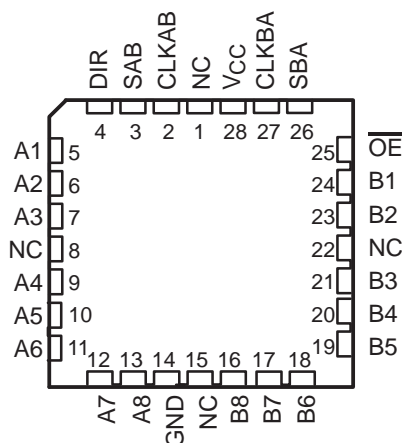
The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The -1 version of the SN74ALS646A is identical to the standard version, except that the recommended maximum I_{OL} in the -1 version is increased to 48 mA. There are no -1 versions of the SN54ALS646, SN54ALS648, or SN74ALS648A.

The SN54ALS646, SN54ALS648, and SN54AS646 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS646A, SN74ALS648A, SN74AS646, and SN74AS648 are characterized for operation from 0°C to 70°C .

SN54ALS646, SN54ALS648, SN54AS646 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

SN54ALS646, SN54ALS648, SN54AS646
 SN74ALS646A, SN74ALS648A, SN74AS646, SN74AS648
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS039F – DECEMBER 1983 – REVISED JANUARY 1995

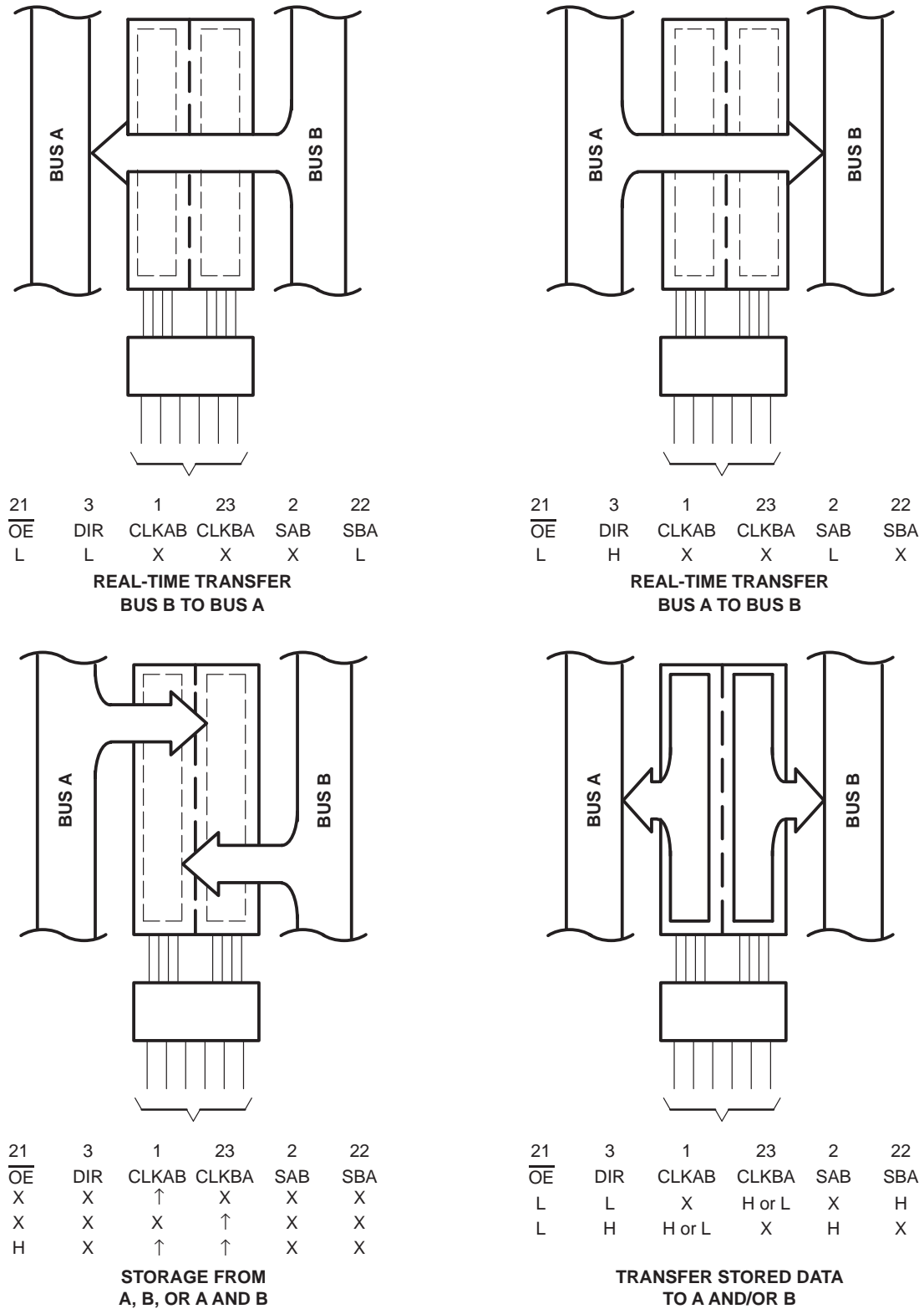


Figure 1. Bus-Management Functions

Pin numbers shown are for the DW, JT, and NT packages.

SN54ALS646, SN54ALS648, SN54AS646
SN74ALS646A, SN74ALS648A, SN74AS646, SN74AS648
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS
SDAS039F – DECEMBER 1983 – REVISED JANUARY 1995

Function Tables

SN54ALS646, SN54AS646, SN74ALS646A, SN74AS646

INPUTS						DATA I/O		OPERATION OR FUNCTION
\overline{OE}	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified [†]	Store A, B unspecified [†]
X	X	X	↑	X	X	Unspecified [†]	Input	Store B, A unspecified [†]
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

[†] The data output functions can be enabled or disabled by various signals at \overline{OE} and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

SN54ALS648, SN74ALS648A, SN74AS648

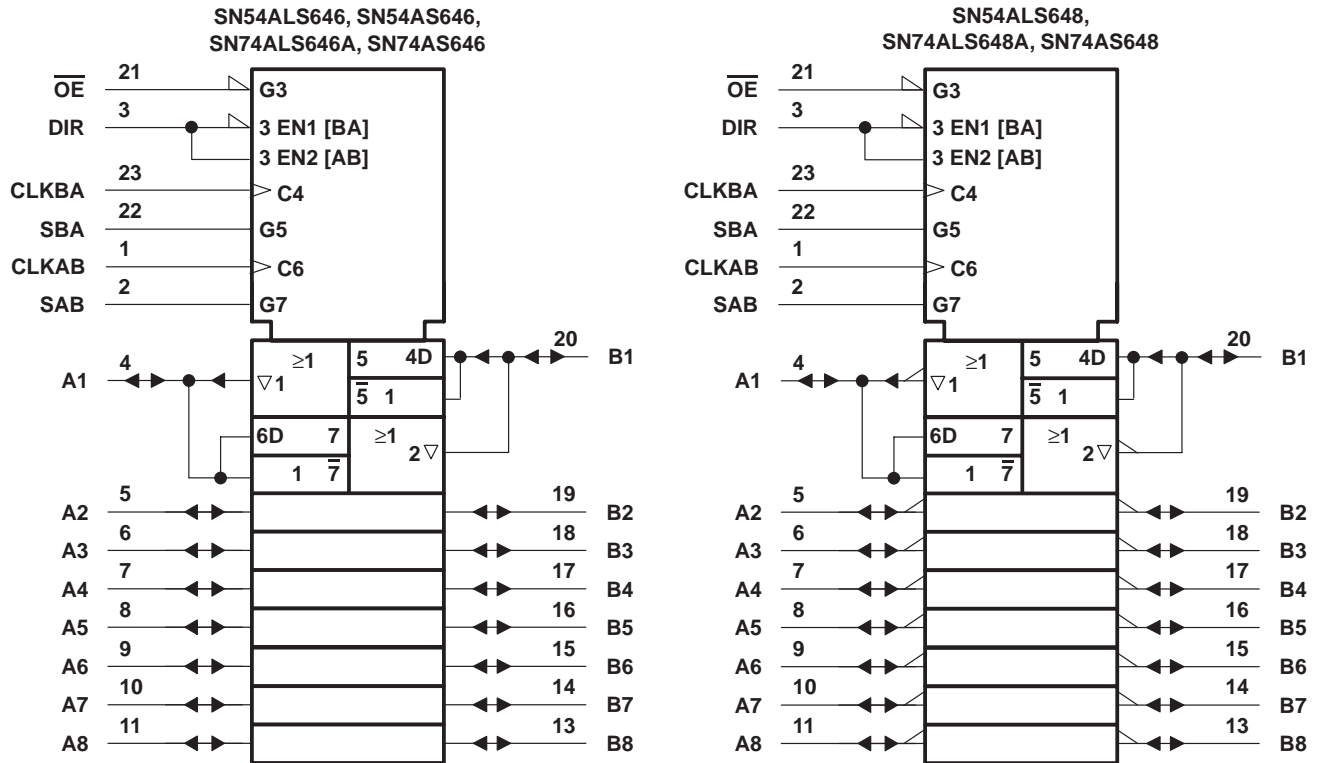
INPUTS						DATA I/O		OPERATION OR FUNCTION
\overline{OE}	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	↑	X	X	X	Input	Unspecified [†]	Store A, B unspecified [†]
X	X	X	↑	X	X	Unspecified [†]	Input	Store B, A unspecified [†]
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time \overline{B} data to A bus
L	L	X	H or L	X	H	Output	Input	Stored \overline{B} data to A bus
L	H	X	X	L	X	Input	Output	Real-time \overline{A} data to B bus
L	H	H or L	X	H	X	Input	Output	Stored \overline{A} data to B bus

[†] The data output functions can be enabled or disabled by various signals at \overline{OE} and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

**SN54ALS646, SN54ALS648, SN54AS646
 SN74ALS646A, SN74ALS648A, SN74AS646, SN74AS648
 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS039F – DECEMBER 1983 – REVISED JANUARY 1995

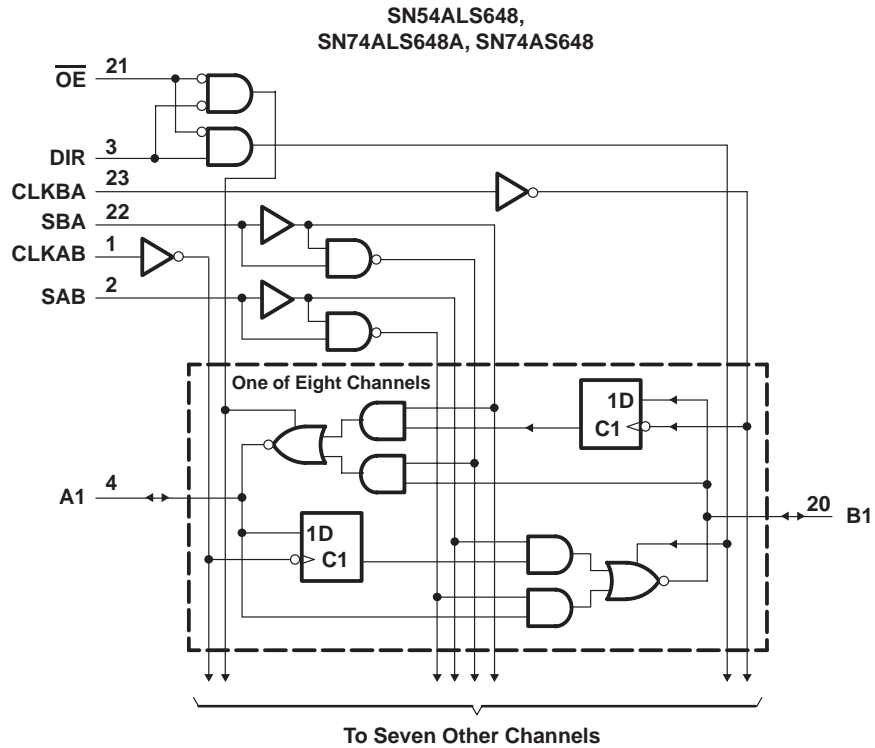
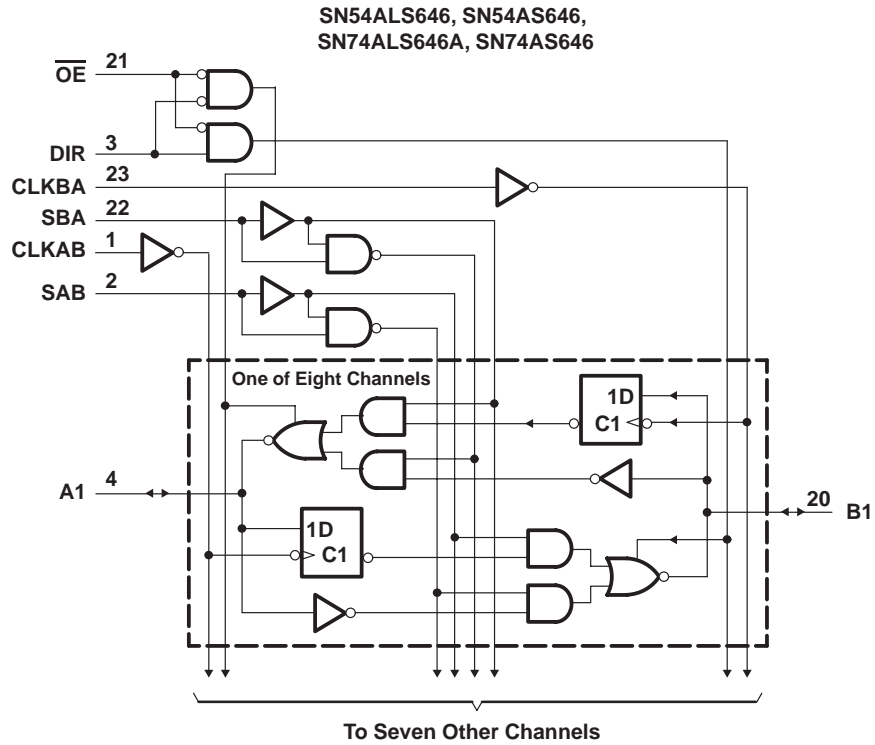
logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for the DW, JT, and NT packages.

SN54ALS646, SN54ALS648, SN54AS646
 SN74ALS646A, SN74ALS648A, SN74AS646, SN74AS648
 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS
 SDAS039F – DECEMBER 1983 – REVISED JANUARY 1995

logic diagrams (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

SN54ALS646, SN54ALS648, SN54AS646
SN74ALS646A, SN74ALS648A, SN74AS646, SN74AS648
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS039F – DECEMBER 1983 – REVISED JANUARY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I : Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, T_A : SN54ALS646	–55°C to 125°C
SN74ALS646A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	SN54ALS646			SN74ALS646A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			–12			–15	mA
I_{OL} Low-level output current			12			24	mA
						48‡	
f_{clock} Clock frequency	0		35	0		40	MHz
t_w Pulse duration, CLKBA or CLKAB high or low	14.5			12.5			ns
t_{su} Setup time, A before CLKAB↑ or B before CLKBA↑	15			10			ns
t_h Hold time, A after CLKAB↑ or B after CLKBA↑	0			0			ns
T_A Operating free-air temperature	–55		125	0		70	°C

‡ Applies only to the -1 version and only if V_{CC} is maintained between 4.75 V and 5.25



SN54ALS646, SN54ALS648, SN54AS646
SN74ALS646A, SN74ALS648A, SN74AS646, SN74AS648
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS039F – DECEMBER 1983 – REVISED JANUARY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS646		SN74ALS646A		UNIT	
		MIN	TYP†	MAX	MIN		TYP†
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2		-1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$	$V_{CC}-2$		$V_{CC}-2$		V	
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.2	2.4		3.2
		$I_{OH} = -12\text{ mA}$	2				
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$	0.25	0.4	0.25	0.4	V
		$I_{OL} = 24\text{ mA}$			0.35	0.5	
		$I_{OL} = 48\text{ mA}‡$			0.35	0.5	
I_I	Control inputs	$V_{CC} = 5.5\text{ V}$	$V_I = 7\text{ V}$	0.1		0.1	mA
	A or B ports		$V_I = 5.5\text{ V}$	0.1		0.1	
I_{IH}	Control inputs	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$	20		20	μA
	A or B ports§			20		20	
I_{IL}	Control inputs	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$	-0.2		-0.2	mA
	A or B ports§			-0.2		-0.2	
$I_{O}¶$	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.25\text{ V}$	-20	-112	-30	-112	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$	Outputs high	47	76	47	76	mA
		Outputs low	55	88	55	88	
		Outputs disabled	55	88	55	88	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Applies only to the -1 version and only if V_{CC} is maintained between 4.75 V and 5.25 V.

§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54ALS646, SN54ALS648, SN54AS646
SN74ALS646A, SN74ALS648A, SN74AS646, SN74AS648
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS039F – DECEMBER 1983 – REVISED JANUARY 1995

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54ALS646		SN74ALS646A		
			MIN	MAX	MIN	MAX	
f _{max}			35		40		MHz
t _{PLH}	CLKBA or CLKAB	A or B	10	35	7	30	ns
t _{PHL}			5	20	5	17	
t _{PLH}	A or B	B or A	5	22	3	20	ns
t _{PHL}			3	15	3	12	
t _{PLH}	SBA or SAB‡ (stored data low)	A or B	10	40	7	35	ns
t _{PHL}			5	23	5	20	
t _{PLH}	SBA or SAB‡ (stored data high)	A or B	8	30	6	25	ns
t _{PHL}			5	24	5	20	
t _{PZH}	\overline{OE}	A or B	3	20	2	17	ns
t _{PZL}			5	22	4	20	
t _{PHZ}	\overline{OE}	A or B	1	12	1	10	ns
t _{PLZ}			1	20	2	16	
t _{PZH}	DIR	A or B	5	38	3	30	ns
t _{PZL}			5	30	4	25	
t _{PHZ}	DIR	A or B	1	12	1	10	ns
t _{PLZ}			2	21	2	16	

† For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

SN54ALS646, SN54ALS648, SN54AS646
SN74ALS646A, SN74ALS648A, SN74AS646, SN74AS648
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS039F – DECEMBER 1983 – REVISED JANUARY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I : Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range, T_A : SN54ALS648	–55°C to 125°C
SN74ALS648A	0°C to 70°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS648			SN74ALS648A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			12			24	mA
f_{clock}	Clock frequency	0		35	0		40	MHz
t_w	Pulse duration, CLKBA or CLKAB high or low	14.5			12.5			ns
t_{su}	Setup time, A before CLKAB↑ or B before CLKBA↑	15			10			ns
t_h	Hold time, A after CLKAB↑ or B after CLKBA↑	0			0			ns
T_A	Operating free-air temperature	–55		125	0		70	°C



**SN54ALS646, SN54ALS648, SN54AS646
SN74ALS646A, SN74ALS648A, SN74AS646, SN74AS648
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS039F – DECEMBER 1983 – REVISED JANUARY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS648		SN74ALS648A		UNIT		
			MIN	TYP†	MAX	MIN		TYP†	MAX
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA			-1.2	-1.2		V	
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} -2		V _{CC} -2		V		
		V _{CC} = 4.5 V	I _{OH} = -3 mA	2.4	3.2	2.4		3.2	
			I _{OH} = -12 mA	2					
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V	
			I _{OL} = 24 mA			0.35	0.5		
I _I	Control inputs	V _{CC} = 5.5 V	V _I = 7 V		0.1		mA		
	A or B ports		V _I = 5.5 V		0.1				
I _{IH}	Control inputs	V _{CC} = 5.5 V,	V _I = 2.7 V		20		μA		
	A or B ports‡				20				
I _{IL}	Control inputs	V _{CC} = 5.5 V,	V _I = 0.4 V		-0.2		mA		
	A or B ports‡				-0.2				
I _{OS} §		V _{CC} = 5.5 V,	V _O = 2.25 V		-20	-112	-30	-112	mA
I _{CC}		V _{CC} = 5.5 V	Outputs high		47	76	47	76	mA
			Outputs low		57	88	57	88	
			Outputs disabled		57	88	57	88	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

**SN54ALS646, SN54ALS648, SN54AS646
SN74ALS646A, SN74ALS648A, SN74AS646, SN74AS648
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS**

SDAS039F – DECEMBER 1983 – REVISED JANUARY 1995

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54ALS648		SN74ALS648A		
			MIN	MAX	MIN	MAX	
f _{max}			35		40		MHz
t _{PLH}	CLKBA or CLKAB	A or B	8	39	7	33	ns
t _{PHL}			5	23	5	20	
t _{PLH}	A or B	B or A	3	20	2	17	ns
t _{PHL}			2	12	2	10	
t _{PLH}	SBA or SAB‡ (stored data low)	A or B	5	44	5	39	ns
t _{PHL}			4	26	4	22	
t _{PLH}	SBA or SAB‡ (stored data high)	A or B	6	30	6	25	ns
t _{PHL}			6	25	6	21	
t _{PZH}	\overline{OE}	A or B	4	25	2	22	ns
t _{PZL}			4	25	4	22	
t _{PHZ}	\overline{OE}	A or B	1	12	1	10	ns
t _{PLZ}			2	21	2	15	
t _{PZH}	DIR	A or B	4	35	2	27	ns
t _{PZL}			3	25	3	19	
t _{PHZ}	DIR	A or B	1	17	1	14	ns
t _{PLZ}			2	22	2	15	

† For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

SN54ALS646, SN54ALS648, SN54AS646
SN74ALS646A, SN74ALS648A, SN74AS646, SN74AS648
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS039F – DECEMBER 1983 – REVISED JANUARY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS646		SN74AS646		UNIT		
		MIN	TYP†	MAX	MIN		TYP†	MAX
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2		-1.2	V	
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -2\text{ mA}$	$V_{CC}-2$		$V_{CC}-2$		V		
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -3\text{ mA}$	2.4	3.2	2.4		3.2	
		$I_{OH} = -12\text{ mA}$	2					
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 32\text{ mA}$	0.25	0.5			V	
		$I_{OL} = 48\text{ mA}$			0.35	0.5		
I_I	Control inputs	$V_{CC} = 5.5\text{ V}$,	$V_I = 7\text{ V}$		0.1		mA	
	A or B ports	$V_{CC} = 5.5\text{ V}$,	$V_I = 5.5\text{ V}$		0.1			
I_{IH}	Control inputs	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$		20		μA	
	A or B ports‡				70			
I_{IL}	Control input	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$		-0.5		mA	
	A or B ports‡				-0.75			
I_{OS}	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.25\text{ V}$		-30	-112	-30	-112	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$	Outputs high	120	195	120	195	mA	
		Outputs low	130	211	130	211		
		Outputs disabled	130	211	130	211		

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54ALS646, SN54ALS648, SN54AS646
 SN74ALS646A, SN74ALS648A, SN74AS646, SN74AS648
 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS039F – DECEMBER 1983 – REVISED JANUARY 1995

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54AS646		SN74AS646		
			MIN	MAX	MIN	MAX	
f _{max} *			75		90	MHz	
t _{PLH}	CLKBA or CLKAB	A or B	2	9.5	2	8.5	ns
t _{PHL}			2	10	2	9	
t _{PLH}	A or B	B or A	2	11.5	2	9	ns
t _{PHL}			1	8	1	7	
t _{PLH}	SBA or SAB‡	A or B	2	13.5	2	11	ns
t _{PHL}			2	11	2	9	
t _{PZH}	\overline{OE}	A or B	2	11	2	9	ns
t _{PZL}			3	15	3	14	
t _{PHZ}	\overline{OE}	A or B	2	11	2	9	ns
t _{PLZ}			2	11	2	9	
t _{PZH}	DIR	A or B	3	21	3	16	ns
t _{PZL}			3	24	3	18	
t _{PHZ}	DIR	A or B	2	12	2	10	ns
t _{PLZ}			2	12	2	10	

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

† For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

SN54ALS646, SN54ALS648, SN54AS646
 SN74ALS646A, SN74ALS648A, SN74AS646, SN74AS648
 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS039F – DECEMBER 1983 – REVISED JANUARY 1995

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX†		UNIT
			SN74AS648		
			MIN	MAX	
f _{max}			90		MHz
t _{PLH}	CLKBA or CLKAB	A or B	2	8.5	ns
t _{PHL}			2	9	
t _{PLH}	A or B	B or A	2	8	ns
t _{PHL}			1	7	
t _{PLH}	SBA or SAB‡	A or B	2	11	ns
t _{PHL}			2	9	
t _{PZH}	\overline{OE}	A or B	2	9	ns
t _{PZL}			3	15	
t _{PHZ}	\overline{OE}	A or B	2	9	ns
t _{PLZ}			2	9	
t _{PZH}	DIR	A or B	3	16	ns
t _{PZL}			3	18	
t _{PHZ}	DIR	A or B	2	10	ns
t _{PLZ}			2	10	

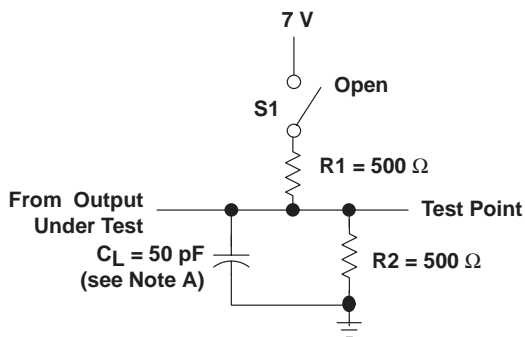
† For conditions shown MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

SN54ALS646, SN54ALS648, SN54AS646
 SN74ALS646A, SN74ALS648A, SN74AS646, SN74AS648
 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SDAS039F – DECEMBER 1983 – REVISED JANUARY 1995

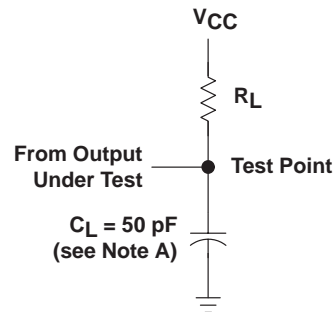
PARAMETER MEASUREMENT INFORMATION



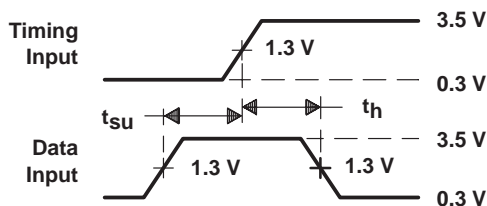
**LOAD CIRCUIT
FOR 3-STATE OUTPUTS**

SWITCH POSITION TABLE

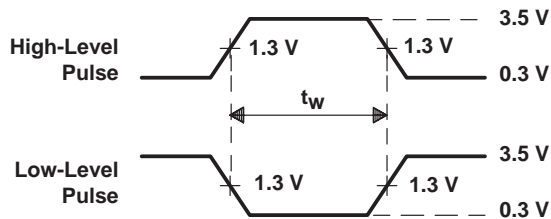
TEST	S1
t _{PLH}	Open
t _{PHL}	Open
t _{PZH}	Open
t _{PZL}	Closed
t _{PHZ}	Open
t _{PLZ}	Closed



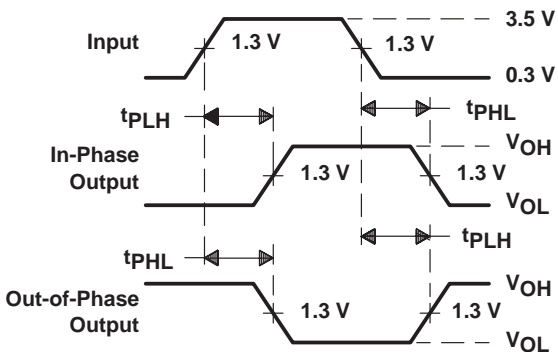
**LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS**



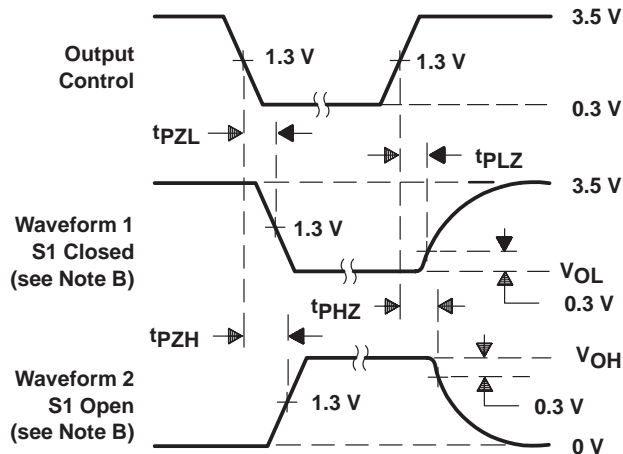
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-87595013A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8759501KA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
5962-8759501LA	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
5962-89956013A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8995601LA	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9052301LA	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SN54AS646JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SN74ALS646A-1DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS646A-1DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS646A-1DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS646A-1DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS646A-1NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS646A-1NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS646ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS646ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS646ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS646ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS646ANT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS646ANTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS648ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS648ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS648ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS648ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS648ANT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS648ANTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS646DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS646DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS646DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
						no Sb/Br)		
SN74AS646DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS646NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS646NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS648DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS648DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS648DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS648DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS648NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS648NT3	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
SN74AS648NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54ALS646FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54ALS646JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54ALS646W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI
SNJ54ALS648FK	OBSOLETE	LCCC	FK	24		TBD	Call TI	Call TI
SNJ54ALS648JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54ALS648W	OBSOLETE	CFP	W	24		TBD	Call TI	Call TI
SNJ54AS646FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54AS646JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54AS646W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

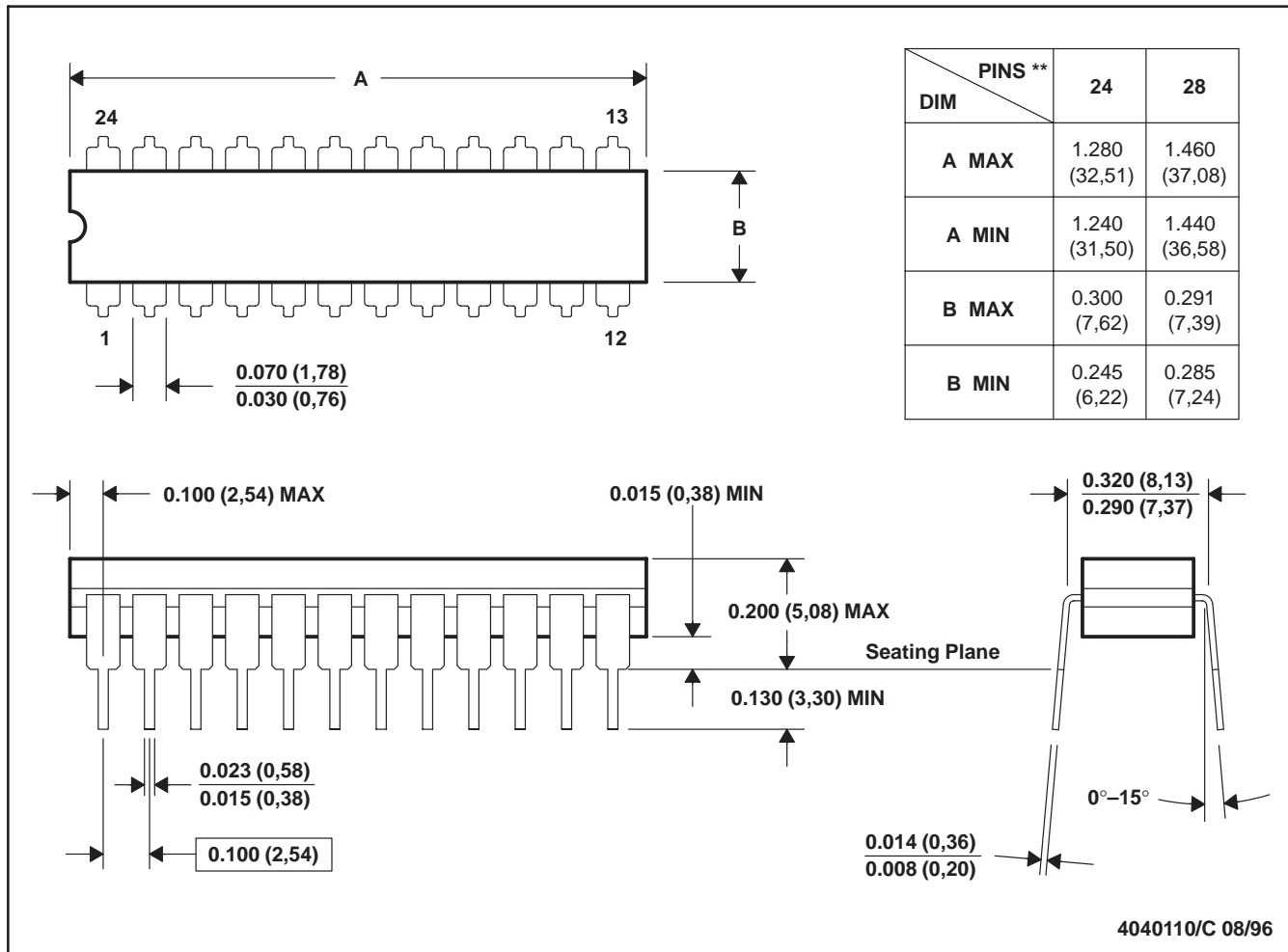
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

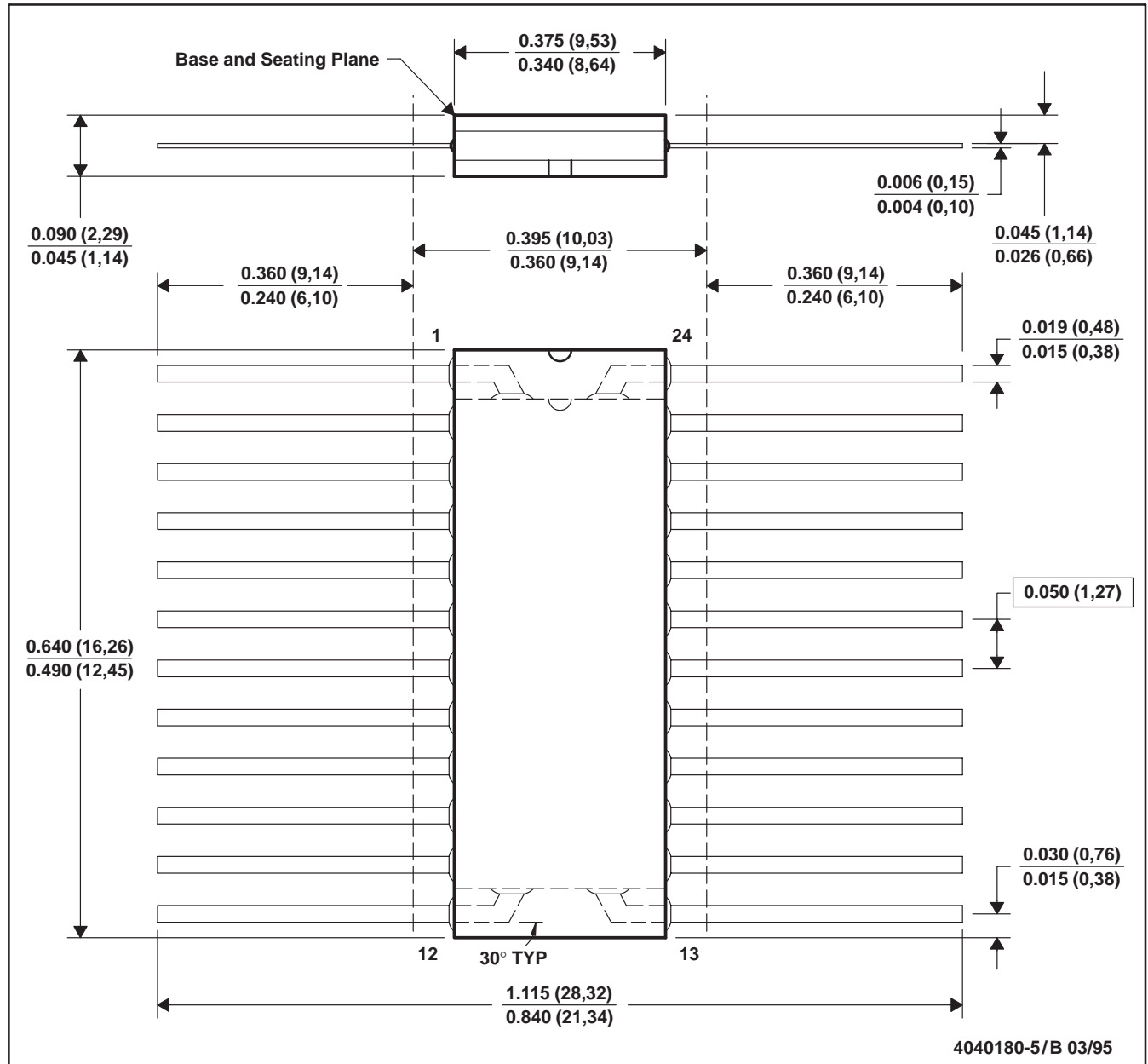
24 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK

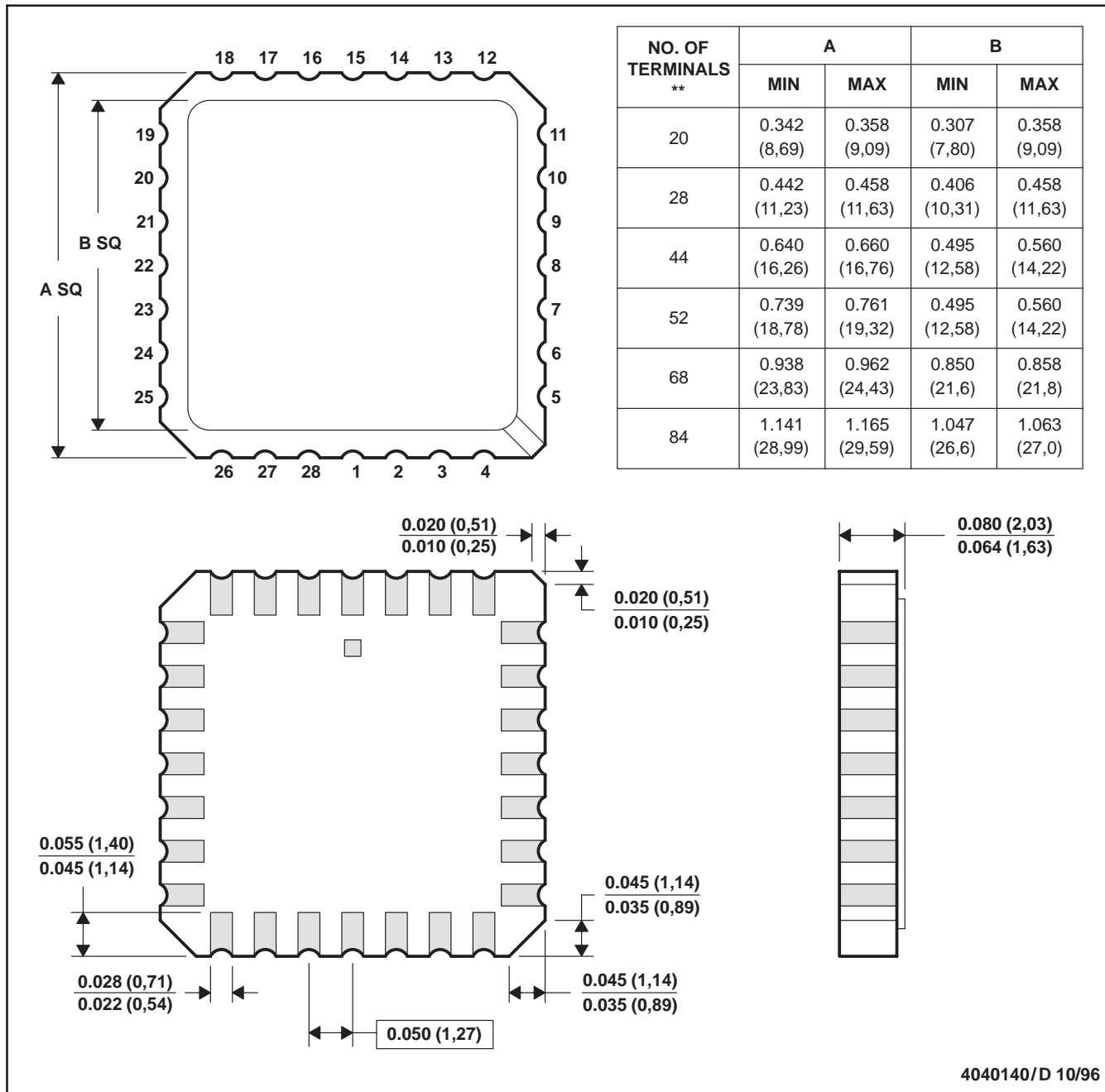


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 - Index point is provided on cap for terminal identification only.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

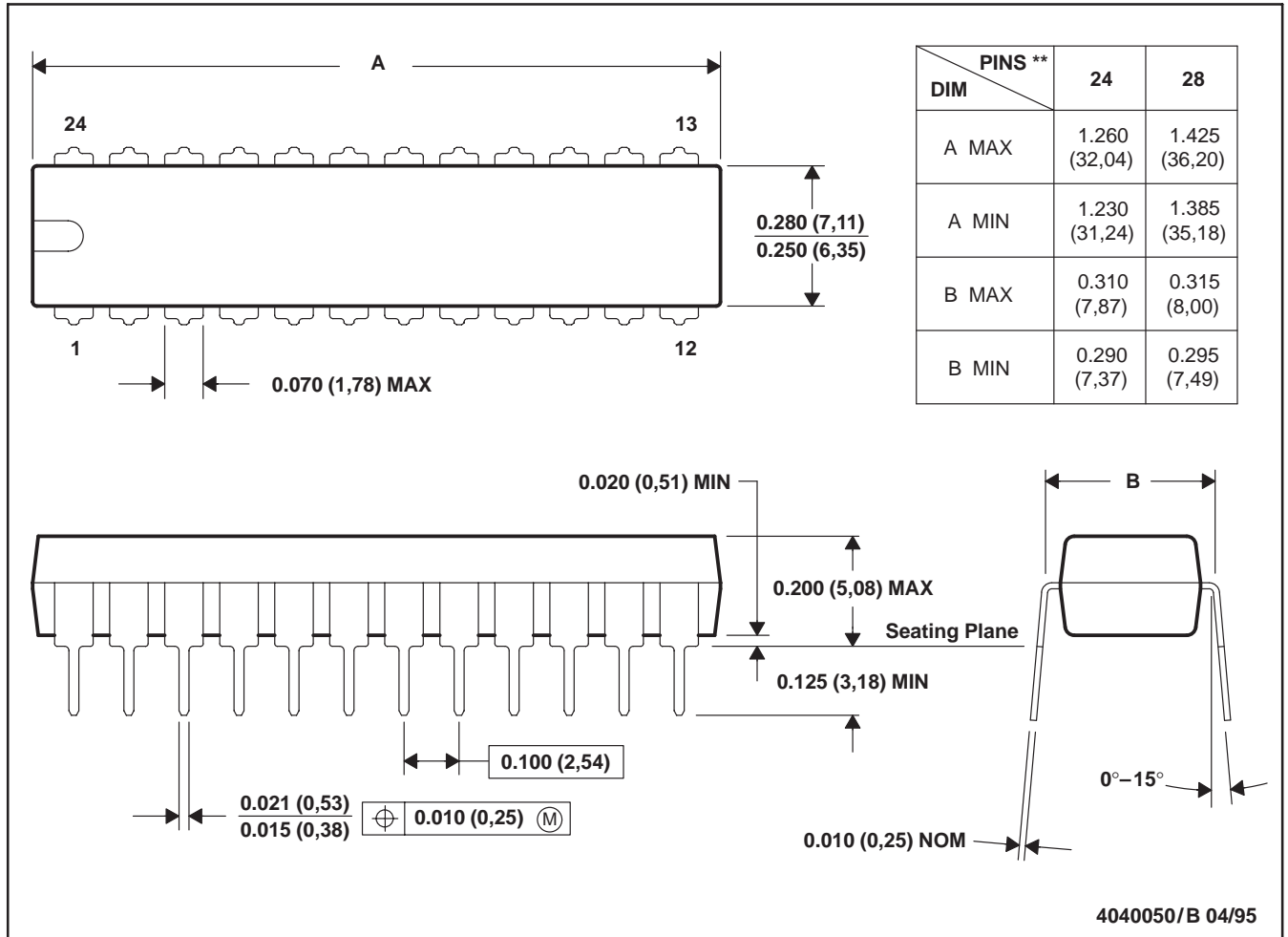


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265