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Jameco Part Number 973697

# SN74ALS29863 9-BIT TRANSCEIVER WITH 3-STATE OUTPUTS

SDAS096C – JANUARY 1986 – REVISED JANUARY 1995

- Functionally Equivalent to AMD's AM29863
- Power-Up High-Impedance State
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

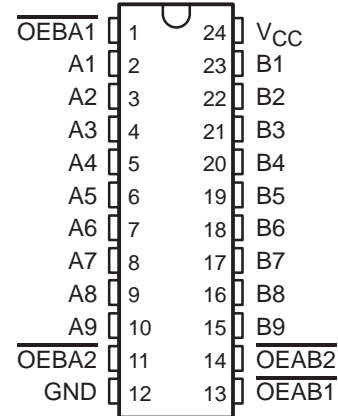
## description

This 9-bit transceiver is designed for asynchronous two-way communication between data buses. The control-function implementation allows for maximum flexibility in timing.

This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic levels at the output-enable ( $\overline{OEAB1}$ ,  $\overline{OEAB2}$ ,  $\overline{OEBA1}$ , and  $\overline{OEBA2}$ ) inputs.

The SN74ALS29863 is characterized for operation from 0°C to 70°C.

DW OR NT PACKAGE  
(TOP VIEW)



FUNCTION TABLE

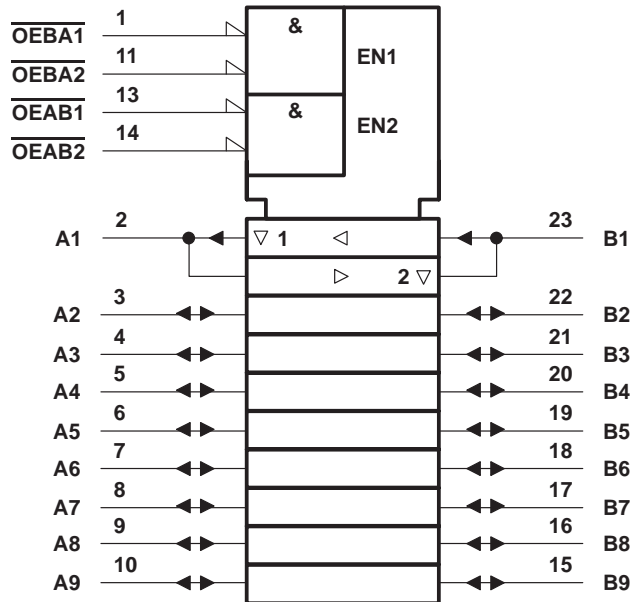
INPUTS				OPERATION
$\overline{OEAB1}$	$\overline{OEAB2}$	$\overline{OEBA1}$	$\overline{OEBA2}$	
L	L	L	L	Latch A and B
L	L	H	X	A to B
L	L	X	H	
H	X	L	L	B to A
X	H	L	L	
H	X	H	X	Isolation
H	X	X	H	
X	H	X	H	
X	H	H	X	

# SN74ALS29863

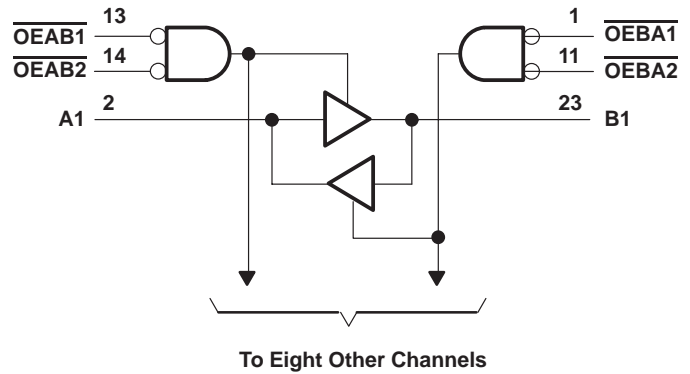
## 9-BIT TRANSCEIVER WITH 3-STATE OUTPUTS

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### logic symbol†



### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$ (all inputs and I/O ports)	5.5 V
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current			-24	mA
$I_{OL}$	Low-level output current			48	mA
$T_A$	Operating free-air temperature	0		70	°C

**SN74ALS29863**  
**9-BIT TRANSCEIVER**  
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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 4.75 V, I <sub>I</sub> = -18 mA			-1.2	V
V <sub>OH</sub>		V <sub>CC</sub> = 4.75 V	I <sub>OH</sub> = -15 mA		2.4	V
			I <sub>OH</sub> = -24 mA		2	
V <sub>OL</sub>		V <sub>CC</sub> = 4.75 V, I <sub>OL</sub> = 48 mA		0.35	0.5	V
I <sub>I</sub>		V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 5.5 V			0.1	mA
I <sub>IH</sub>	Control inputs	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.7 V			20	μA
	A or B ports‡				20	
I <sub>IL</sub>	Control inputs	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.4 V			-0.1	mA
	A or B ports‡				-0.1	
I <sub>OS</sub> §		V <sub>CC</sub> = 5.25 V, V <sub>O</sub> = 0	-75		-250	mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.25 V		40	65	mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

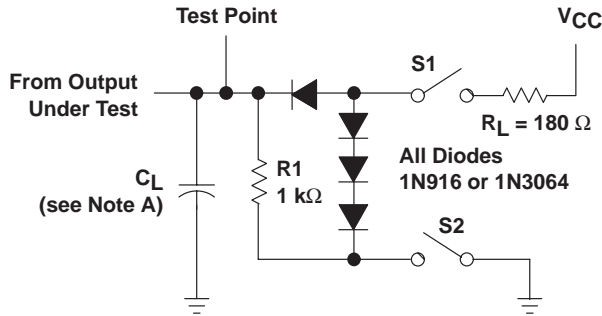
**switching characteristics (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V <sub>CC</sub> = 4.75 V to 5.25 V		UNIT
				MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	C <sub>L</sub> = 300 pF			ns
t <sub>PHL</sub>						
t <sub>PLH</sub>	A or B	B or A	C <sub>L</sub> = 50 pF			ns
t <sub>PHL</sub>						
t <sub>PZH</sub>	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	C <sub>L</sub> = 300 pF			ns
t <sub>PZL</sub>						
t <sub>PZH</sub>	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	C <sub>L</sub> = 50 pF			ns
t <sub>PZL</sub>						
t <sub>PHZ</sub>	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	C <sub>L</sub> = 50 pF			ns
t <sub>PLZ</sub>						
t <sub>PHZ</sub>	$\overline{OEAB}$ or $\overline{OEBA}$	A or B	C <sub>L</sub> = 5 pF			ns
t <sub>PLZ</sub>						

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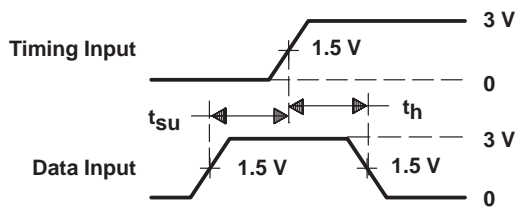
## PARAMETER MEASUREMENT INFORMATION



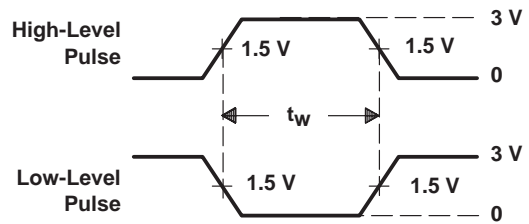
LOAD CIRCUIT

SWITCH POSITION TABLE

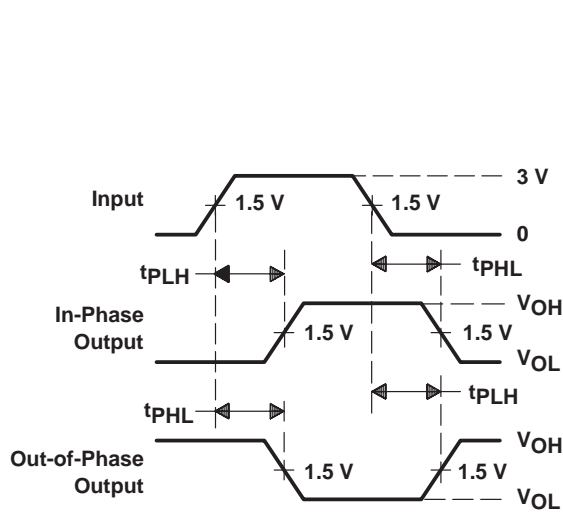
TEST	S1	S2
$t_{PLH}$	Closed	Closed
$t_{PHL}$	Closed	Closed
$t_{PZH}$	Open	Closed
$t_{PZL}$	Closed	Open
$t_{PHZ}$	Closed	Closed
$t_{PLZ}$	Closed	Closed



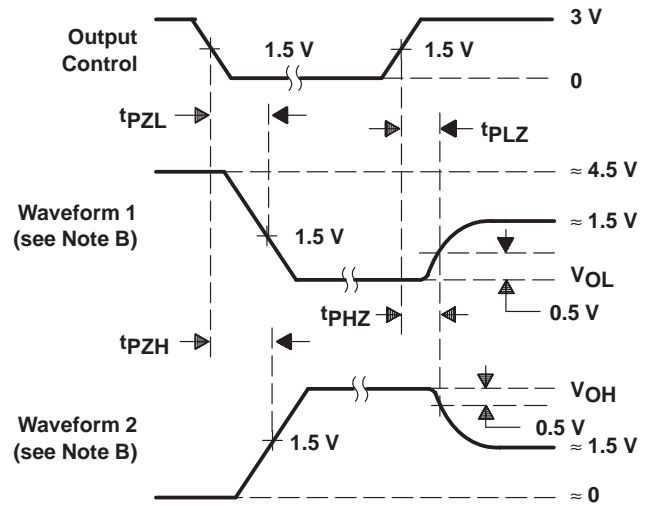
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ALS29863DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS29863DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS29863DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS29863DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS29863DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS29863DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS29863NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS29863NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

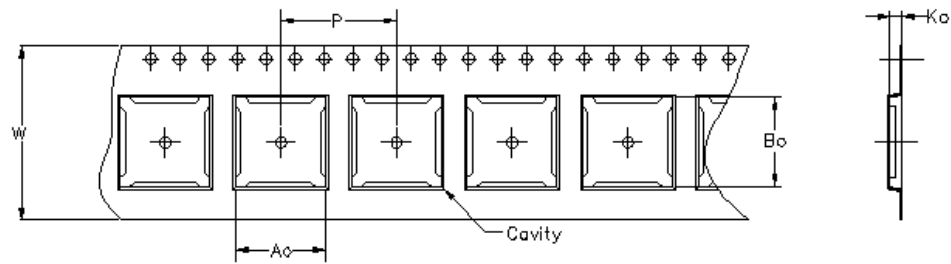
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

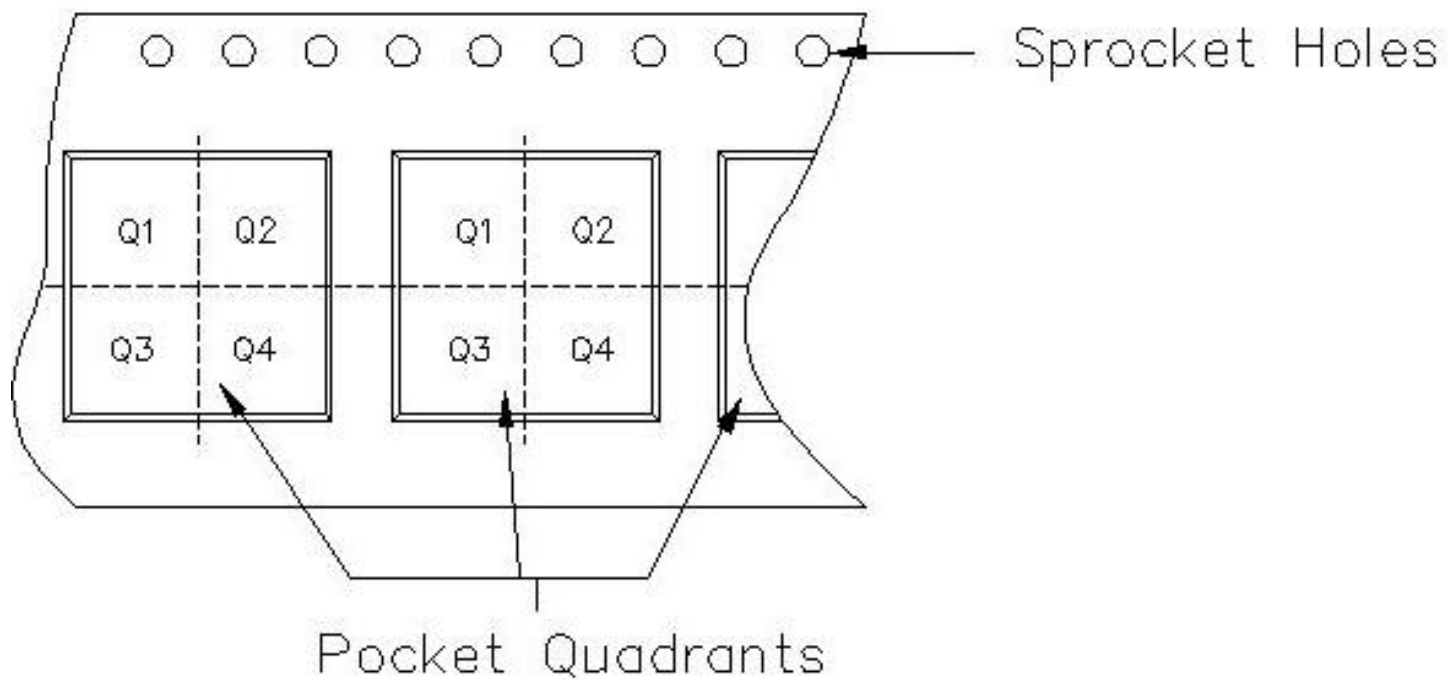
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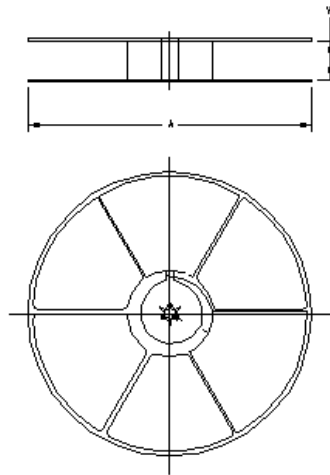
Carrier tape design is defined largely by the component length, width, and thickness.

$A_o$ = Dimension designed to accommodate the component width.
$B_o$ = Dimension designed to accommodate the component length.
$K_o$ = Dimension designed to accommodate the component thickness.
$W$ = Overall width of the carrier tape.
$P$ = Pitch between successive cavity centers.



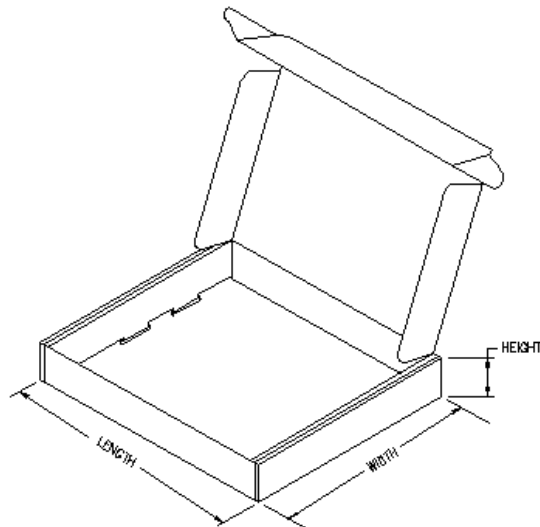
**TAPE AND REEL INFORMATION**

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS29863DWR	DW	24	TAI	330	24	10.75	15.7	2.7	12	24	Q1



**TAPE AND REEL BOX INFORMATION**

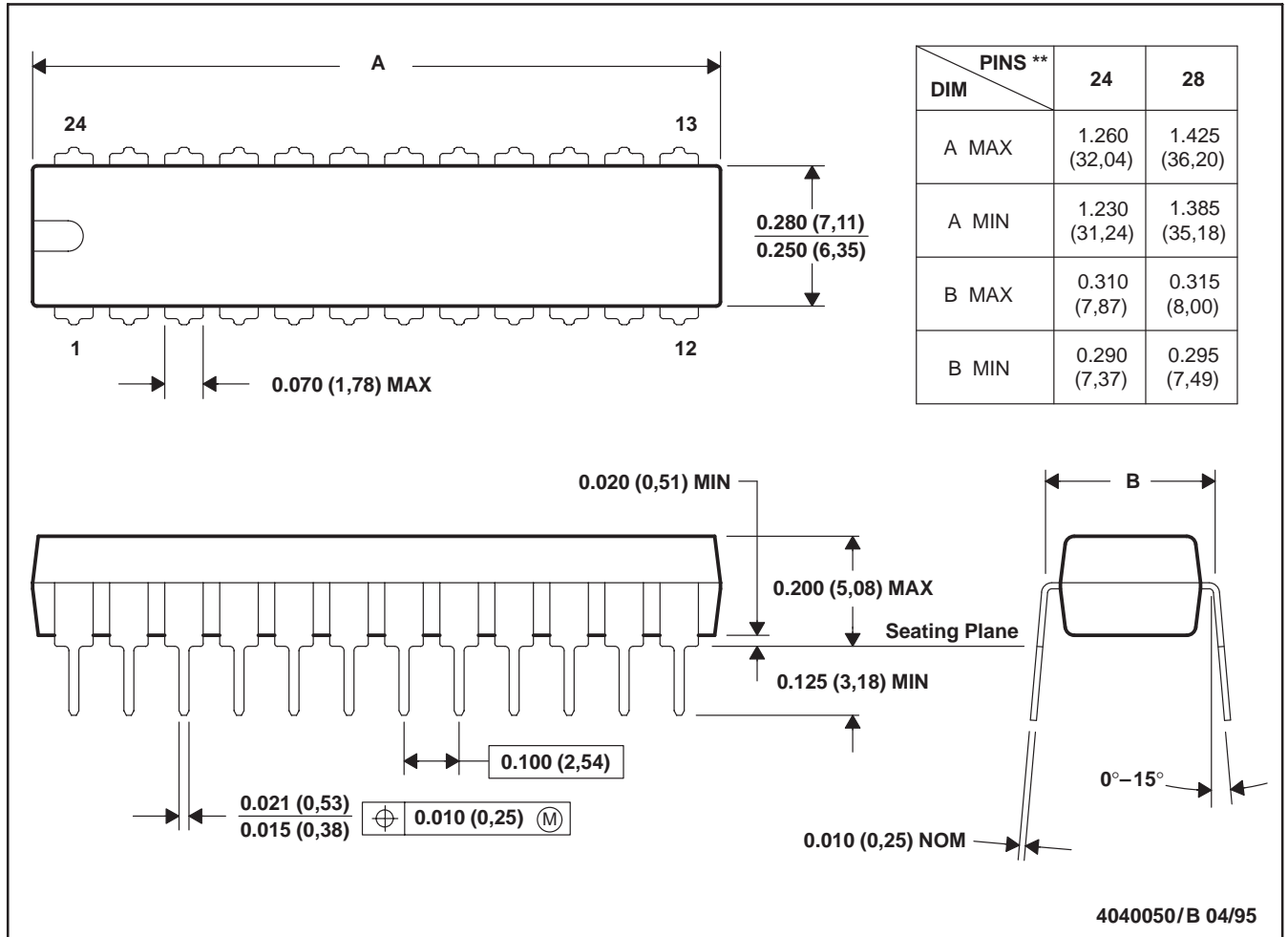
Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74ALS29863DWR	DW	24	TAI	346.0	346.0	41.0



NT (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.



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