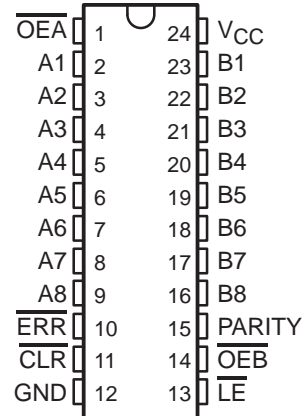


# SN74ALS29854 8-BIT TO 9-BIT PARITY BUS TRANSCEIVER

SDAS118C – FEBRUARY 1987 – REVISED JANUARY 1995

- Functionally Similar to AMD's AM29854
- High-Speed Bus Transceiver With Parity Generator/Checker
- Parity-Error Flag With Open-Collector Outputs
- Latch for Storing the Parity-Error Flag
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

DW OR NT PACKAGE  
(TOP VIEW)



## description

The SN74ALS29854 is an 8-bit to 9-bit parity transceiver designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the parity-error ( $\overline{\text{ERR}}$ ) output indicates whether or not an error in the B data has occurred. The output-enable ( $\overline{\text{OEA}}$ ,  $\overline{\text{OEB}}$ ) inputs can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with an open-collector  $\overline{\text{ERR}}$  flag.  $\overline{\text{ERR}}$  can be either passed, sampled, stored, or cleared from the latch using the latch-enable ( $\overline{\text{LE}}$ ) and clear (CLR) control inputs. When both  $\overline{\text{OEA}}$  and  $\overline{\text{OEB}}$  are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The SN74ALS29854 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						OUTPUT AND I/O				OPERATION
$\overline{\text{OEB}}$	$\overline{\text{OEA}}$	$\overline{\text{CLR}}$	$\overline{\text{LE}}$	Ai Σ of Hs	Bi† Σ of Ls	A	B	PARITY	$\overline{\text{ERR}}‡$	
L	H	X	X	Odd Even	NA	NA	$\overline{\text{A}}$	H L	NA	$\overline{\text{A}}$ data to B bus and generate parity
H	L	X	L	NA	Odd Even	$\overline{\text{B}}$	NA	NA	H L	$\overline{\text{B}}$ data to A bus and check parity
H	L	H	H	NA	X	X	NA	NA	N-1	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error-flag register
H	H	H L X X	H H L L	X X L Odd H Even	X	Z	Z	Z	NC H L H	Isolation§
L	L	X	X	Odd Even	NA	NA	$\overline{\text{A}}$	L H	NA	$\overline{\text{A}}$ data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care

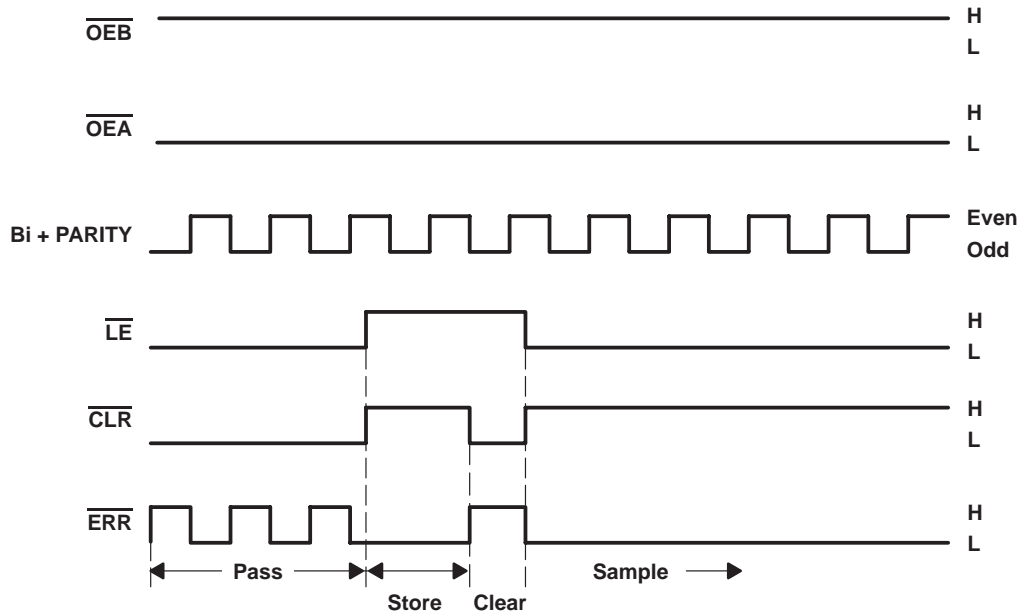
† Summation of high-level inputs includes PARITY along with Bi inputs.

‡ Output states shown assume  $\overline{\text{ERR}}$  was previously high.

§ In this mode,  $\overline{\text{ERR}}$ , when enabled, shows inverted parity of the A bus.



error-flag waveforms



ERROR-FLAG FUNCTIONS

INPUTS		INTERNAL TO DEVICE	OUTPUT PRESTATE	OUTPUT	FUNCTION
$\overline{LE}$	$\overline{CLR}$	POINT P	$\overline{ERR}_{n-1}^\dagger$	$\overline{ERR}$	
L	L	L H	X	L H	Pass
L	H	L X H	X L H	L L H	Sample
H	L	X	X	H	Clear
H	H	X	L H	L H	Store

$^\dagger \overline{ERR}_{n-1}$  represents the state of  $\overline{ERR}$  before any changes at  $\overline{CLR}$ ,  $\overline{LE}$ , or point P.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) $^\ddagger$

- Supply voltage,  $V_{CC}$  ..... 7 V
- Input voltage,  $V_I$  ..... 7 V
- Voltage applied to a disabled I/O port ..... 5.5 V
- Operating free-air temperature range,  $T_A$  ..... 0°C to 70°C
- Storage temperature range ..... -65°C to 150°C

$^\ddagger$  Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# SN74ALS29854

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### recommended operating conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
V <sub>OH</sub>	High-level output voltage, $\overline{\text{ERR}}$			5.5	V
I <sub>OH</sub>	High-level output current			-24	mA
I <sub>OL</sub>	Low-level output current			48	mA
t <sub>w</sub>	Pulse duration	$\overline{\text{LE}}$ high	10		ns
		$\overline{\text{LE}}$ low	10		
		$\overline{\text{CLR}}$ low	10		
t <sub>su</sub>	Setup time before $\overline{\text{LE}}\downarrow$	Bi and PARITY	10		ns
		$\overline{\text{CLR}}$ high	15		
t <sub>h</sub>	Hold time, Bi and PARITY after $\overline{\text{LE}}\downarrow$	3			ns
T <sub>A</sub>	Operating free-air temperature	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 4.75 V,	I <sub>I</sub> = -18 mA			-1.2	V
V <sub>OH</sub>	All I/Os except $\overline{\text{ERR}}$	V <sub>CC</sub> = 4.75 V	I <sub>OH</sub> = -15 mA	2.4			V
			I <sub>OH</sub> = -24 mA	2			
I <sub>OH</sub>	$\overline{\text{ERR}}$	V <sub>CC</sub> = 4.75 V,	V <sub>OH</sub> = 5.5 V			0.1	mA
V <sub>OL</sub>		V <sub>CC</sub> = 4.75 V,	I <sub>OL</sub> = 48 mA	0.35	0.5		V
I <sub>I</sub>		V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 5.5 V			0.1	mA
I <sub>IH</sub> ‡		V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 2.7 V			20	μA
I <sub>IL</sub> ‡	Data	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 0.4 V			-0.2	mA
	Control					-0.75	
I <sub>O</sub> §		V <sub>CC</sub> = 5.25 V,	V <sub>O</sub> = 0	-75		-250	mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.25 V,	All outputs open		70	100	mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ For I/O ports, the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I<sub>OS</sub>.



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## switching characteristics (see Figure 1)

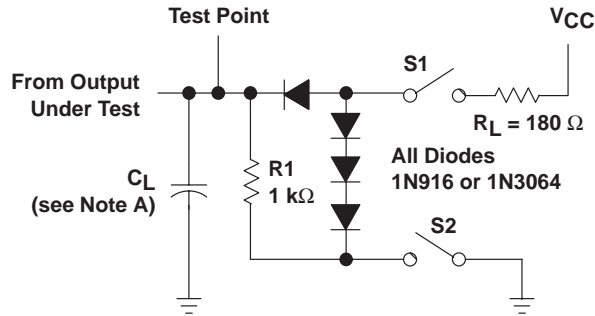
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CC} = 4.75 \text{ V to } 5.25 \text{ V},$ $T_A = \text{MIN to MAX}^\dagger$		UNIT
				MIN	MAX	
t <sub>PLH</sub>	A or B	B or A	C <sub>L</sub> = 50 pF	8		ns
t <sub>PHL</sub>				8		
t <sub>PLH</sub>	A or B	B or A	C <sub>L</sub> = 300 pF	13		ns
t <sub>PHL</sub>				13		
t <sub>PLH</sub>	A	PARITY	C <sub>L</sub> = 50 pF	15		ns
t <sub>PHL</sub>				18		
t <sub>PLH</sub>	A	PARITY	C <sub>L</sub> = 300 pF	22		ns
t <sub>PHL</sub>				22		
t <sub>PZH</sub>	$\overline{OE}A$ or $\overline{OE}B$	A or B	C <sub>L</sub> = 50 pF	17		ns
t <sub>PZL</sub>				17		
t <sub>PZH</sub>	$\overline{OE}A$ or $\overline{OE}B$	A or B	C <sub>L</sub> = 300 pF	23		ns
t <sub>PZL</sub>				23		
t <sub>PHZ</sub>	$\overline{OE}A$ or $\overline{OE}B$	A or B	C <sub>L</sub> = 5 pF	8		ns
t <sub>PLZ</sub>				8		
t <sub>PHZ</sub>	$\overline{OE}A$ or $\overline{OE}B$	A or B	C <sub>L</sub> = 50 pF	15		ns
t <sub>PLZ</sub>				8		
t <sub>PHL</sub>	$\overline{LE}$	$\overline{ERR}$	C <sub>L</sub> = 50 pF	12		ns
t <sub>PLH</sub>	$\overline{CLR}$	$\overline{ERR}$	C <sub>L</sub> = 50 pF	12		ns
t <sub>PLH</sub>	$\overline{OE}A$	PARITY	C <sub>L</sub> = 50 pF	17		ns
t <sub>PHL</sub>				19		
t <sub>PLH</sub>	$\overline{OE}A$	PARITY	C <sub>L</sub> = 300 pF	22		ns
t <sub>PHL</sub>				25		
t <sub>PLH</sub>	Bi/PARITY	$\overline{ERR}$	C <sub>L</sub> = 50 pF	20		ns
t <sub>PHL</sub>				20		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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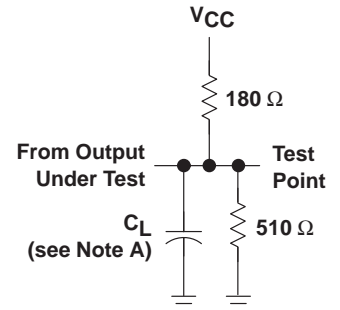
## PARAMETER MEASUREMENT INFORMATION



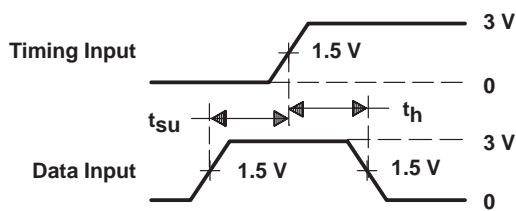
**LOAD CIRCUIT 1**  
ALL OUTPUTS EXCEPT FOR ERROR FLAG

**SWITCH POSITION TABLE**

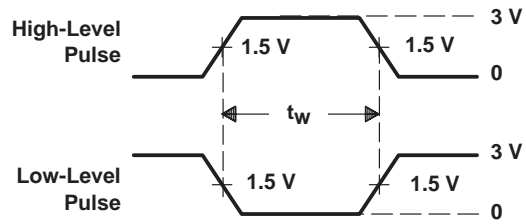
TEST	S1	S2
t <sub>PLH</sub>	Closed	Closed
t <sub>PHL</sub>	Closed	Closed
t <sub>PZH</sub>	Open	Closed
t <sub>PZL</sub>	Closed	Open
t <sub>PHZ</sub>	Closed	Closed
t <sub>PLZ</sub>	Closed	Closed



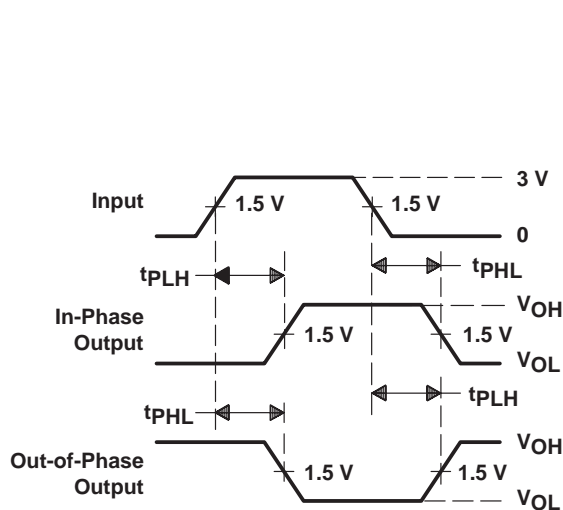
**LOAD CIRCUIT 2**  
ERROR-FLAG OUTPUT



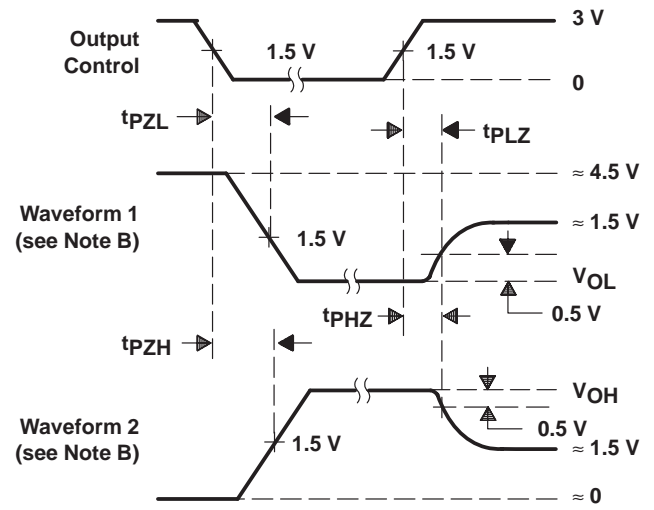
**VOLTAGE WAVEFORMS**  
SETUP AND HOLD TIMES



**VOLTAGE WAVEFORMS**  
PULSE DURATIONS



**VOLTAGE WAVEFORMS**  
PROPAGATION DELAY TIMES



**VOLTAGE WAVEFORMS**  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.

**Figure 1. Load Circuits and Voltage Waveforms**

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