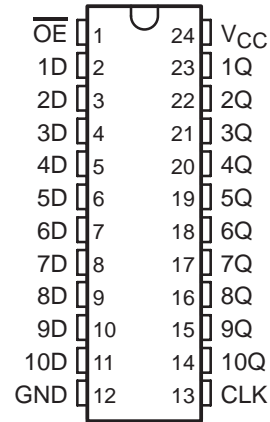


# SN54ALS29821, SN74ALS29821 10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS145B – JANUARY 1986 – REVISED JANUARY 1995

- Functionally Equivalent to AMD's AM29821
- Provide Extra Data Width Necessary for Wider Address/Data Paths or Buses With Parity
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs Reduce dc Loading Effects
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

SN54ALS29821 . . . JT PACKAGE  
SN74ALS29821 . . . DW OR NT PACKAGE  
(TOP VIEW)



## description

These 10-bit edge-triggered D-type flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are true to the data (D) input.

A buffered output-enable ( $\overline{OE}$ ) input can place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. The outputs also are in the high-impedance state during power-up and power-down conditions. The outputs remain in the high-impedance state while the device is powered down. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS29821 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS29821 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

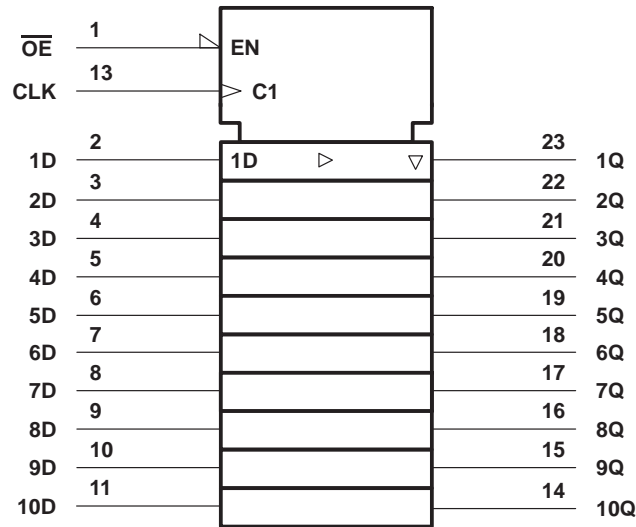
FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	L	X	$Q_0$
H	X	X	Z

# SN54ALS29821, SN74ALS29821 10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

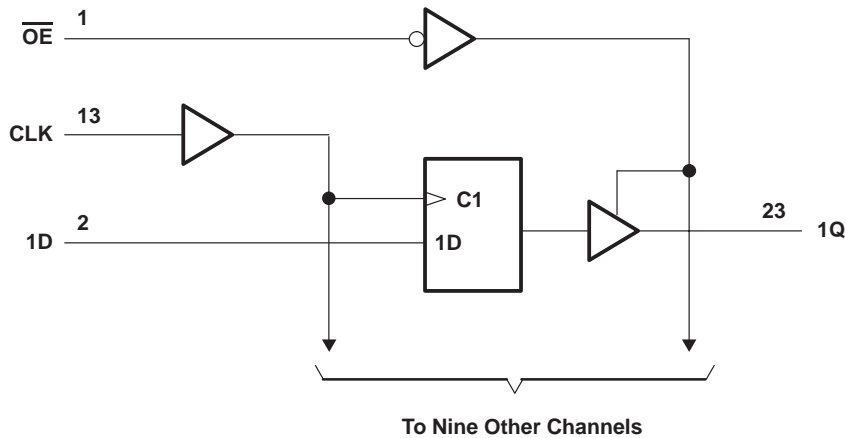
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS29821	-55°C to 125°C
SN74ALS29821	0°C to 70°C
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



# SN54ALS29821, SN74ALS29821 10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

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## recommended operating conditions

		SN54ALS29821			SN74ALS29821			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{OH}$	High-level output current			-24			-24	mA
$I_{OL}$	Low-level output current			48			48	mA
$t_w$	Pulse duration, CLK high or low	7			7			ns
$t_{su}$	Setup time, data before CLK $\uparrow$	4			4			ns
$t_h$	Hold time, data after CLK $\uparrow$	2			2			ns
$T_A$	Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS29821			SN74ALS29821			UNIT		
		MIN	TYP $\dagger$	MAX	MIN	TYP $\dagger$	MAX			
$V_{IK}$	$V_{CC} = 4.75\text{ V}$ , $I_I = -18\text{ mA}$			-1.2			-1.2	V		
$V_{OH}$	$V_{CC} = 4.75\text{ V}$			2.4	3.3		2.4	3.3	V	
				2	3.1		2	3.1		
$V_{OL}$	$V_{CC} = 4.75\text{ V}$ , $I_{OL} = 48\text{ mA}$			0.35	0.5		0.35	0.5	V	
$I_{OZH}$	$V_{CC} = 5.25\text{ V}$ , $V_O = 2.4\text{ V}$						50	20	$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 5.25\text{ V}$ , $V_O = 0.4\text{ V}$						-50	-20	$\mu\text{A}$	
$I_I$	$V_{CC} = 5.25\text{ V}$ , $V_I = 5.5\text{ V}$						0.1	0.1	mA	
$I_{IH}$	$V_{CC} = 5.25\text{ V}$ , $V_I = 2.7\text{ V}$						20	20	$\mu\text{A}$	
$I_{IL}$	$V_{CC} = 5.25\text{ V}$ , $V_I = 0.4\text{ V}$						-0.5	-0.2	mA	
$I_{OS}^\ddagger$	$V_{CC} = 5.25\text{ V}$ , $V_O = 0$			-75			-250	-75	-250	mA
$I_{CC}$	$V_{CC} = 5.25\text{ V}$ , Outputs open			80	115		80	115	mA	

$\dagger$  All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

$\ddagger$  Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.



# SN54ALS29821, SN74ALS29821 10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS145B – JANUARY 1986 – REVISED JANUARY 1995

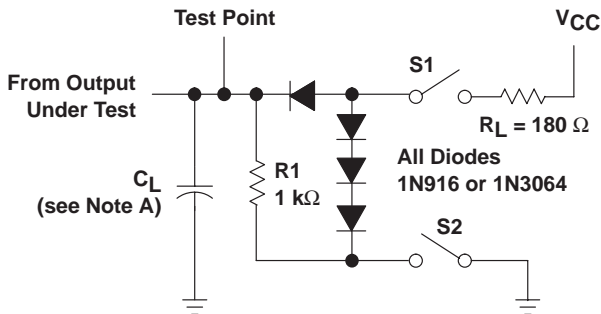
## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V <sub>CC</sub> = MIN to MAX†, T <sub>A</sub> = MIN to MAX†				UNIT
				SN54ALS29821		SN74ALS29821		
				MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	CLK	Any Q	C <sub>L</sub> = 50 pF	2	11.5	2	10	ns
t <sub>PHL</sub>				2	11.5	2	10	
t <sub>PLH</sub>	CLK	Any Q	C <sub>L</sub> = 300 pF	2	21	16		ns
t <sub>PHL</sub>				2	21	16		
t <sub>PZH</sub>	$\overline{OE}$	Any Q	C <sub>L</sub> = 50 pF	1	17	14		ns
t <sub>PZL</sub>				1	17	14		
t <sub>PZH</sub>	$\overline{OE}$	Any Q	C <sub>L</sub> = 300 pF	1	25	20		ns
t <sub>PZL</sub>				1	29.5	23		
t <sub>PHZ</sub>	$\overline{OE}$	Any Q	C <sub>L</sub> = 50 pF	1	16	14		ns
t <sub>PLZ</sub>				1	14	12		
t <sub>PHZ</sub>	$\overline{OE}$	Any Q	C <sub>L</sub> = 5 pF	1	12	9		ns
t <sub>PLZ</sub>				1	11	9		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



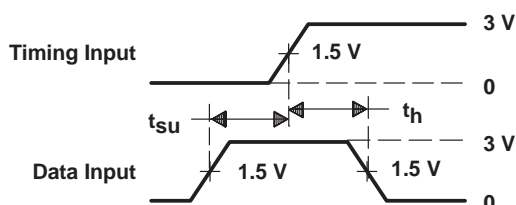
PARAMETER MEASUREMENT INFORMATION



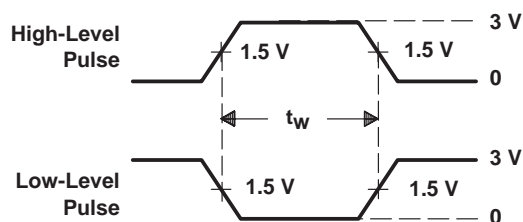
LOAD CIRCUIT

SWITCH POSITION TABLE

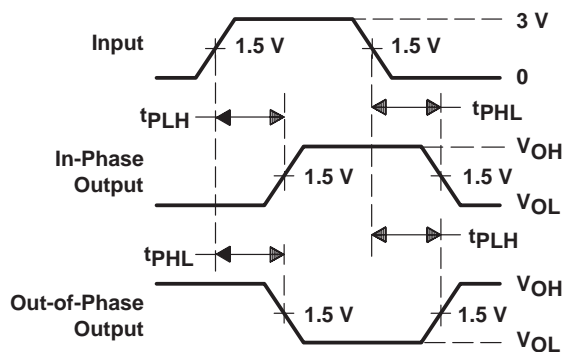
TEST	S1	S2
t <sub>PLH</sub>	Closed	Closed
t <sub>PHL</sub>	Closed	Closed
t <sub>PZH</sub>	Open	Closed
t <sub>PZL</sub>	Closed	Open
t <sub>PHZ</sub>	Closed	Closed
t <sub>PLZ</sub>	Closed	Closed



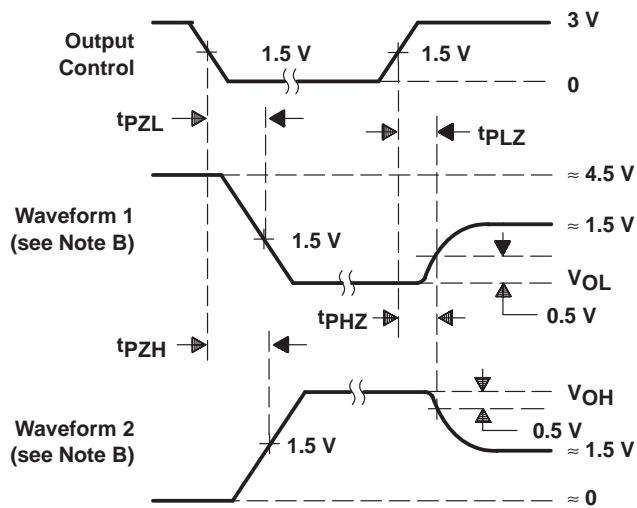
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9061601LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9061601LA SNJ54ALS29821J T	<a href="#">Samples</a>
SN74ALS29821DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS29821	<a href="#">Samples</a>
SN74ALS29821NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS29821NT	<a href="#">Samples</a>
SNJ54ALS29821JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9061601LA SNJ54ALS29821J T	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ALS29821, SN74ALS29821 :**

- Catalog: [SN74ALS29821](#)
- Military: [SN54ALS29821](#)

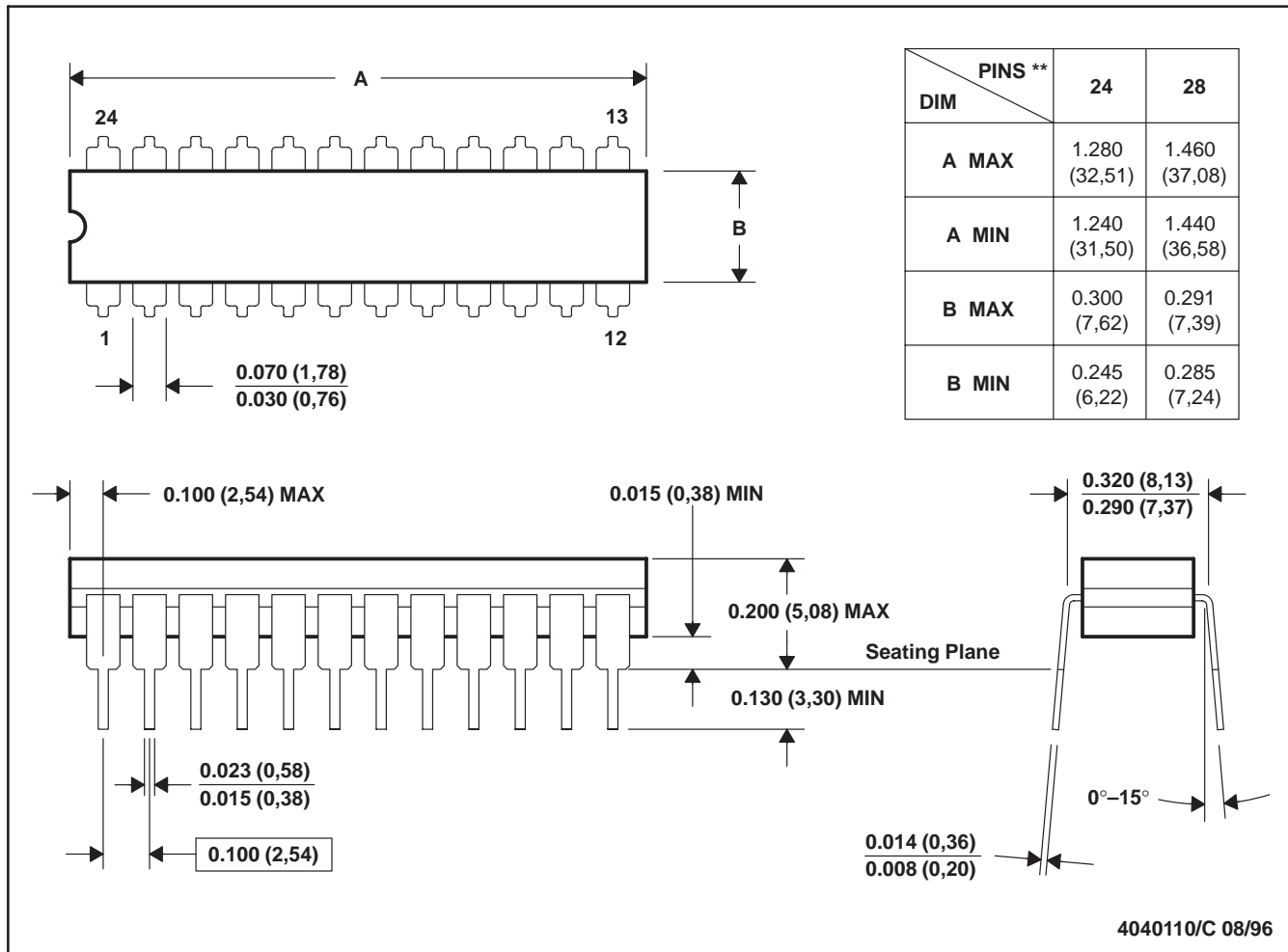
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

JT (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN

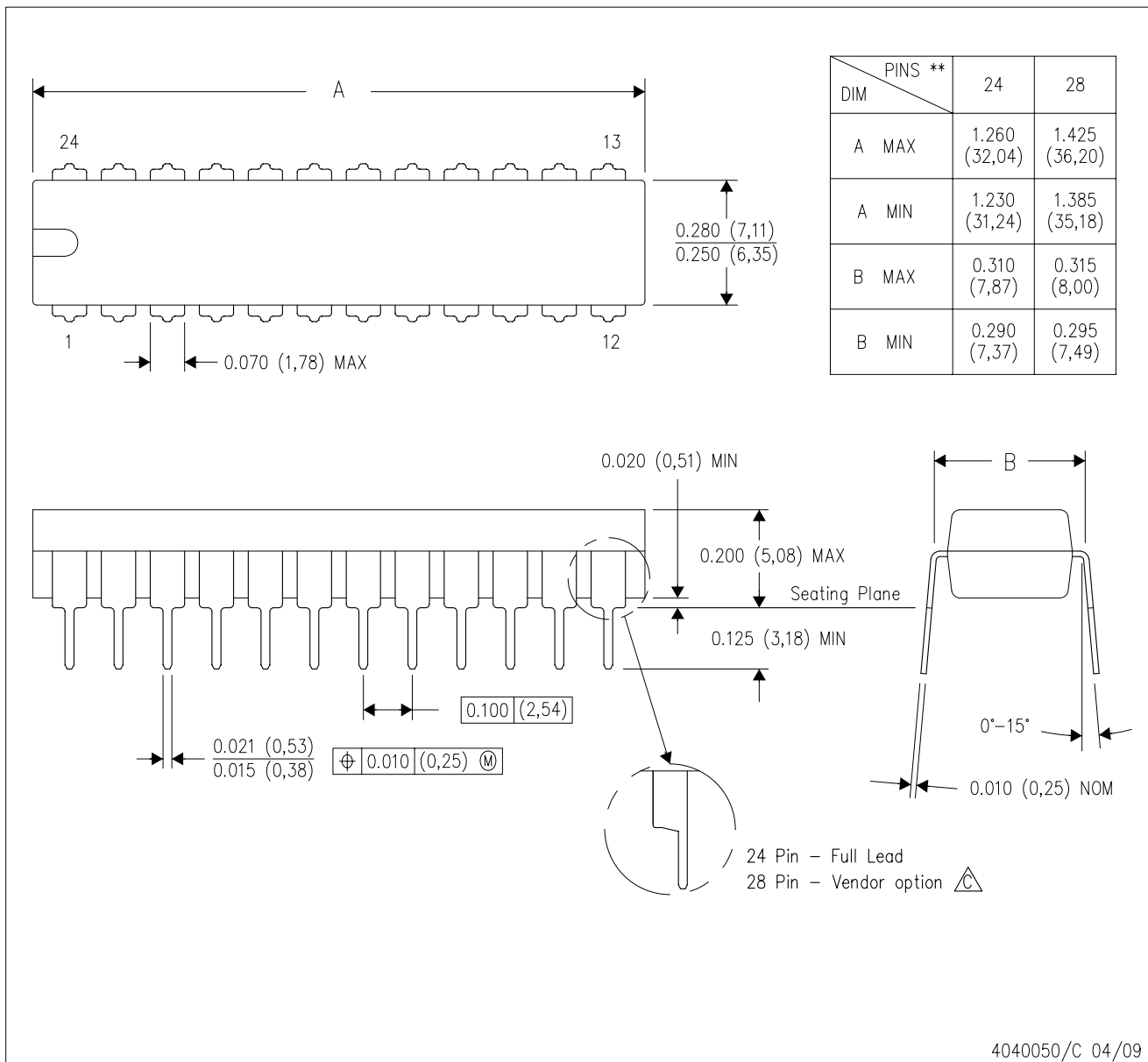



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

# MECHANICAL DATA

NT (R-PDIP-T\*\*) 24 PINS SHOWN

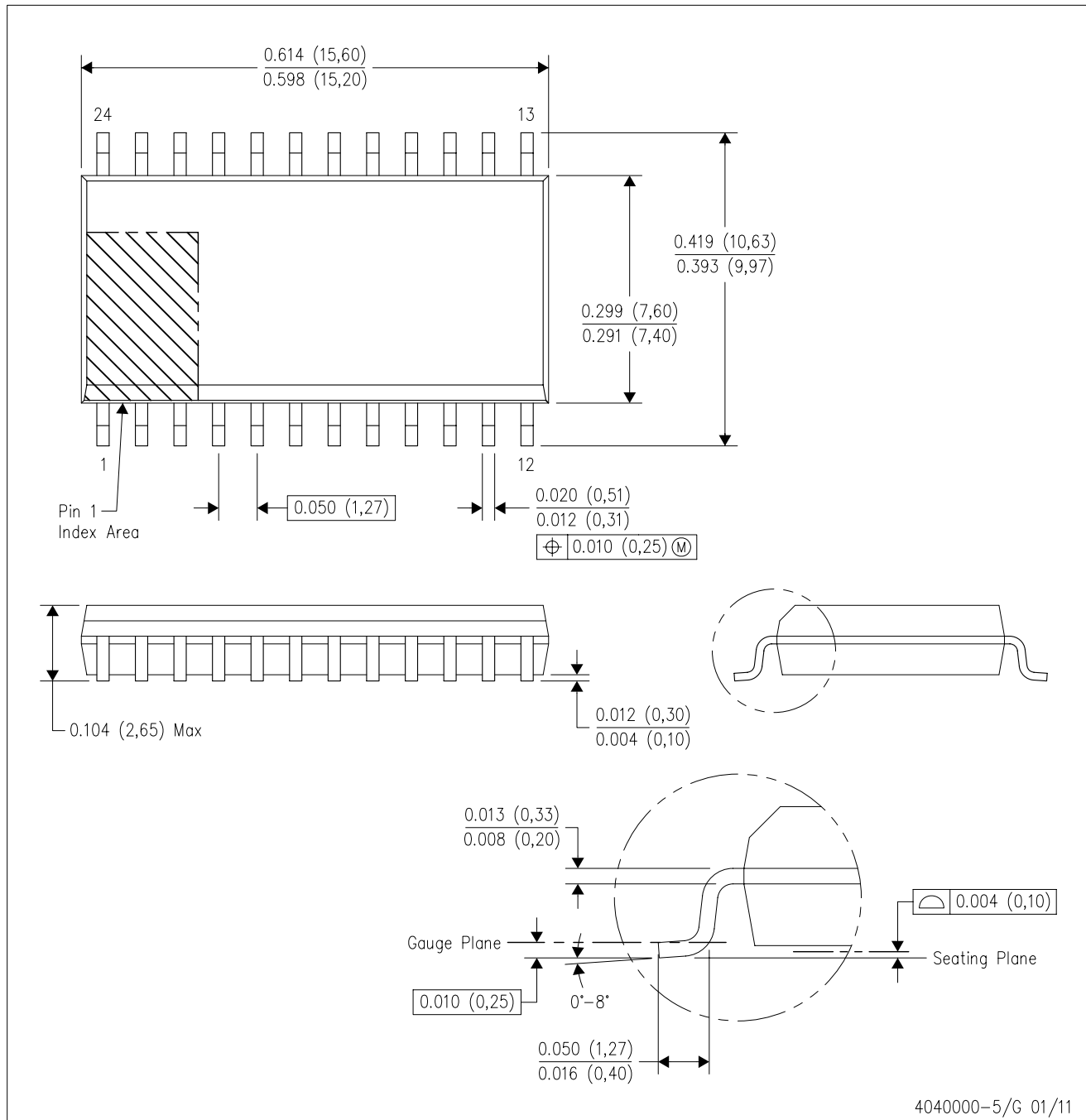
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

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