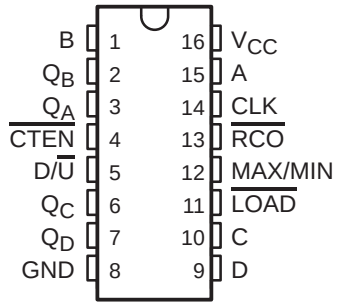
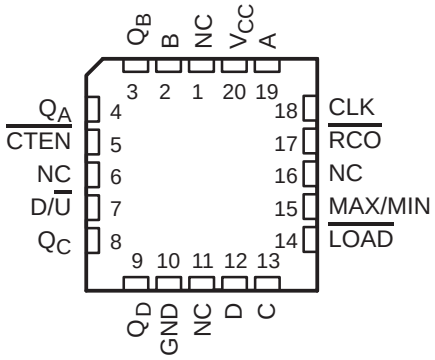
- **Single Down/Up Count-Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable With Load Control**
- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54ALS191A . . . J PACKAGE
SN74ALS191A . . . D OR N PACKAGE
(TOP VIEW)



SN54ALS191A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’ALS191A are synchronous 4-bit reversible up/down binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock (CLK) input if the count enable ($\overline{CTEN}$) input is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up, and when D/$\overline{U}$ is high, the counter counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and D/$\overline{U}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter is dictated solely by the conditions meeting the stable setup and hold times.

These counters are fully programmable. Each output can be preset to either level by placing a low on the $\overline{LOAD}$ input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

CLK, D/$\overline{U}$, and $\overline{LOAD}$ are buffered to lower the drive requirement, which significantly reduces the loading on (current required by) clock drivers, for long parallel words.

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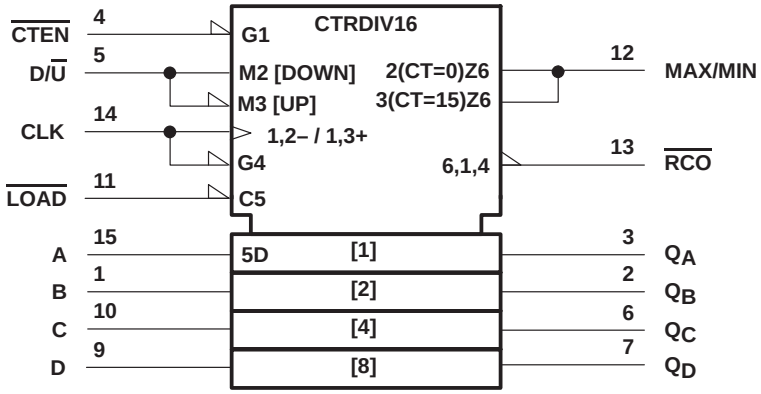
description (continued)

Two outputs are available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is minimum (0) counting down or maximum (15) counting up. The ripple-clock output ($\overline{RCO}$) produces a low-level output pulse under those same conditions, but only while the clock input is low. The counter easily can be cascaded by feeding the ripple-clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count (MAX/MIN) output can be used to accomplish look ahead for high-speed operation.

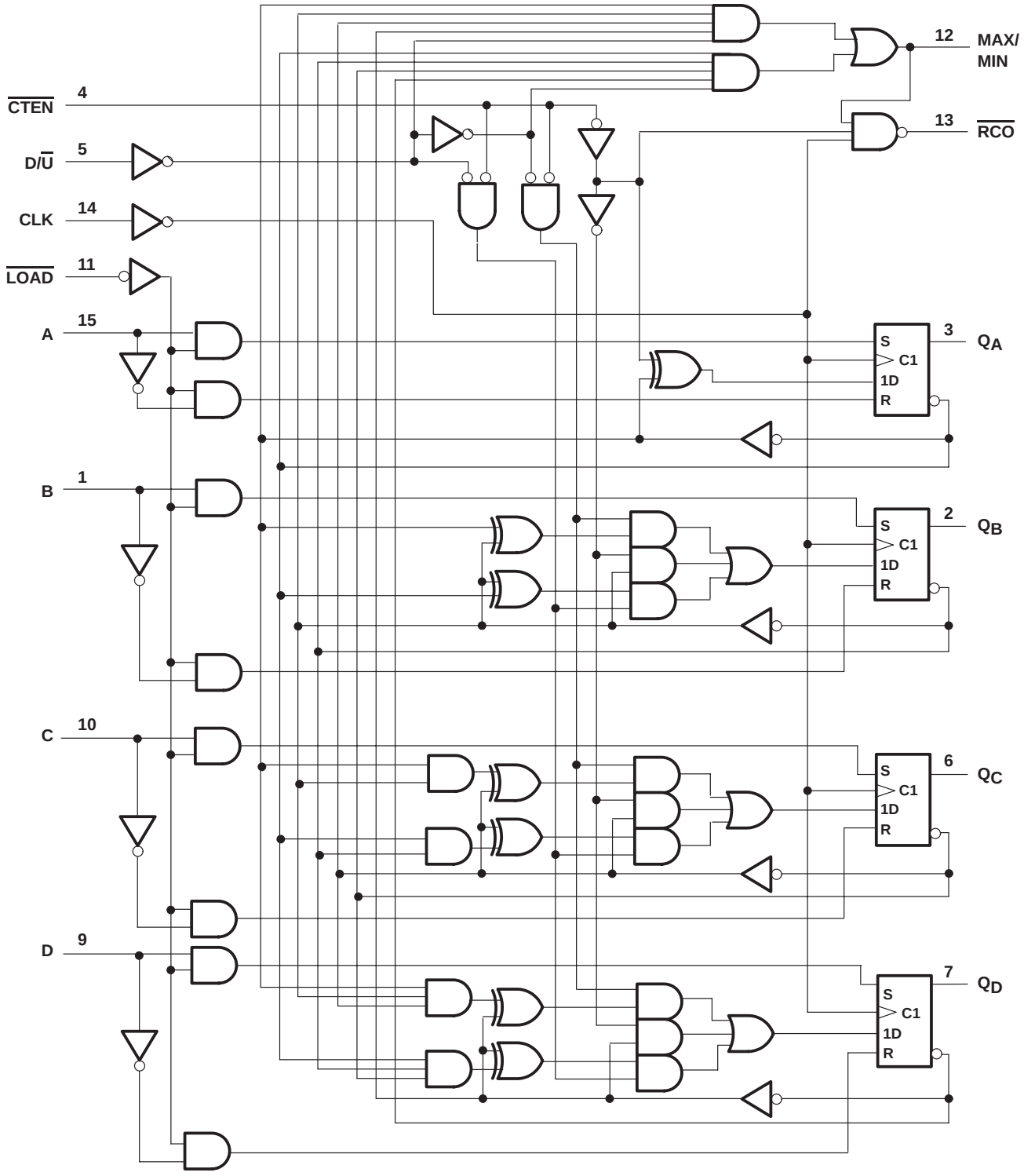
The SN54ALS191A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS191A is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)

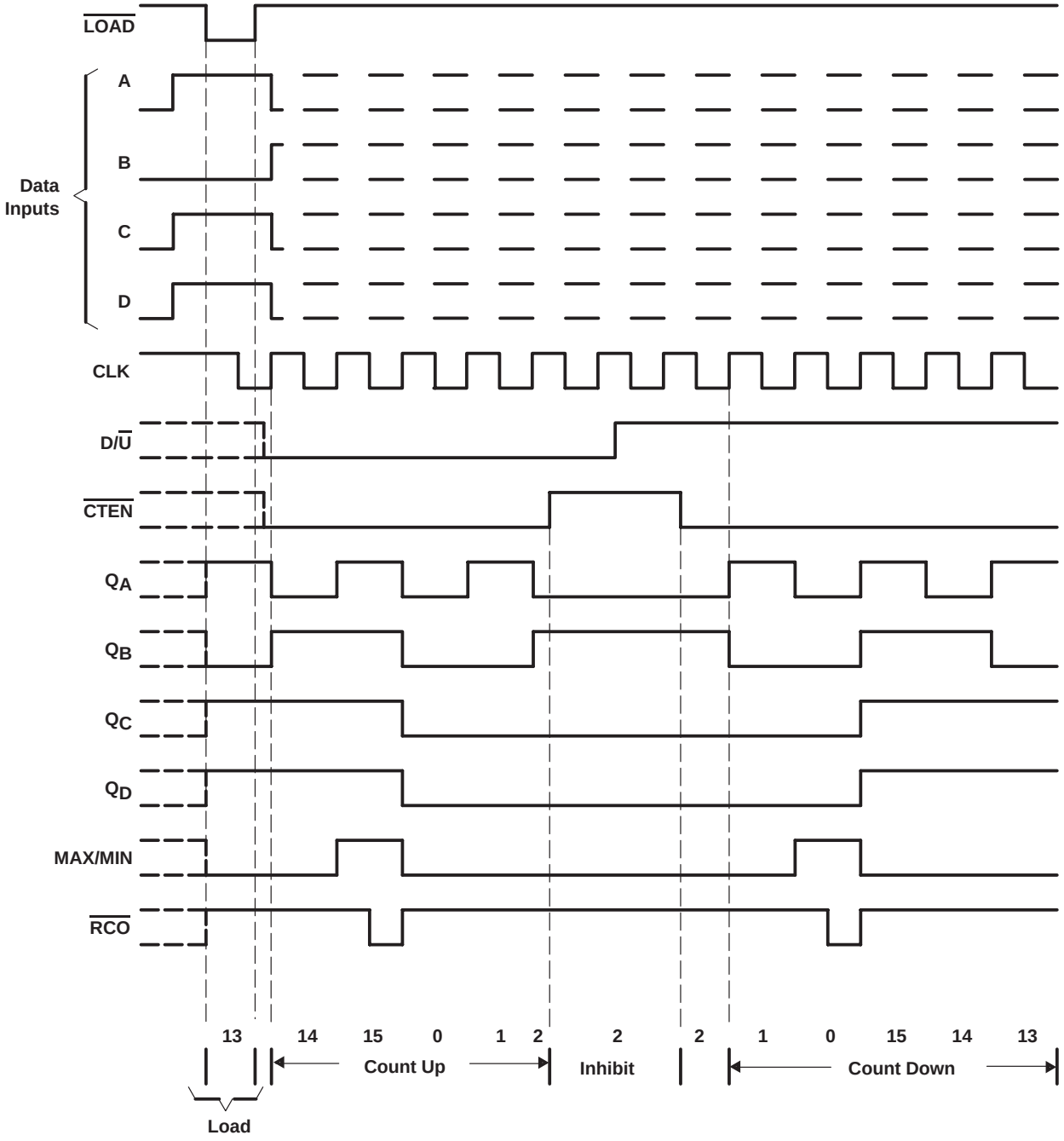


Pin numbers shown are for the D, J, and N packages.

typical load, count, and inhibit sequences

The following sequence is illustrated below:

1. Load (preset) to binary 13
2. Count up to 14, 15 (maximum), 0, 1, and 2
3. Inhibit
4. Count down to 1, 0 (minimum), 15, 14, and 13



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Operating free-air temperature range, T_A: SN54ALS191A . . . . . –55°C to 125°C
SN74ALS191A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS191A			SN74ALS191A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				–0.4			–0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		20	0		30	MHz
t_w	Pulse duration	CLK high or low	20			16.5			ns
		$\overline{\text{LOAD}}$ low	25			20			
t_{su}	Setup time	Data before $\overline{\text{LOAD}}\uparrow$	25			20			ns
		$\overline{\text{CTEN}}$ before CLK$\uparrow$	45			20			
		D/$\overline{\text{U}}$ before CLK$\uparrow$	30			20			
		$\overline{\text{LOAD}}$ inactive before CLK$\uparrow$	20			20			
t_h	Hold time	Data after $\overline{\text{LOAD}}\uparrow$	5			5			ns
		$\overline{\text{CTEN}}$ after CLK$\uparrow$	0			0			
		D/$\overline{\text{U}}$ after CLK$\uparrow$	0			0			
T_A	Operating free-air temperature		–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS191A			SN74ALS191A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.5			–1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC} – 2			V_{CC} – 2			V
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
			I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	$\overline{CTEN}$ or CLK	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.2			–0.2	mA
	All others					–0.2			–0.1	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	–20		–112	–30		– 112	mA
I_{CC}		V_{CC} = 5.5 V,	All inputs at 0		12	22		12	22	mA

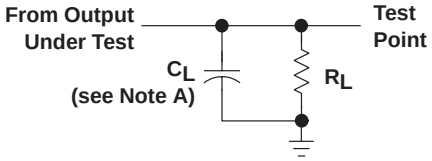
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

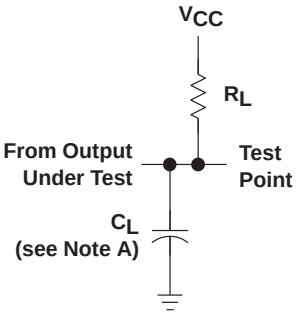
PARAMETER	FROM (OUTPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			SN54ALS191A		SN74ALS191A		
			MIN	MAX	MIN	MAX	
f_{max}			20		30		MHz
t_{PLH}	$\overline{LOAD}$	Any Q	7	37	7	30	ns
t_{PHL}			8	34	8	30	
t_{PLH}	A, B, C, D	Any Q	3	25	3	21	ns
t_{PHL}			4	25	4	21	
t_{PLH}	CLK	$\overline{RCO}$	5	24	5	20	ns
t_{PHL}			5	25	5	20	
t_{PLH}	CLK	Any Q	3	26	3	18	ns
t_{PHL}			3	22	3	18	
t_{PLH}	CLK	MAX/MIN	8	37	8	31	ns
t_{PHL}			8	34	8	31	
t_{PLH}	D/$\overline{U}$	$\overline{RCO}$	8	45	8	37	ns
t_{PHL}			10	36	10	28	
t_{PLH}	D/$\overline{U}$	MAX/MIN	8	35	8	25	ns
t_{PHL}			8	30	8	25	
t_{PLH}	$\overline{CTEN}$	$\overline{RCO}$	4	21	4	18	ns
t_{PHL}			4	23	4	18	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

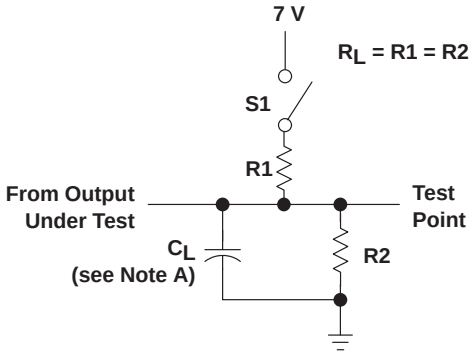
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



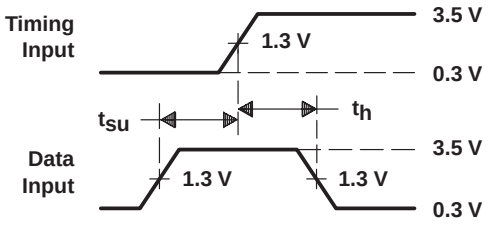
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



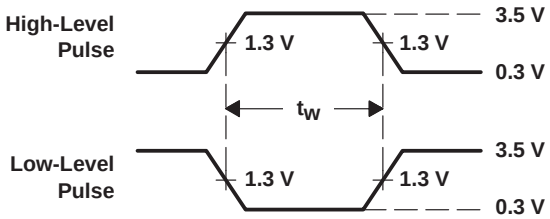
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



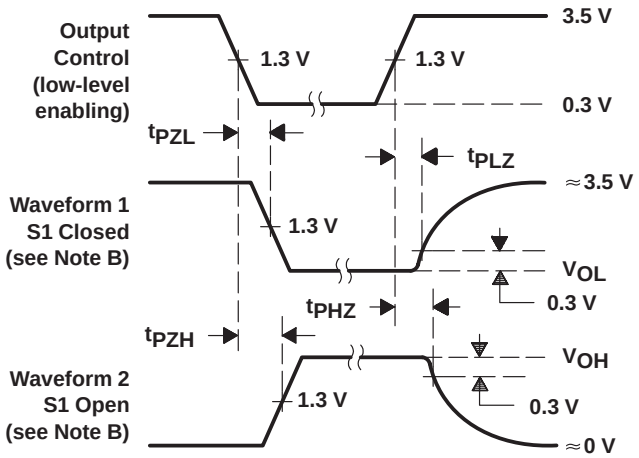
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



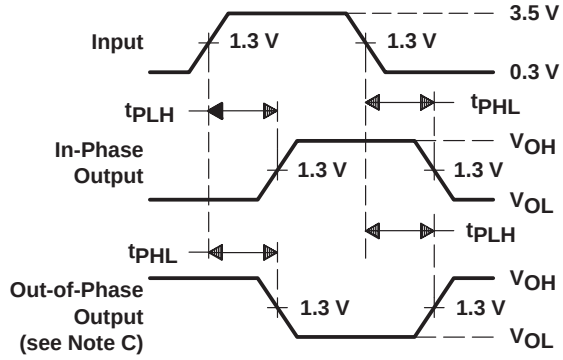
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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