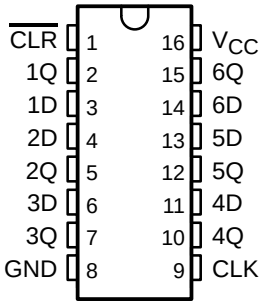
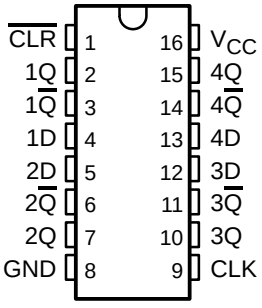
- **'ALS174 and 'AS174 Contain Six Flip-Flops With Single-Rail Outputs**
- **'ALS175 and 'AS175B Contain Four Flip-Flops With Double-Rail Outputs**
- **Buffered Clock and Direct-Clear Inputs**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Fully Buffered Outputs for Maximum Isolation From External Disturbances ('AS Only)**

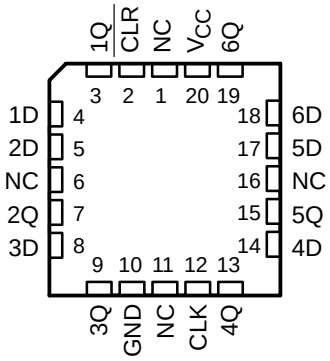
SN54ALS174 . . . J OR W PACKAGE
SN54AS174 . . . J PACKAGE
SN74ALS174, SN74AS174 . . . D , N, OR NS PACKAGE
(TOP VIEW)



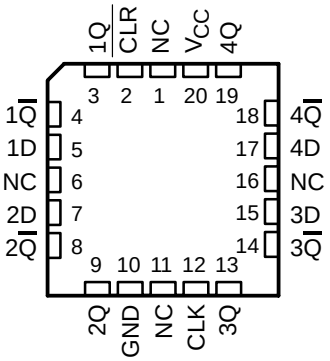
SN54ALS175 . . . J OR W PACKAGE
SN54AS175B . . . J PACKAGE
SN74ALS175, SN74AS175B . . . D, N, OR NS PACKAGE
(TOP VIEW)



SN54ALS174, SN54AS174 . . . FK PACKAGE
(TOP VIEW)



SN54ALS175 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct-clear ($\overline{CLR}$) input. The 'ALS175 and 'AS175B feature complementary outputs from each flip-flop.

Information at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS174N	SN74ALS174N
			SN74AS174N	SN74AS174N
			SN74ALS175N	SN74ALS175N
			SN74AS175BN	SN74AS175BN
	SOIC – D	Tube	SN74ALS174D	ALS174
		Tape and reel	SN74ALS174DR	
		Tube	SN74AS174D	AS174
		Tape and reel	SN74AS174DR	
		Tube	SN74ALS175D	ALS175
		Tape and reel	SN74ALS175DR	
		Tube	SN74AS175BD	AS175B
		Tape and reel	SN74AS175BDR	
	SOP – NS	Tape and reel	SN74ALS174NSR	ALS174
			SN74AS174NSR	74AS174
			SN74ALS175NSR	ALS175
			SN74AS175BNSR	74AS175B
–55°C to 125°C	CDIP – J	Tube	SNJ54ALS174J	SNJ54ALS174J
			SNJ54AS174J	SNJ54AS174J
			SNJ54ALS175J	SNJ54ALS175J
			SNJ54AS175BJ	SNJ54AS175BJ
	CFP – W	Tube	SNJ54ALS174W	SNJ54ALS174W
			SNJ54ALS175W	SNJ54ALS175W
	LCCC – FK	Tube	SNJ54ALS174FK	SNJ54ALS174FK
			SNJ54AS174FK‡	SNJ54AS174FK
			SNJ54ALS175FK	SNJ54ALS175FK

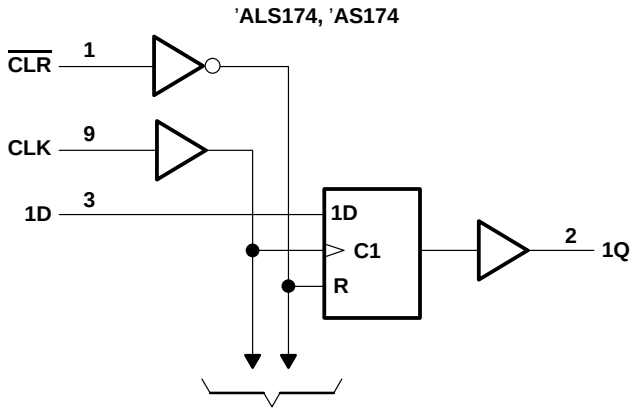
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
‡ This orderable is not recommended for new designs.

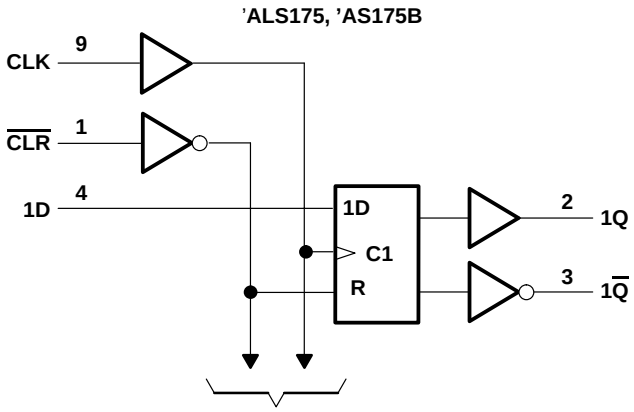
FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$§
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

§ 'ALS175 and 'AS175B only

logic diagrams (positive logic)





Pin numbers shown are for the D, J, N, NS, and W packages.

absolute maximum ratings over operating free-air temperature range, SN54/74ALS174, SN54/74ALS175 (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Package thermal impedance, θ_{JA} (see Note 1): D package . . . . . 73°C/W
N package . . . . . 67°C/W
NS package . . . . . 64°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.5			–1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC}–2			V_{CC}–2			V
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	All others	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.1			–0.1	mA
	CLK					–0.15				
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	–20		–112	–30		–112	mA
I_{CC}	’ALS174	V_{CC} = 5.5 V,	See Note 3		11	19		11	19	mA
	’ALS175				8	14		9	14	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.
NOTE 3: I_{CC} is measured with D inputs and $\overline{CLR}$ grounded, and CLK at 4.5 V.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54ALS174 SN54ALS175		SN74ALS174 SN74ALS175		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			40		50	MHz
t_w	Pulse duration	$\overline{CLR}$ low	15		10		ns
		CLK high	12.5		10		
		CLK low	12.5		10		
t_{su}	Setup time before CLK↑	Data	15		10		ns
		$\overline{CLR}$ inactive	8		6		
t_h	Hold time, data after CLK↑		0		0		ns

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§				UNIT
			SN54ALS174 SN54ALS175		SN74ALS174 SN74ALS175		
			MIN	MAX	MIN	MAX	
f_{max}			40		50		MHz
t_{PLH}	$\overline{CLR}$	Any Q (or $\overline{Q}$, ’ALS175)	3	20	5	18	ns
t_{PHL}			5	30	8	23	
t_{PLH}	CLK	Any Q (or $\overline{Q}$, ’ALS175)	3	20	3	15	ns
t_{PHL}			5	24	5	17	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.