

SN74ALS166 PARALLEL-LOAD 8-BIT SHIFT REGISTER

SDAS156D – APRIL 1982 – REVISED AUGUST 2000

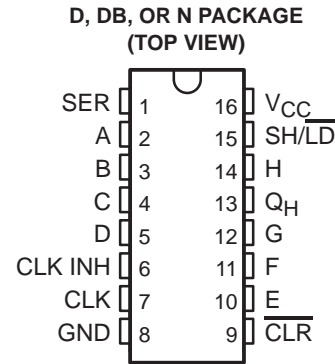
- Synchronous Load
- Direct Overriding Clear
- Parallel-to-Serial Conversion
- Package Options Include Plastic Small-Outline (D) and Shrink Small-Outline (DB) Packages and Standard Plastic (N) DIP

description

The SN74ALS166 parallel-load 8-bit shift register is compatible with most other TTL logic families. All inputs are buffered to lower the drive requirements. Input clamping diodes minimize switching transients and simplify system design.

These parallel-in or serial-in, serial-out registers have a complexity of 77 equivalent gates on the chip. They feature gated clocks (CLK and CLK INH) inputs and an overriding clear ($\overline{\text{CLR}}$) input. The parallel-in or serial-in modes are established by the shift/load ($\text{SH}/\overline{\text{LD}}$) input. When high, $\text{SH}/\overline{\text{LD}}$ enables the serial data (SER) input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data (A–H) inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive-NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running and the register can be stopped on command with the clock input. CLK INH should be changed to the high level only when CLK is high. The buffered $\overline{\text{CLR}}$ overrides all other inputs, including CLK, and sets all flip-flops to zero.

The SN74ALS166 is characterized for operation from 0°C to 70°C.



FUNCTION TABLE

INPUTS					PARALLEL A . . . H	INTERNAL OUTPUTS		OUTPUT Q _H
$\overline{\text{CLR}}$	$\text{SH}/\overline{\text{LD}}$	CLK INH	CLK	SER		Q _A	Q _B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q _{A0}	Q _{B0}	Q _{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q _{An}	Q _{Gn}
H	H	L	↑	L	X	L	Q _{An}	Q _{Gn}
H	X	H	↑	X	X	Q _{A0}	Q _{B0}	Q _{H0}



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 **TEXAS
INSTRUMENTS**

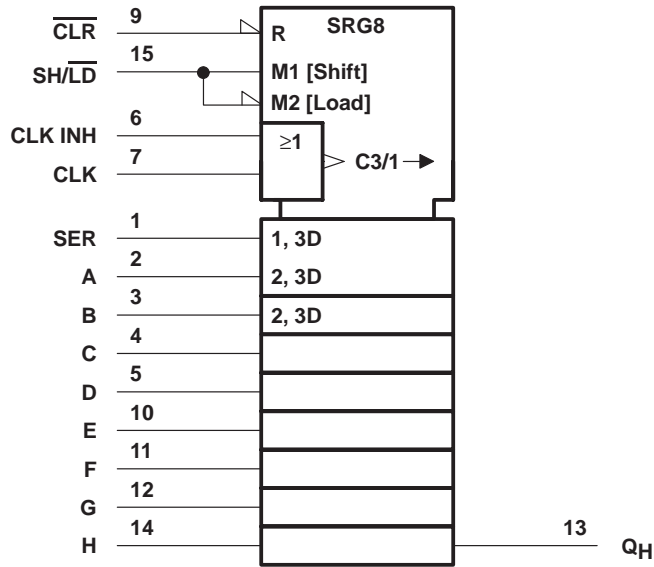
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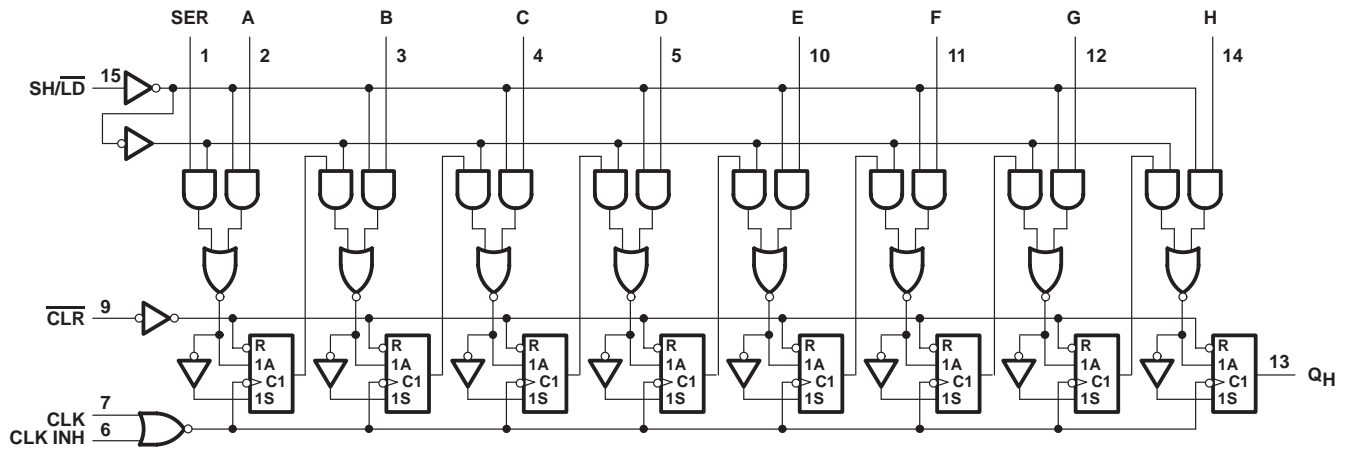
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logic symbol†

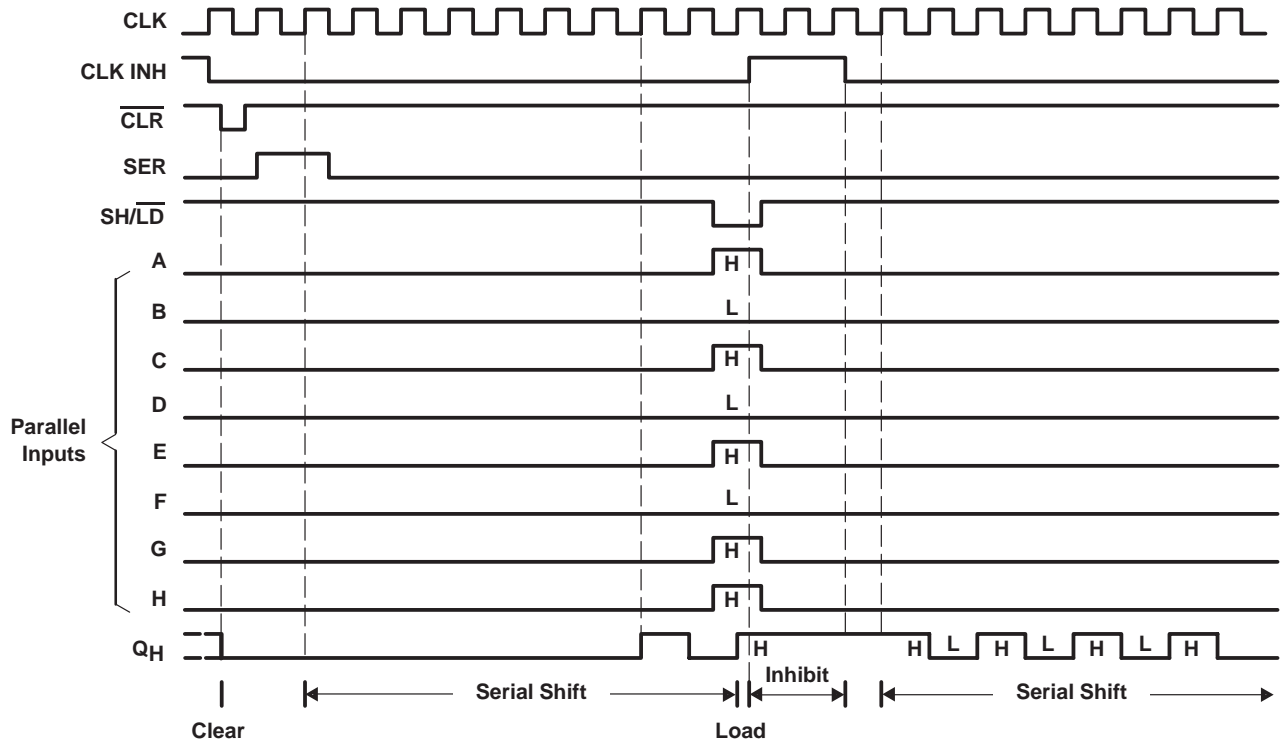


† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



typical clear, shift, load, inhibit, and shift sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I	-0.5 V to 7 V
Package thermal impedance, θ_{JA} (see Note 1): D package	73°C/W
DB package	82°C/W
N package	67°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{OH} High-level output current			-0.4	mA
I_{OL} Low-level output current			8	mA
T_A Operating free-air temperature	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.5	V
V_{OH}	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$,	$I_{OH} = -0.4\text{ mA}$	$V_{CC}-2$			V
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$		0.25	0.4	V
		$I_{OL} = 8\text{ mA}$		0.35	0.5	
I_I	$V_{CC} = 5.5\text{ V}$,	$V_I = 7\text{ V}$			0.1	mA
I_{IH}	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			20	μA
I_{IL}	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$			-0.1	mA
I_{O}^{\ddagger}	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.25\text{ V}$	-30		-112	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$,	See Note 2		14	24	mA

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 2: With 4.5 V applied to SER and all other inputs, except the clock, grounded, I_{CC} is measured after a clock transition from 0 V to 4.5 V.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
f_{clock}	Clock frequency		45	MHz
t_w	Pulse duration	$\overline{\text{CLR}}$ low	9	ns
		CLK high	10	
		CLK low	10	
t_{su}	Setup time before $\text{CLK}\uparrow$	$\text{SH}/\overline{\text{LD}}$	16	ns
		Data	7	
		$\overline{\text{CLR}}$ inactive	11	
t_h	Hold time, data after $\text{CLK}\uparrow$	3		ns

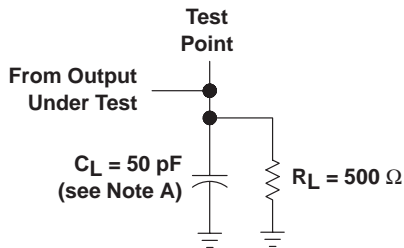
switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}			45			MHz
t_{PHL}	$\overline{\text{CLR}}$	Q_H	4	9	14	ns
t_{PLH}	CLK	Q_H	2	7	12	ns
t_{PHL}			2	9	13	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.



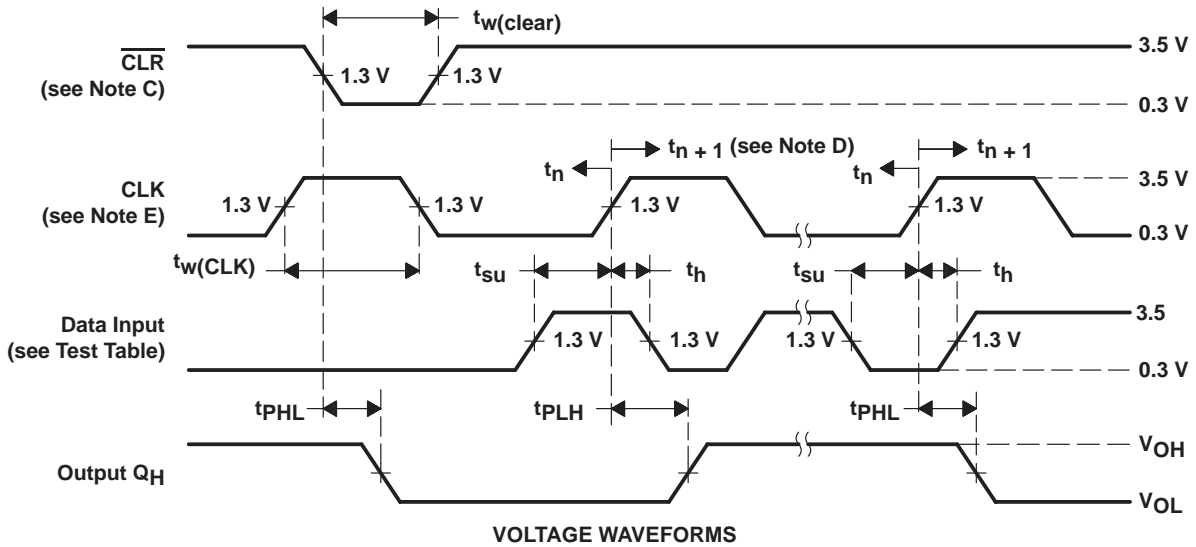
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SH/ $\overline{\text{LD}}$	OUTPUT TESTED (see Note B)
H	0 V	Q_H at t_{n+1}
Serial input	4.5 V	Q_H at t_{n+1}



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+8} with a functional test.
 - C. A clear pulse is applied prior to each test.
 - D. t_n = bit time before clocking transition, t_{n+1} = bit time after one clocking transition, and t_{n+8} = bit time after eight clocking transitions.
 - E. The clock pulse has the following characteristics: $t_{w(\text{clock})} \leq 20$ ns and $\text{PRR} = 1$ MHz. The clear pulse has the following characteristics: $t_{w(\text{clear})} \leq 20$ ns.
 - F. All pulse generators have the following characteristics: $Z_O \approx 50 \Omega$; $t_r = t_f = 2$ ns. Duty cycle = 50% when testing f_{max} .

Figure 1. Load Circuit and Voltage Waveforms

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