

# SN54ALS165, SN74ALS165 PARALLEL-LOAD 8-BIT REGISTERS

SDAS157B – JUNE 1982 – REVISED DECEMBER 1994

- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

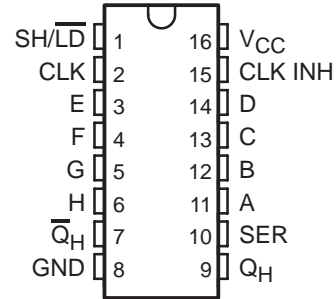
## description

The 'ALS165 are parallel-load 8-bit serial shift registers that, when clocked, shift the data toward serial ( $Q_H$  and  $\overline{Q}_H$ ) outputs. Parallel-in access to each stage is provided by eight individual direct data (A–H) inputs that are enabled by a low level at the shift/load ( $SH/\overline{LD}$ ) input. The 'ALS165 have a clock-inhibit function and complemented serial outputs.

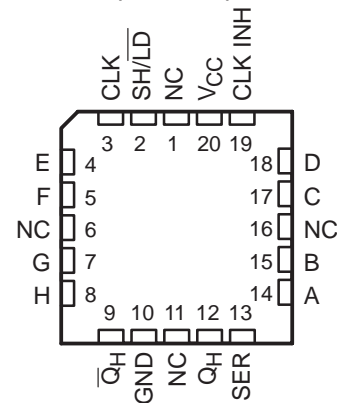
Clocking is accomplished by a low-to-high transition of the clock (CLK) input while  $SH/\overline{LD}$  is held high and the clock inhibit (CLK INH) input is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplishes clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when  $SH/\overline{LD}$  is held high. The parallel inputs to the register are enabled while  $SH/\overline{LD}$  is low independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

The SN54ALS165 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS165 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS165 . . . J PACKAGE  
SN74ALS165 . . . D OR N PACKAGE  
(TOP VIEW)



SN54ALS165 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

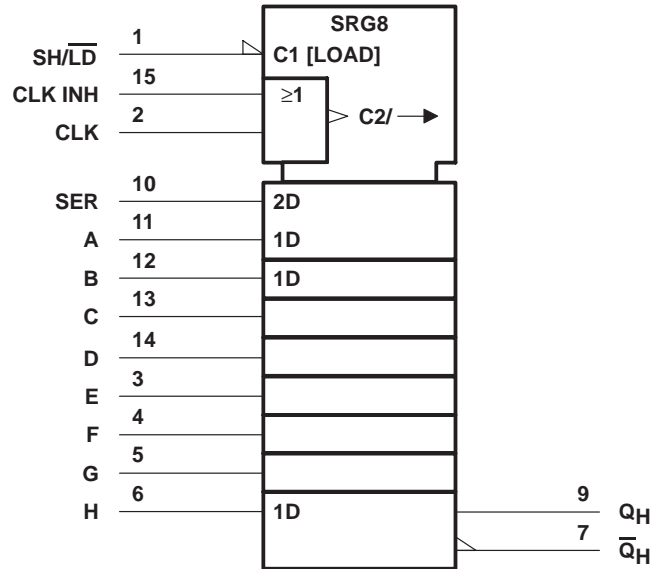
INPUTS			FUNCTION
$SH/\overline{LD}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	$\uparrow$	Shift <sup>†</sup>
H	$\uparrow$	L	Shift <sup>†</sup>

<sup>†</sup> Shift = content of each internal register shifts toward serial outputs. Data at SER is shifted into first register.

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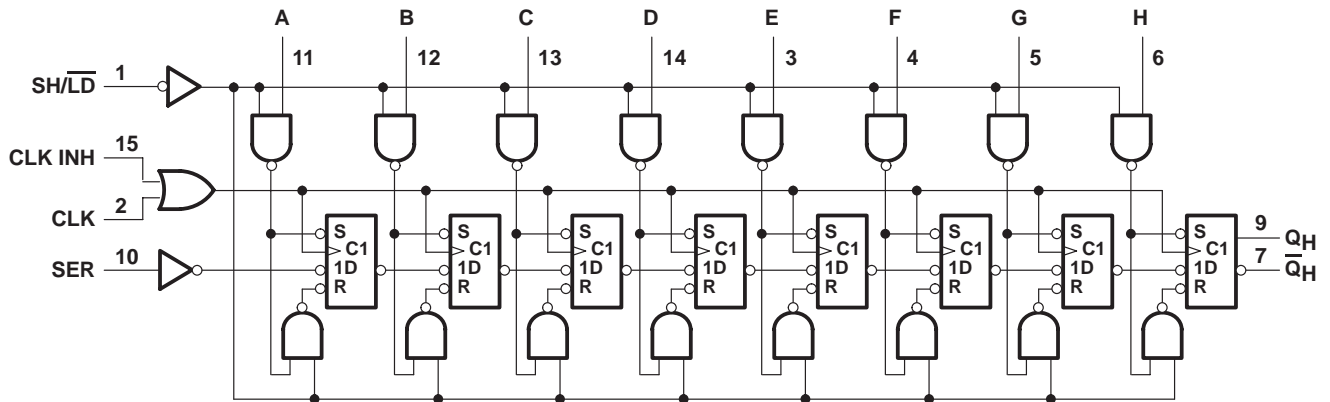
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## logic symbol†



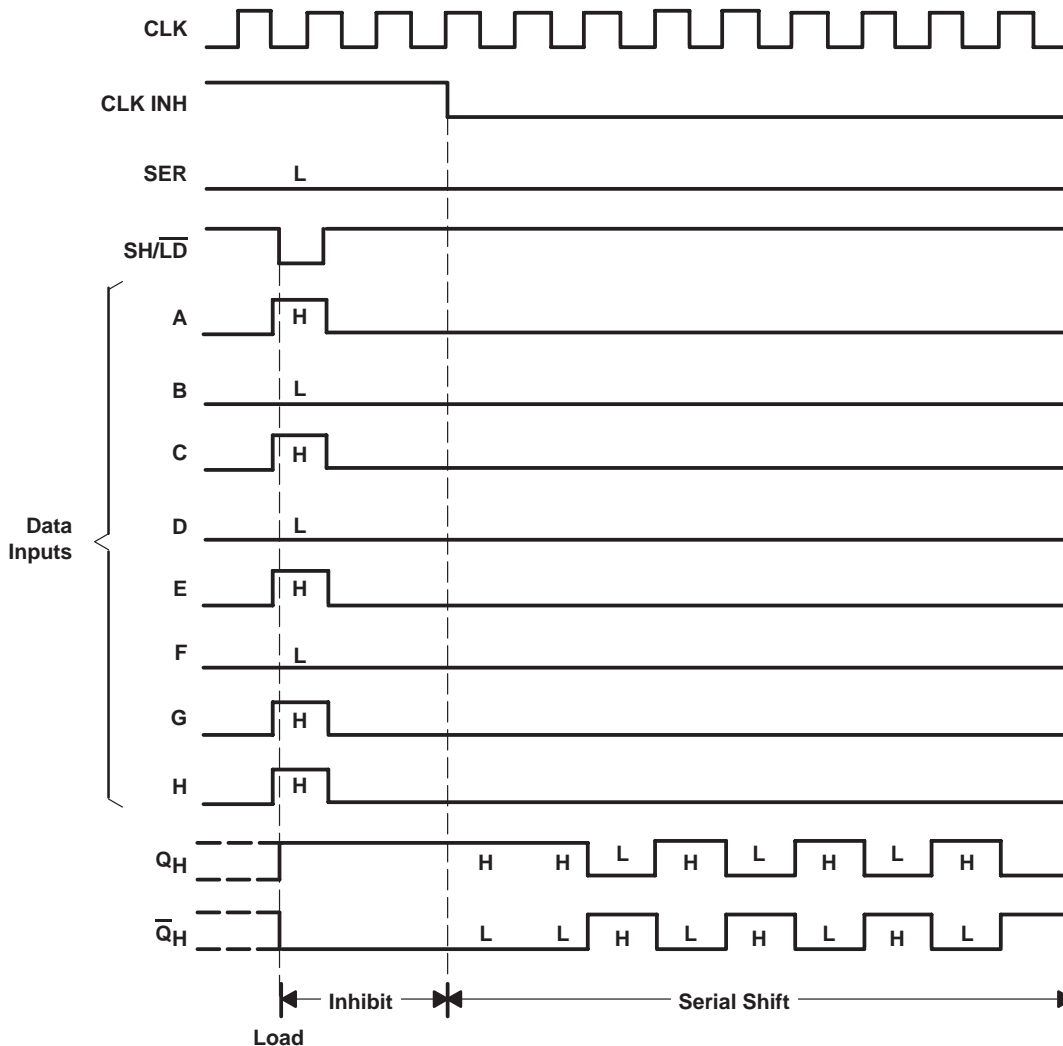
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)



Pin numbers shown are for the D, J, and N packages.

typical shift, load, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ .....	7 V
Operating free-air temperature range, $T_A$ : SN54ALS165 .....	-55°C to 125°C
SN74ALS165 .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# SN54ALS165, SN74ALS165 PARALLEL-LOAD 8-BIT REGISTERS

SDAS157B – JUNE 1982 – REVISED DECEMBER 1994

## recommended operating conditions

		SN54ALS165			SN74ALS165			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			-0.4			-0.4	mA
$I_{OL}$	Low-level output current			4			8	mA
$f_{clock}$	Clock frequency	0		35	0		45	MHz
$t_w(\text{CLK})$	Pulse duration, CLK (see Figure 1)	CLK high		14		11		ns
		CLK low		14		11		
$t_w(\text{load})$	Pulse duration, SH/LD low			15		12		ns
$t_{su1}$	Setup time, clock enable (see Figure 1)			15		11		ns
$t_{su2}$	Setup time, parallel input (see Figure 1)			11		10		ns
$t_{su3}$	Setup time, serial input (see Figure 2)			11		10		ns
$t_{su4}$	Setup time, shift (see Figure 2)			15		10		ns
$t_h$	Hold time at any input			4		4		ns
$T_A$	Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS165			SN74ALS165			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.5			-1.5	V
$V_{OH}$	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$	0.25	0.4	0.25	0.4	V	
		$I_{OL} = 8\text{ mA}$			0.35	0.5		
$I_I$	$V_{CC} = 5.5\text{ V}$ , $V_I = 7\text{ V}$			0.1		0.1	mA	
$I_{IH}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$			20		20	μA	
$I_{IL}$	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$			-0.1		-0.1	mA	
$I_{O†}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	-20		-112	-30		-112	mA
$I_{CC}$	$V_{CC} = 5.5\text{ V}$ , See Note 1		12	24		12	24	mA

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1: With the outputs open, CLK INH and CLK at 4.5 V, and a clock pulse applied to SH/LD,  $I_{CC}$  is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

# SN54ALS165, SN74ALS165 PARALLEL-LOAD 8-BIT REGISTERS

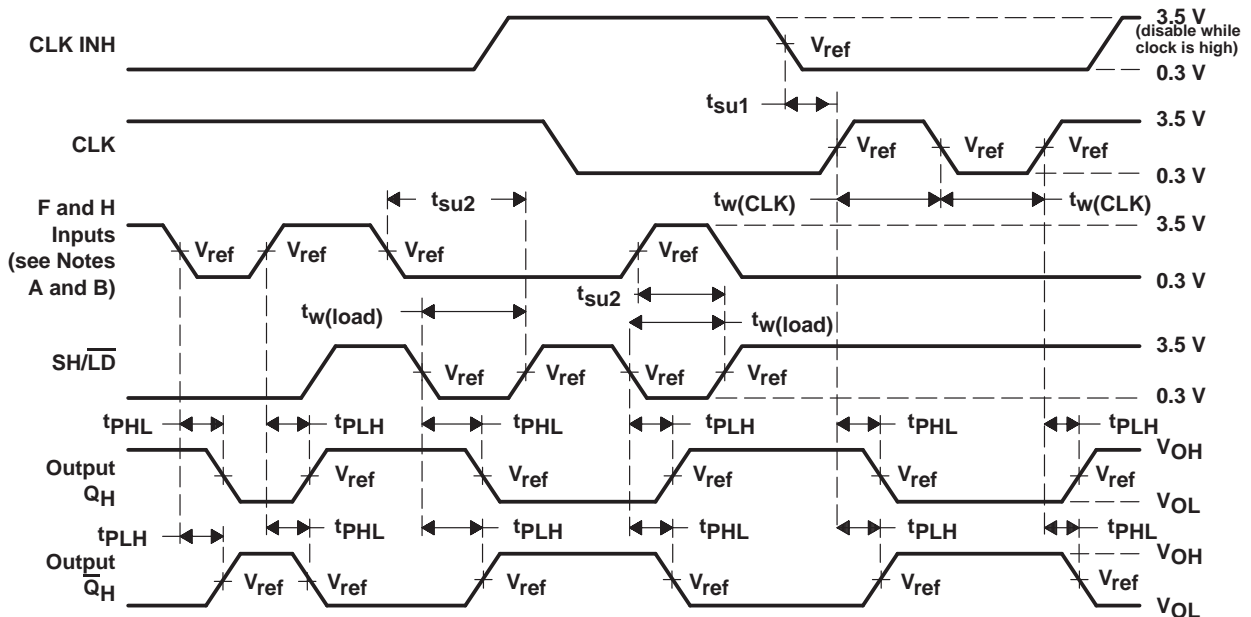
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switching characteristics (see Figures 1, 2, and 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54ALS165		SN74ALS165		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			35		45	MHz	
t <sub>PLH</sub>	SH/LD	Any	4	23	4	20	ns
t <sub>PHL</sub>			4	23	4	22	
t <sub>PLH</sub>	CLK	Any	3	14	3	13	ns
t <sub>PHL</sub>			3	15	3	14	
t <sub>PLH</sub>	H	Q <sub>H</sub>	3	14	3	13	ns
t <sub>PHL</sub>			3	18	3	16	
t <sub>PLH</sub>	H	Q̄ <sub>H</sub>	2	17	2	15	ns
t <sub>PHL</sub>			3	17	3	16	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The remaining six data inputs and SER are low.  
 B. Prior to test, high-level data is loaded into the H input.  
 C. The input pulse generators have the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t<sub>r</sub> = t<sub>f</sub> = 2 ns.  
 D. V<sub>ref</sub> = 1.3 V

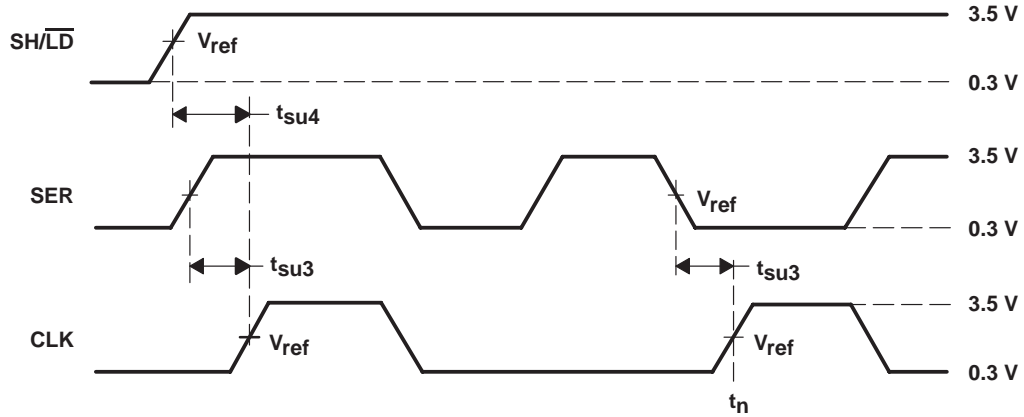
Figure 1. Voltage Waveforms



# SN54ALS165, SN74ALS165 PARALLEL-LOAD 8-BIT REGISTERS

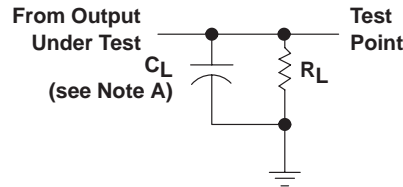
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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The eight data inputs and CLK INH are low. Results are monitored at  $Q_H$  at  $t_n + 7$ .  
 B. The input pulse generators have the following characteristics:  $PRR \leq 1$  MHz, duty cycle = 50%,  $t_r = t_f = 2$  ns.  
 C.  $V_{ref} = 1.3$  V

Figure 2. Voltage Waveforms



NOTE A:  $C_L$  includes probe and jig capacitance.

Figure 3. Load Circuit for Switching Tests

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ALS165D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS165DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS165DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS165DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS165DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS165DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS165N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS165N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74ALS165NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54ALS165J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54ALS165W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS165DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS165DR	SOIC	D	16	2500	333.2	345.9	28.6

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

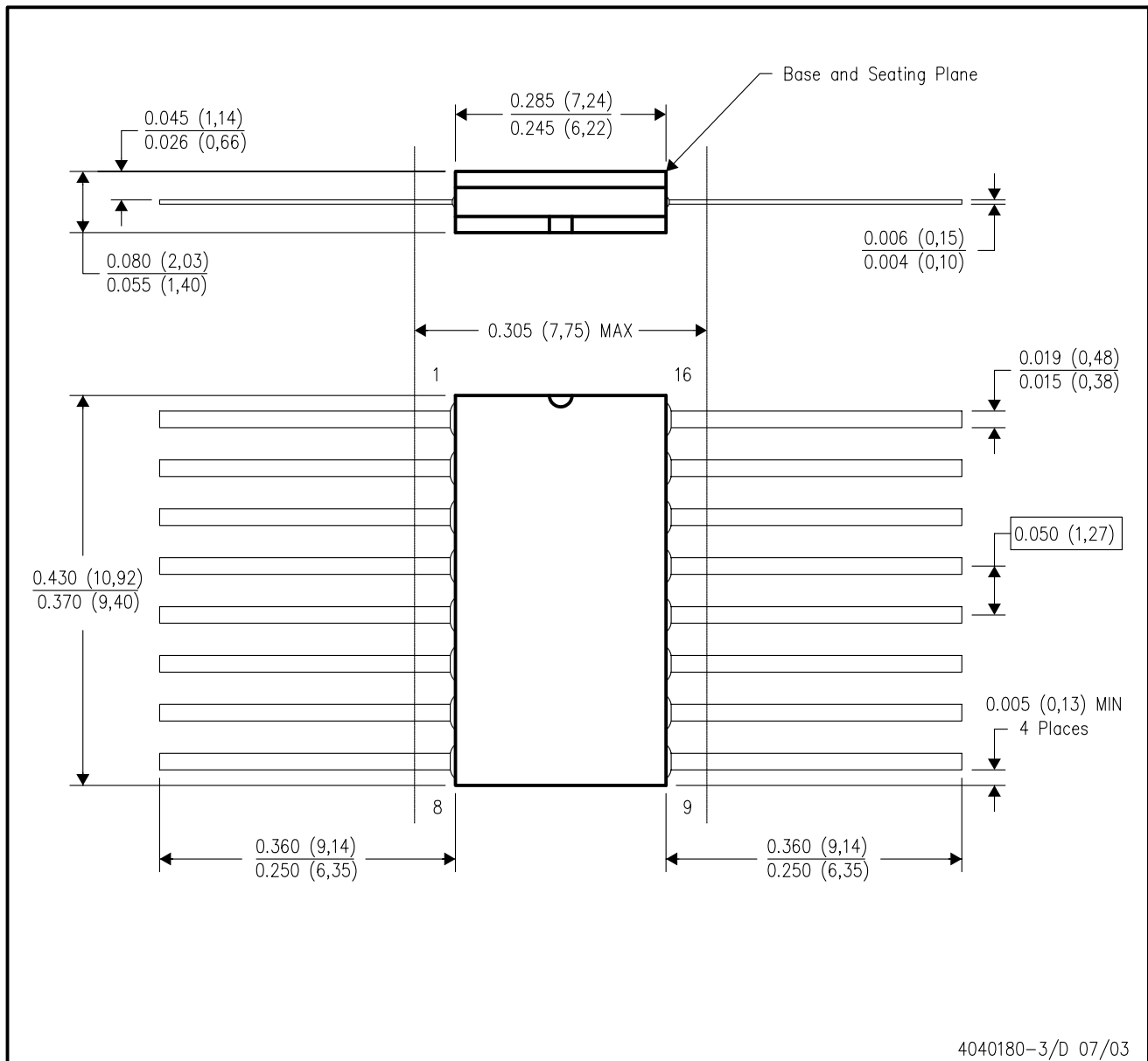


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

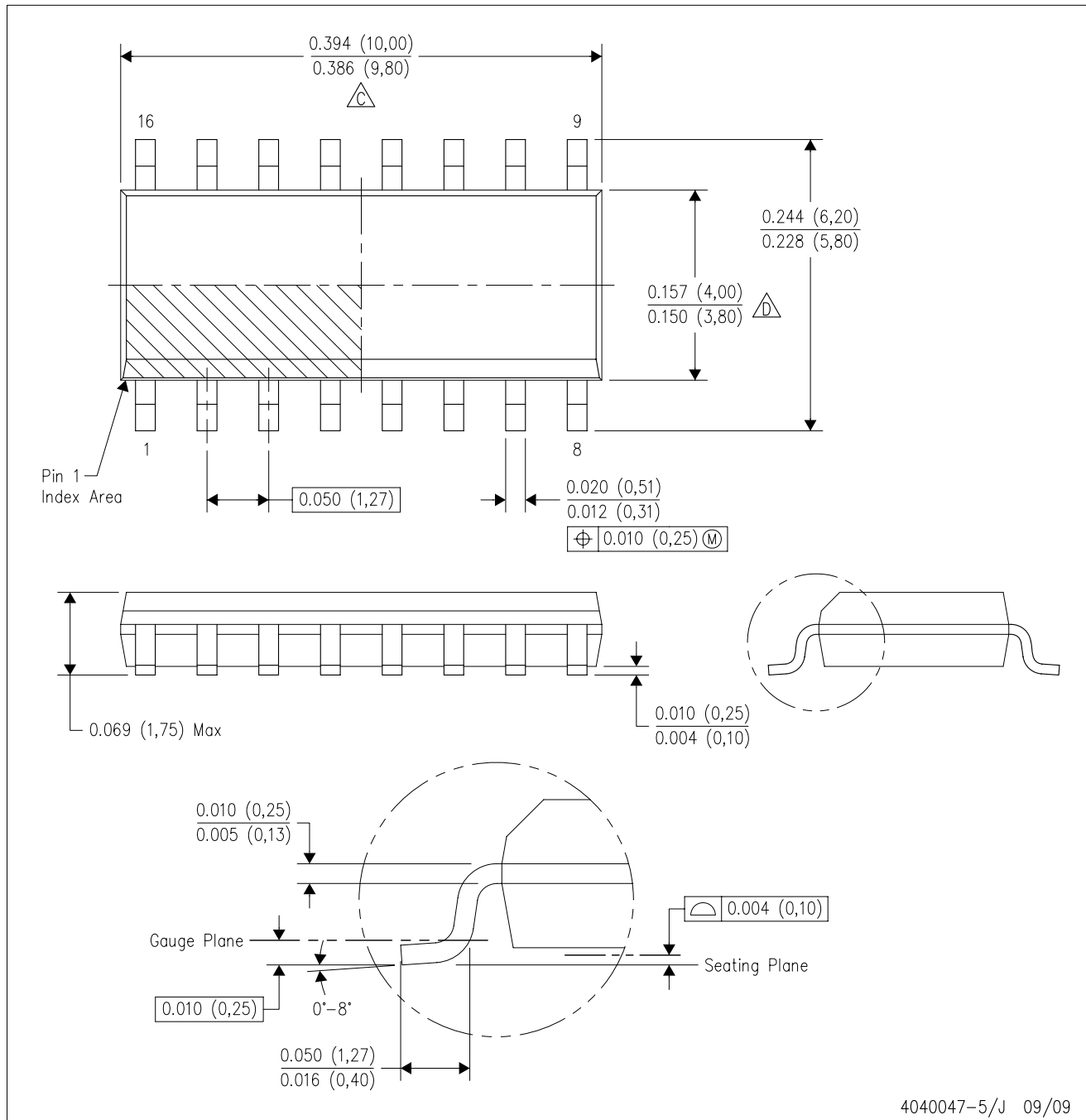
CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

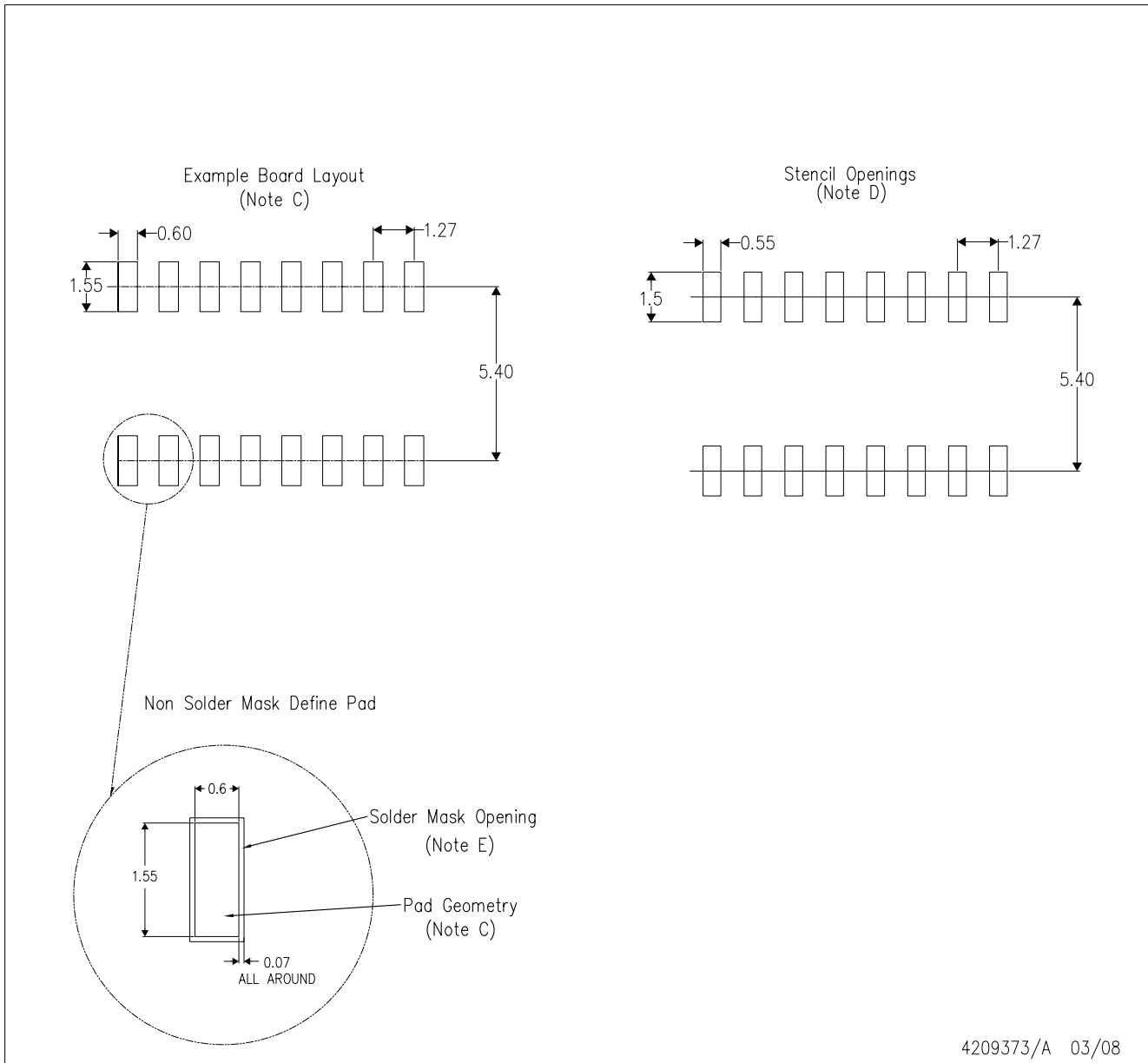
D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

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Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
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Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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