REVISIONS

| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
|---|---|---|---|
| A | Update to reflect latest changes in format and requirements. Editorial changes throughout. --les | 04-07-28 | Raymond Monnin |

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

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| REV | | | | | | | | | | | | | | | | | | | | |
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| REV STATUS | REV | A | A | A | A | A | A | A | A | A | | | | | |
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | | | | | |

| | | |
|---|---|---|
| PMIC N/A | PREPARED BY<br>Larry T. Gauder | **DEFENSE SUPPLY CENTER COLUMBUS**<br>**COLUMBUS, OHIO 43218-3990**<br>**http://www.dscc.dla.mil** |
| **STANDARD MICROCIRCUIT DRAWING**<br>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS<br>AND AGENCIES OF THE DEPARTMENT OF DEFENSE<br>AMSC N/A | CHECKED BY<br>Ray Monnin | |
| | APPROVED BY<br>Michael A. Frye | MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED LOW POWER SCHOTTKY, TTL, HEX NONINVERTING BUFFERS, MONOLITHIC SILICON |
| | DRAWING APPROVAL DATE<br>88-10-12 | |
| | REVISION LEVEL<br>**A** | SIZE<br>A |
| | | CAGE CODE<br>**67268** |
| | | **5962-88742** |
| | | SHEET 1 OF 9 |

## 1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

| 5962-88742 | 01 | C | A |
|---|---|---|---|
| Drawing number | Device type<br>(see 1.2.1) | Case outline<br>(see 1.2.2) | Lead finish<br>(see 1.2.3) |

1.2.1 Device type. The device type identifies the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 54ALS1035 | Hex noninverting buffers with open collector outputs |

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| C | GDIP1-T14 or CDIP2-T14 | 14 | dual-in-line |
| D | GDFP1-F14 or CDFP2-F14 | 14 | flat |
| 2 | CQCC1-N20 | 20 | square chip carrier |

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

| | |
|---|---|
| Supply voltage range ..................................................... | -0.5 V minimum dc to +7.0 V dc maximum |
| Input voltage range ........................................................ | -1.5 V dc at –18 mA to +7.0 V dc |
| Storage temperature range ........................................... | -65°C to +150°C |
| Maximum power dissipation ($P_D$) .................................. | 77 mW 1/ |
| Lead temperature (soldering, 10 seconds) .................... | +300°C |
| Junction temperature ($T_J$) ............................................... | +175°C |
| Thermal resistance, junction-to-case ($\theta_{JC}$) .................... | See MIL-STD-1835 |

1.4 Recommended operating conditions.

| | |
|---|---|
| Supply voltage range ($V_{CC}$) ........................................................ | +4.5 V dc minimum to +5.5 V dc maximum |
| Minimum high level input voltage ($V_{IH}$) .................................... | 2.0 V dc |
| Maximum low level input voltage ($V_{IL}$): | |
| $T_C$ = +125°C ......................................................................... | 0.7 V dc |
| $T_C$ = -55°C .......................................................................... | 0.8 V dc |
| $T_C$ = +25°C .......................................................................... | 0.7 V dc |
| Maximum high level output voltage ($V_{OH}$) ................................ | 5.5 V dc |
| Maximum low level output current ($I_{OL}$) .................................. | 12 mA |
| Case operating temperature range ($T_C$) .................................. | -55°C to +125°C |

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1/ Maximum power dissipation is defined as $V_{CC}$ X $I_{CC}$, and must withstand the added $P_D$ due to short circuit test e.g., $I_{OS}$.

## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 -- Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 -- List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions<br>$-55°C \leq T_C \leq +125°C$ 1/<br>unless otherwise specified | Group A subgroups | Device type | Limits |  | Unit |
|---|---|---|---|---|---|---|---|
|  |  |  |  |  | Min | Max |  |
| Low level output voltage | $V_{OL}$ | $V_{CC}$ = 4.5 V,<br>$V_{IH}$ = 2.0 V,<br>$I_{OL}$ = 12 mA<br>2/<br>$V_{IL}$ at:<br>+125°C = 0.7 V<br>-55°C = 0.8 V<br>+25°C = 0.7 V | 1, 2, 3 | All |  | 0.4 | V |
| High level output current | $I_{OH}$ | $V_{CC}$ = 4.5 V, $V_{OH}$ = 5.5 V | 1, 2, 3 | All |  | 0.1 | mA |
| Input clamp voltage | $V_{IC}$ | $V_{CC}$ = 4.5 V, $I_{IN}$ = -18 mA | 1, 2, 3 | All |  | -1.5 | V |
| Low level input current | $I_{IL}$ | $V_{CC}$ = 5.5 V, $V_{IN}$ = 0.4 V<br>Unused inputs ≥ 4.5 V | 1, 2, 3 | All |  | -0.1 | mA |
| High level input current | $I_{IH1}$ | $V_{CC}$ = 5.5 V, $V_{IN}$ = 2.7 V<br>Unused inputs = 0.0 V | 1, 2, 3 | All |  | 20 | μA |
|  | $I_{IH2}$ | $V_{CC}$ = 5.5 V, $V_{IN}$ = 7.0 V<br>Unused inputs = 0.0 V | 1, 2, 3 | All |  | 0.1 | mA |
| Supply current | $I_{CCH}$ | $V_{CC}$ = 5.5 V, $V_{IN}$ = 4.5 V | 1, 2, 3 | All |  | 6 | mA |
|  | $I_{CCL}$ | $V_{CC}$ = 5.5 V, $V_{IN}$ = 0.0 V | 1, 2, 3 | All |  | 14 | mA |
| Functional tests |  | See 4.3.1c 3/ | 7, 8 | All |  |  |  |
| Propagation delay time, from A to Y | $t_{PLH}$ | $V_{CC}$ = 4.5 to 5.5 V,<br>$C_L$ = 50 pF,<br>$R_L$ = 680Ω,<br>See figure 3 4/ | 9, 10, 11 | All | 5 | 35 | ns |
|  | $t_{PHL}$ |  | 9, 10, 11 | All | 2 | 14 | ns |

1/ Unused inputs that do not directly control the pin under test must be ≥ 2.5 V or ≤ 0.4 V. No unused inputs shall exceed 5.5 V or go less than 0.0 V. No inputs shall be floated.

2 All outputs must be tested. In the case where only one input at $V_{IL}$ maximum or $V_{IH}$ minimum produces the proper output state, the test must be performed with each input being selected as the $V_{IL}$ maximum or $V_{IH}$ minimum input.

3/ Functional tests shall be conducted at input test conditions of $GND \leq V_{IL} \leq V_{OL}$ and $V_{OH} \leq V_{IH} \leq V_{CC}$.

4/ Propagation delay limits are based on single output switching. Unused inputs = 3.5 V or ≤ 0.3 V.

| Case outlines | C and D | 2 |
|---|---|---|
| Terminal number | Terminal symbol | |
| 1 | 1A | NC |
| 2 | 1Y | 1A |
| 3 | 2A | 1Y |
| 4 | 2Y | 2A |
| 5 | 3A | NC |
| 6 | 3Y | 2Y |
| 7 | GND | NC |
| 8 | 4Y | 3A |
| 9 | 4A | 3Y |
| 10 | 5Y | GND |
| 11 | 5A | NC |
| 12 | 6Y | 4Y |
| 13 | 6A | 4A |
| 14 | $V_{CC}$ | 5Y |
| 15 | - - - | NC |
| 16 | - - - | 5A |
| 17 | - - - | NC |
| 18 | - - - | 6Y |
| 19 | - - - | 6A |
| 20 | - - - | $V_{CC}$ |

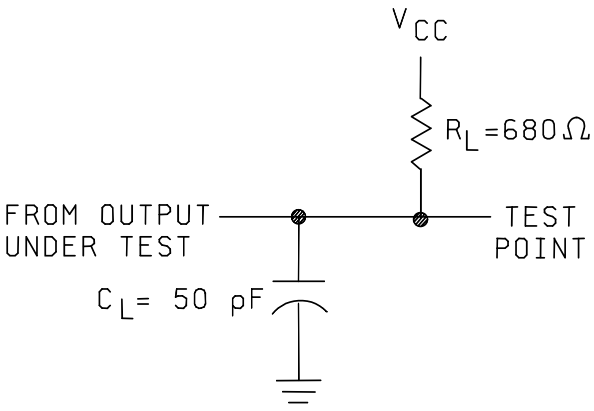
NC = No connection

FIGURE 1. Terminal connections.

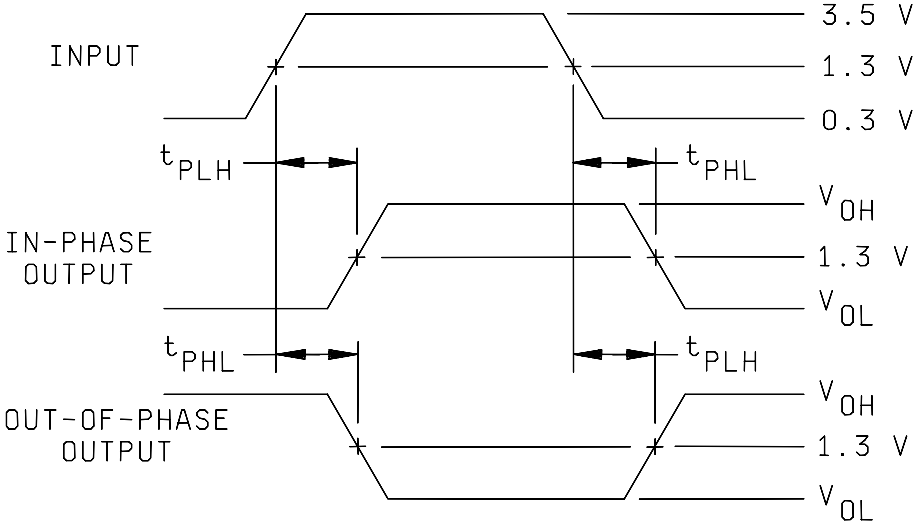
| Input A | Output Y |
|---|---|
| H | H |
| L | L |

H = High level voltage
L = Low level voltage

FIGURE 2. Truth table.



TEST CIRCUIT



PROPAGATION DELAY TIMES

NOTES:

1. $C_L$ includes probe and jig capacitance.
2. All input pulses have the following characteristics: PRR ≤ 10 MHz, duty cycle = 50%, $t_r$ = $t_f$ = 3 ns ±1 ns.
3. The outputs are measured one at a time with one input transition per measurement.

FIGURE 3. Test circuit and switching waveforms.

| | | | |
|---|---|---|---|
| **STANDARD**<br>**MICROCIRCUIT DRAWING**<br>DEFENSE SUPPLY CENTER COLUMBUS<br>COLUMBUS, OHIO 43218-3990 | SIZE<br>**A** | | **5962-88742** |
| | | REVISION LEVEL<br>**A** | SHEET<br>**7** |

## 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

  (1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

  (2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) |
|---|---|
| Interim electrical parameters (method 5004) | - - - |
| Final electrical test parameters (method 5004) | 1*, 2, 3, 7, 8, 9 10, 11 |
| Group A test requirements (method 5005) | 1, 2, 3, 7, 8, 9, 10, 11 |
| Groups C and D end-point electrical parameters (method 5005) | 1, 2, 3 |

* PDA applies to subgroups 1 and 7.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

# STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 04-07-28

Approved sources of supply for SMD 5962-88742 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ | Reference military specification PIN |
|---|---|---|---|
| 5962-8874201CA | 01295 | SNJ54ALS1035J | M38510/38401CA |
| 5962-8874201DA | 01295 | SNJ54ALS1035W | M38510/38401DA |
| 5962-88742012A | 01295 | SNJ54ALS1035FK | M38510/384012A |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 01295 | Texas Instruments, Inc.<br>Semiconductor Group<br>8505 Forest Ln.<br>PO Box 660199<br>Dallas, Tx 75243<br>POC U.S. Highway 75 South<br>P.O. Box 84, M/S 853<br>Sherman, TX 75090-9493 |