

SN54AHCT240, SN74AHCT240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS252K – OCTOBER 1995 – REVISED JULY 2003

- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17

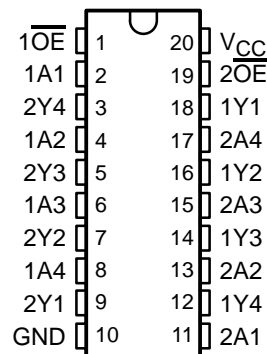
description/ordering information

These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

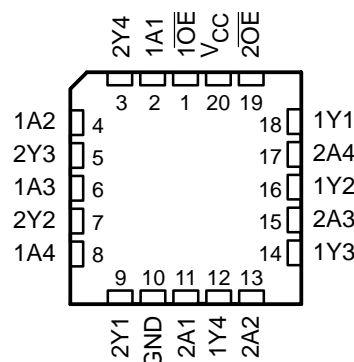
The 'AHCT240 devices are organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54AHCT240 . . . J OR W PACKAGE
SN74AHCT240 . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHCT240 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74AHCT240N	SN74AHCT240N
	SOIC – DW	Tube	SN74AHCT240DW	AHCT240
		Tape and reel	SN74AHCT240DWR	
	SOP – NS	Tape and reel	SN74AHCT240NSR	AHCT240
	SSOP – DB	Tape and reel	SN74AHCT240DBR	HB240
	TSSOP – PW	Tube	SN74AHCT240PW	HB240
		Tape and reel	SN74AHCT240PWR	
TVSOP – DGV	Tape and reel	SN74AHCT240DGV	HB240	
-55°C to 125°C	CDIP – J	Tube	SNJ54AHCT240J	SNJ54AHCT240J
	CFP – W	Tube	SNJ54AHCT240W	SNJ54AHCT240W
	LCCC – FK	Tube	SNJ54AHCT240FK	SNJ54AHCT240FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

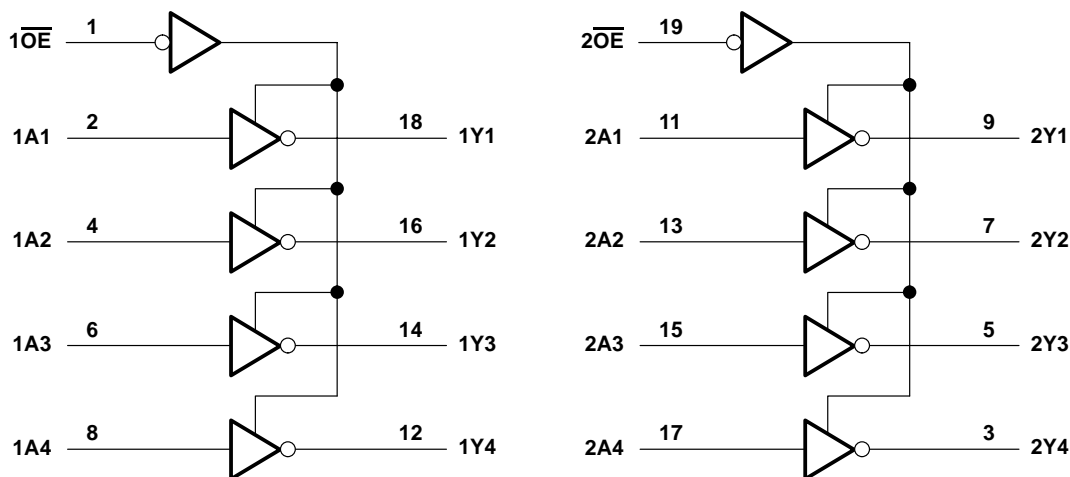
SN54AHCT240, SN74AHCT240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS252K – OCTOBER 1995 – REVISED JULY 2003

FUNCTION TABLE
(each 4-bit buffer/driver)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	L
L	L	H
H	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 75 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C/W
DGV package	92°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54AHCT240, SN74AHCT240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS252K – OCTOBER 1995 – REVISED JULY 2003

recommended operating conditions (see Note 3)

		SN54AHCT240		SN74AHCT240		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-8		-8	mA
I _{OL}	Low-level output current		8		8	mA
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT240		SN74AHCT240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I _{OH} = -8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1		0.1		V	
	I _{OL} = 8 mA				0.36		0.44			0.44
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25		±2.5		μA	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*		μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40		μA	
ΔI _{CC} †	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5		mA	
C _i	V _I = V _{CC} or GND	5 V		2.5	10				pF	
C _o	V _O = V _{CC} or GND	5 V		3					pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

SN54AHCT240, SN74AHCT240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS252K – OCTOBER 1995 – REVISED JULY 2003

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHCT240		SN74AHCT240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	5.4*	7.4*		1*	8.5*	1	8.5	ns
t_{PHL}				5.4*	7.4*	1*	8.5*	1	8.5		
t_{PZH}	\overline{OE}	Y	$C_L = 15\text{ pF}$	7.7*	10.4*		1*	12*	1	12	ns
t_{PZL}				7.7*	10.4*	1*	12*	1	12		
t_{PHZ}	\overline{OE}	Y	$C_L = 15\text{ pF}$	8.3*	10.4*		1*	12*	1	12	ns
t_{PLZ}				8.3*	10.4*	1*	12*	1	12		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.9	8.4		1	9.5	1	9.5	ns
t_{PHL}				5.9	8.4	1	9.5	1	9.5		
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	8.2	11.4		1	13	1	13	ns
t_{PZL}				8.2	11.4	1	13	1	13		
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	8.8	11.4		1	13	1	13	ns
t_{PLZ}				8.8	11.4	1	13	1	13		
$t_{sk(o)}$			$C_L = 50\text{ pF}$			1**				1	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	SN74AHCT240			UNIT
	MIN	TYP	MAX	
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		4.1		V
$V_{IH(D)}$ High-level dynamic input voltage	2			V
$V_{IL(D)}$ Low-level dynamic input voltage			0.8	V

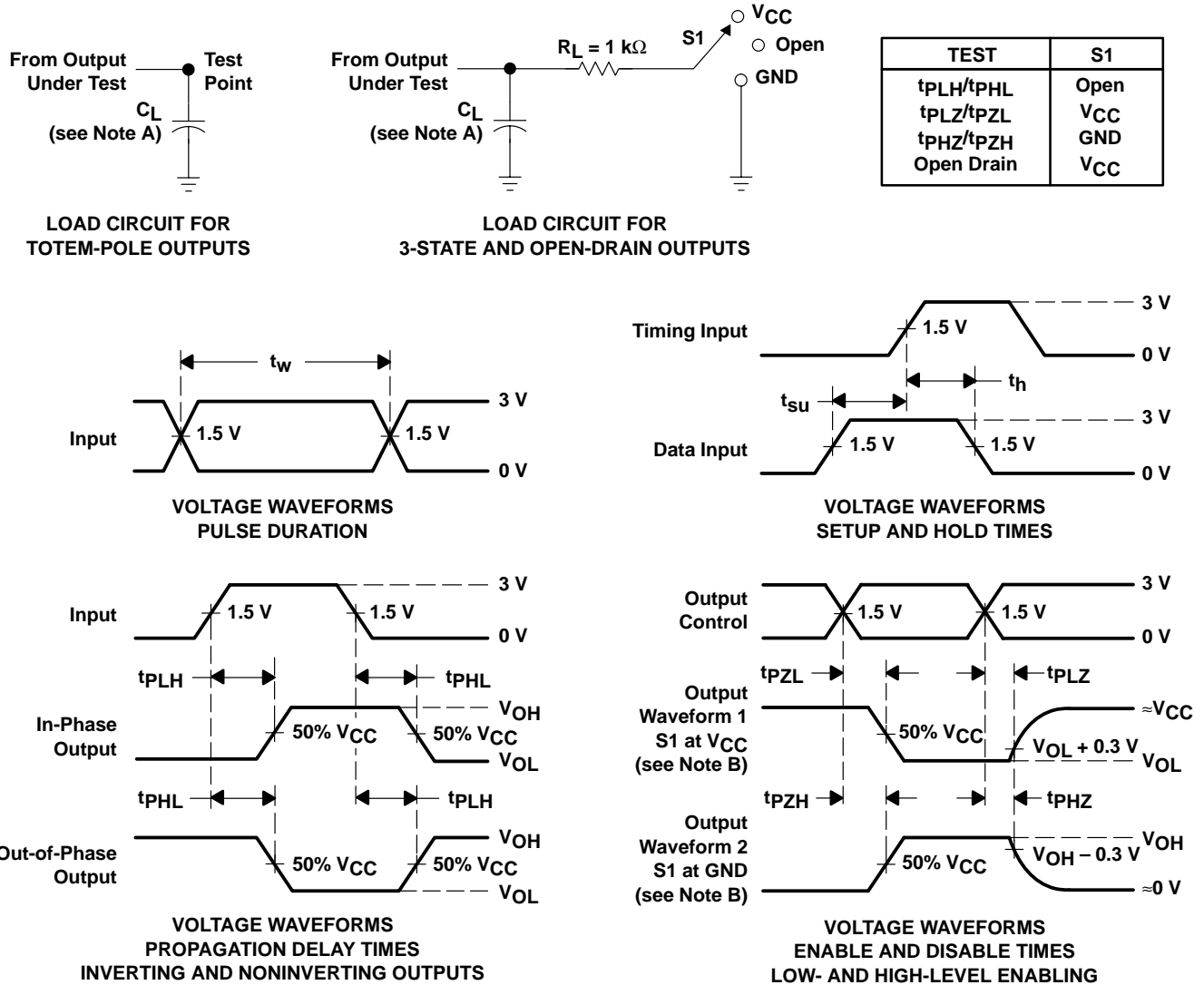
NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	10	pF



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms