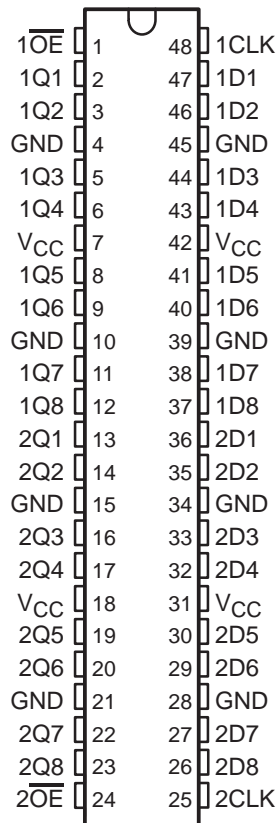


SN54AHCT16374, SN74AHCT16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS3371 – MARCH 1996 – REVISED FEBRUARY 2000

- **Members of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Inputs Are TTL-Voltage Compatible**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54AHCT16374 . . . WD PACKAGE
SN74AHCT16374 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The 'AHCT16374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

\overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54AHCT16374 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AHCT16374 is characterized for operation from -40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated

SN54AHCT16374, SN74AHCT16374

16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS

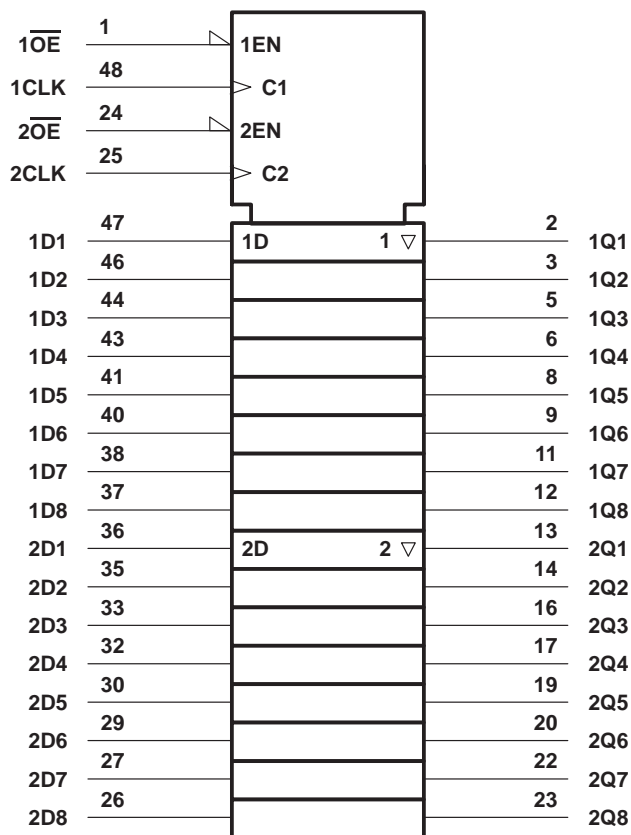
WITH 3-STATE OUTPUTS

SCLS3371 – MARCH 1996 – REVISED FEBRUARY 2000

FUNCTION TABLE
(each 8-bit flip-flop)

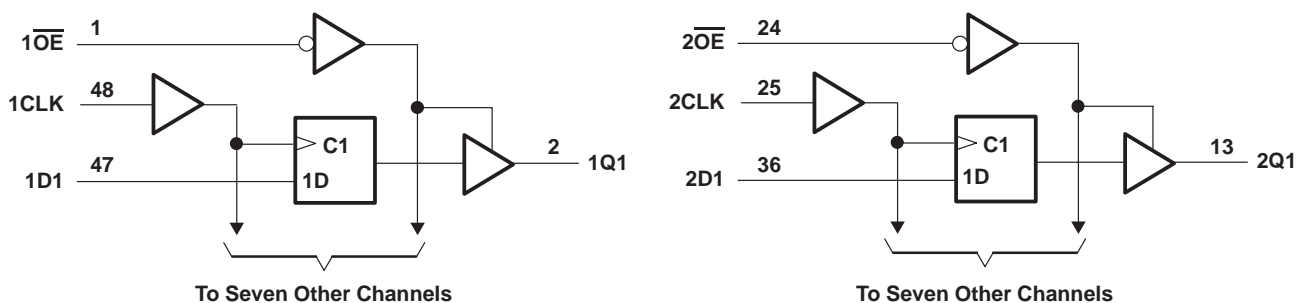
| INPUTS | | | OUTPUT |
|-----------------|--------|---|--------|
| \overline{OE} | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q_0 |
| H | X | X | Z |

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54AHCT16374, SN74AHCT16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS3371 – MARCH 1996 – REVISED FEBRUARY 2000

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | –0.5 V to 7 V |
| Output voltage range, V_O (see Note 1) | –0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | –20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±25 mA |
| Continuous current through each V_{CC} or GND | ±75 mA |
| Package thermal impedance, θ_{JA} (see Note 2): DGG package | 70°C/W |
| DGV package | 58°C/W |
| DL package | 63°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

| | SN54AHCT16374 | | SN74AHCT16374 | | UNIT |
|--|---------------|----------|---------------|----------|------|
| | MIN | MAX | MIN | MAX | |
| V_{CC} Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} High-level input voltage | 2 | | 2 | | V |
| V_{IL} Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| V_O Output voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} High-level output current | | –8 | | –8 | mA |
| I_{OL} Low-level output current | | 8 | | 8 | mA |
| $\Delta t/\Delta v$ Input transition rise or fall rate | | 20 | | 20 | ns/V |
| T_A Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54AHCT16374, SN74AHCT16374
16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

SCLS3371 – MARCH 1996 – REVISED FEBRUARY 2000

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54AHCT16374 | | SN74AHCT16374 | | UNIT |
|--------------------|---|-----------------|-----------------------|-----|-------|---------------|------|---------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = -50 μA | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | V | |
| | I _{OH} = -8 mA | | 3.94 | | | 3.8 | | 3.8 | | |
| V _{OL} | I _{OL} = 50 μA | 4.5 V | | | 0.1 | | | 0.1 | V | |
| | I _{OL} = 8 mA | | | | 0.36 | | 0.44 | 0.44 | | |
| I _I | V _I = V _{CC} or GND | 0 V to 5.5 V | | | ±0.1 | | ±1* | ±1 | μA | |
| I _{OZ} | V _O = V _{CC} or GND, V _I = V _{IH} or V _{IL} | 5.5 V | | | ±0.25 | | ±2.5 | ±2.5 | μA | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 4 | | 40 | 40 | μA | |
| ΔI _{CC} † | One input at 3.4 V, Other inputs at V _{CC} or GND | 5.5 V | | | 1.35 | | 1.5 | 1.5 | mA | |
| C _i | V _I = V _{CC} or GND | 5 V | | 2.5 | 10 | | | 10 | pF | |
| C _o | V _O = V _{CC} or GND | 5 V | | 3.5 | | | | | pF | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | T _A = 25°C | | SN54AHCT16374 | | SN74AHCT16374 | | UNIT |
|-----------------|---------------------------------|-----------------------|-----|---------------|-----|---------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _w | Pulse duration, CLK high or low | 6.5 | | 6.5 | | 6.5 | | ns |
| t _{su} | Setup time, data before CLK↑ | 2.5 | | 2.5 | | 2.5 | | ns |
| t _h | Hold time, data after CLK↑ | 2.5 | | 2.5 | | 2.5 | | ns |

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54AHCT16374, SN74AHCT16374
16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

SCLS3371 – MARCH 1996 – REVISED FEBRUARY 2000

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | SN54AHCT16374 | | SN74AHCT16374 | | UNIT |
|--------------------|------------------------|-------------|----------------------|--------------------------|-------|-----|---------------|-------|---------------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | $C_L = 15\text{ pF}$ | 90* | 140* | | 80* | | 110 | | MHz |
| | | | $C_L = 50\text{ pF}$ | 85 | 130 | | 75 | | 75 | | |
| t_{PLH} | CLK | Q | $C_L = 15\text{ pF}$ | 6.5* | 9.4* | | 1* | 10.5* | 1 | 10.5 | ns |
| t_{PHL} | | | | 6.5* | 9.4* | | 1* | 10.5* | 1 | 10.5 | |
| t_{PZH} | $\overline{\text{OE}}$ | Q | $C_L = 15\text{ pF}$ | 6.5* | 9.5* | | 1* | 10.5* | 1 | 10.5 | ns |
| t_{PZL} | | | | 6.5* | 9.5* | | 1* | 10.5* | 1 | 10.5 | |
| t_{PHZ} | $\overline{\text{OE}}$ | Q | $C_L = 15\text{ pF}$ | 6.2* | 10.2* | | 1* | 11* | 1 | 11 | ns |
| t_{PLZ} | | | | 6.2* | 10.2* | | 1* | 11* | 1 | 11 | |
| t_{PLH} | CLK | Q | $C_L = 50\text{ pF}$ | 7.3 | 10.4 | | 1 | 11.5 | 1 | 11.5 | ns |
| t_{PHL} | | | | 7.1 | 10.4 | | 1 | 11.5 | 1 | 11.5 | |
| t_{PZH} | $\overline{\text{OE}}$ | Q | $C_L = 50\text{ pF}$ | 6.2 | 10.5 | | 1 | 11.5 | 1 | 11.5 | ns |
| t_{PZL} | | | | 5.1 | 10.5 | | 1 | 11.5 | 1 | 11.5 | |
| t_{PHZ} | $\overline{\text{OE}}$ | Q | $C_L = 50\text{ pF}$ | 7.1 | 11.2 | | 1 | 12 | 1 | 12 | ns |
| t_{PLZ} | | | | 7.9 | 11.2 | | 1 | 12 | 1 | 12 | |
| $t_{\text{sk(o)}}$ | | | $C_L = 50\text{ pF}$ | | | 1** | | | | 1 | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

| PARAMETER | | SN74AHCT16374 | | | UNIT |
|--------------------|---|---------------|------|------|------|
| | | MIN | TYP | MAX | |
| $V_{\text{OL(P)}}$ | Quiet output, maximum dynamic V_{OL} | | 0.36 | 0.8 | V |
| $V_{\text{OL(V)}}$ | Quiet output, minimum dynamic V_{OL} | | -0.1 | -0.8 | V |
| $V_{\text{OH(V)}}$ | Quiet output, minimum dynamic V_{OH} | | 4.7 | | V |
| $V_{\text{IH(D)}}$ | High-level dynamic input voltage | | 2 | | V |
| $V_{\text{IL(D)}}$ | Low-level dynamic input voltage | | | 0.8 | V |

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------------|-------------------------------|-----------------------------|-----|------|
| C_{pd} | Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 27 | pF |

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

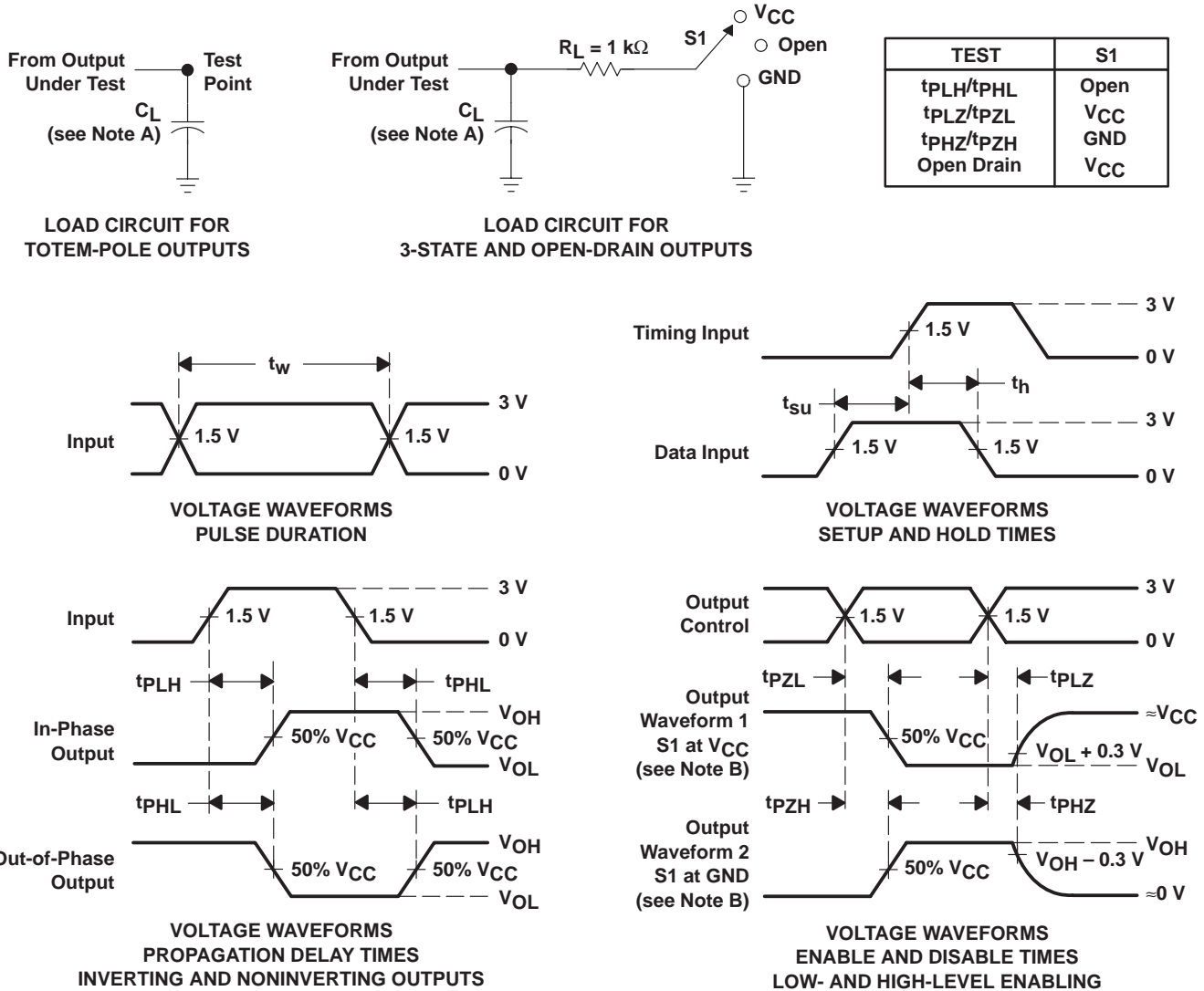


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54AHCT16374, SN74AHCT16374 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCLS3371 – MARCH 1996 – REVISED FEBRUARY 2000

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.