

SNx4AHCT126 Quadruple Bus Buffer Gates With 3-State Outputs

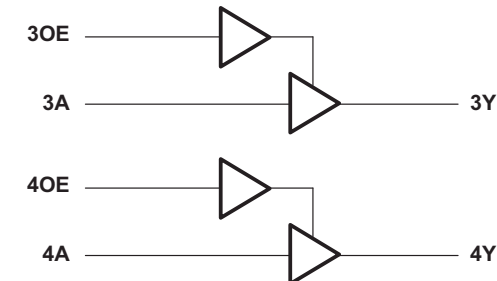
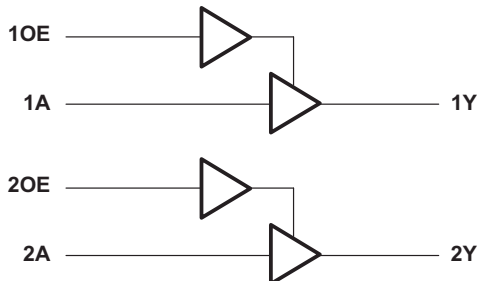
1 Features

- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Servers
- PCs and Notebooks
- Network Switches
- Wearable Health and Fitness Devices
- Telecom Infrastructures
- Electronic Points of Sale

4 Simplified Schematic



3 Description

The SNxAHCT126 devices are quadruple-bus buffer gates featuring independent line drivers with 3-state outputs.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4AHCT126	SOIC (14)	8.65 mm × 3.91 mm
	SSOP (14)	6.20 mm × 5.30 mm
	TVSOP (14)	3.60 mm × 4.40 mm
	PDIP (14)	3.90 mm × 6.35 mm
	SOP (14)	10.30 mm × 5.30 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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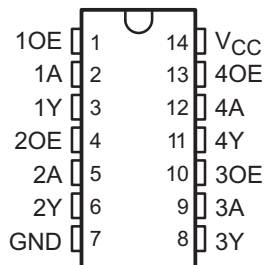
1 Features 1 2 Applications 1 3 Description 1 4 Simplified Schematic 1 5 Revision History 2 6 Pin Configuration and Functions 3 7 Specifications 4 7.1 Absolute Maximum Ratings 4 7.2 Handling Ratings 4 7.3 Recommended Operating Conditions 4 7.4 Thermal Information 5 7.5 Electrical Characteristics 5 7.6 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ 6 7.7 Noise Characteristics 6 7.8 Operating Characteristics 6 7.9 Typical Characteristics 6 8 Parameter Measurement Information 7 9 Detailed Description 8	9.1 Overview 8 9.2 Functional Block Diagram 8 9.3 Feature Description 8 9.4 Device Functional Modes 8 10 Application and Implementation 9 10.1 Application Information 9 10.2 Typical Application 9 11 Power Supply Recommendations 10 12 Layout 10 12.1 Layout Guidelines 10 12.2 Layout Example 10 13 Device and Documentation Support 11 13.1 Related Links 11 13.2 Trademarks 11 13.3 Electrostatic Discharge Caution 11 13.4 Glossary 11 14 Mechanical, Packaging, and Orderable Information 11
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5 Revision History

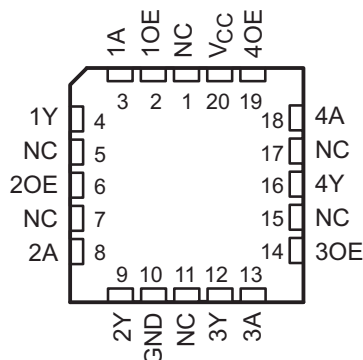
Changes from Revision O (July 2003) to Revision P	Page
• Updated document to new TI data sheet standards.	1
• Deleted Ordering Information Table.	1
• Added Military Disclaimer to Features list.	1
• Added Applications.	1
• Added Pin Functions table.	3
• Added Handling Ratings table.	4
• Changed MAX operating temperature to 125°C in Recommended Operating Conditions table.	4
• Added Thermal Information table.	5
• Added –40°C to 125°C for SN74AHCT126 in Electrical Characteristics table.	5
• Added –40°C to 125°C for SN74AHCT126 in the Switching Characteristics table.	6
• Added Typical Characteristics.	6
• Added Detailed Description section.	8
• Added Application and Implementation section.	9
• Added Power Supply Recommendations and Layout sections.	10

6 Pin Configuration and Functions

SN54AHCT126 . . . J OR W PACKAGE
SN74AHCT126 . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHCT126 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

Pin Functions

NAME	PIN			I/O	DESCRIPTION
	SN74AHCT126 D, DB, DGV, N, NS, PW	SN54AHCT126 J, W	FK		
1A	2	2	3	I	1A Input
1OE	1	1	2	I	Output Enable 1
1Y	3	3	4	O	1Y Output
2A	5	5	8	I	2A Input
2OE	4	4	6	I	Output Enable 2
2Y	6	6	9	O	2Y Output
3A	9	9	13	I	3A Input
3OE	10	10	14	I	Output Enable 3
3Y	8	8	12	O	3Y Output
4A	12	12	18	I	4A Input
4OE	13	13	19	I	Output Enable 4
4Y	11	11	16	O	4Y Output
GND	7	7	10	—	Ground Pin
NC		—	1	—	No Connection
			5		
			7		
			11		
			15		
V _{CC}	14	14	20	—	Power Pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	–0.5	7	V
V _I	Input voltage range ⁽²⁾	–0.5	7	V
V _O	Output voltage range ⁽²⁾	–0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		–20
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{CC}		±20
I _O	Continuous output current	V _O = 0 to V _{CC}		±25
Continuous current through V _{CC} or GND				±50

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 Handling Ratings

		MIN	MAX	UNIT
T _{stg}	Storage temperature range	–65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾		V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN54AHCT126 ⁽²⁾		SN74AHCT126		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		–8		–8	mA
I _{OL}	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T _A	Operating free-air temperature	–55	125	–40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI Application Report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.
- (2) Product Preview.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHCT126						UNIT
		D	DB	DGV	N	NS	PW	
		14 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	90.6	107.1	129.0	57.4	90.7	122.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	50.9	59.6	52.1	44.9	48.3	51.4	
R _{θJB}	Junction-to-board thermal resistance	44.8	54.4	62.0	37.2	49.4	64.4	
ψ _{JT}	Junction-to-top characterization parameter	14.7	20.5	6.5	30.1	14.6	6.7	
ψ _{JB}	Junction-to-board characterization parameter	44.5	53.8	61.3	37.1	49.1	63.8	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT126		SN74AHCT126		SN74AHCT126 –40 to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 μA	4.5 V	4.4	4.5		4.4		4.4		4.4		V
	I _{OH} = –8 mA		3.94			3.8		3.8		3.8		
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1		0.1		0.1		0.1	V
	I _{OL} = 8 mA				0.36		0.44		0.44		0.44	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1 ⁽¹⁾		±1		±1	μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25		±2.5		±2.5		±2.5	μA
I _{CC}	V _I = V _{CC} or GND I _O = 0	5.5 V			2		20		20		20	μA
ΔI _{CC} ⁽²⁾	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5		1.5		1.5	mA
C _i	V _I = V _{CC} or GND	5 V			4	10			10			pF
C _o	V _O = V _{CC} or GND	5 V			15							pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

7.6 Switching Characteristics, $V_{CC} = 5 V \pm 0.5 V$

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (OUTPUT)	TO (INPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHCT126 –55°C to 125°C		SN74AHCT126 –40°C to 85°C		SN74AHCT126 –40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15 \text{ pF}$	3.8 ⁽¹⁾	5.5 ⁽¹⁾	1 ⁽¹⁾	6.5 ⁽¹⁾	1	6.5	1	7	ns	
t_{PHL}				3.8 ⁽¹⁾	5.5 ⁽¹⁾	1 ⁽¹⁾	6.5 ⁽¹⁾	1	6.5	1	7		
t_{PZH}	OE	Y	$C_L = 15 \text{ pF}$	3.6 ⁽¹⁾	5.1 ⁽¹⁾	1 ⁽¹⁾	6 ⁽¹⁾	1	6	1	6.5	ns	
t_{PZL}				3.6 ⁽¹⁾	5.1 ⁽¹⁾	1 ⁽¹⁾	6 ⁽¹⁾	1	6	1	6.5		
t_{PHZ}	OE	Y	$C_L = 15 \text{ pF}$	4.6 ⁽¹⁾	6.8 ⁽¹⁾	1 ⁽¹⁾	8 ⁽¹⁾	1	8	1	8.5	ns	
t_{PLZ}				4.6 ⁽¹⁾	6.8 ⁽¹⁾	1 ⁽¹⁾	8 ⁽¹⁾	1	8	1	8.5		
t_{PLH}	A	Y	$C_L = 50 \text{ pF}$	5.3	7.5	1	8.5	1	8.5	1	9.5	ns	
t_{PHL}				5.3	7.5	1	8.5	1	8.5	1	9.5		
t_{PZH}	OE	Y	$C_L = 50 \text{ pF}$	5.1	7.1	1	8	1	8	1	9	ns	
t_{PZL}				5.1	7.1	1	8	1	8	1	9		
t_{PHZ}	OE	Y	$C_L = 50 \text{ pF}$	6.1	8.8	1	10	1	10	1	11	ns	
t_{PLZ}				6.1	8.8	1	10	1	10	1	11		
$t_{sk(o)}$			$C_L = 50 \text{ pF}$		1 ⁽²⁾				1		1	ns	

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
 (2) On products compliant to MIL-PRF-38535, this parameter does not apply.

7.7 Noise Characteristics

 $V_{CC} = 5 V$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER	DESCRIPTION	SN74AHCT126		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4		V
$V_{IH(D)}$	High-level dynamic input voltage	2		V
$V_{IL(D)}$	Low-level dynamic input voltage		0.8	V

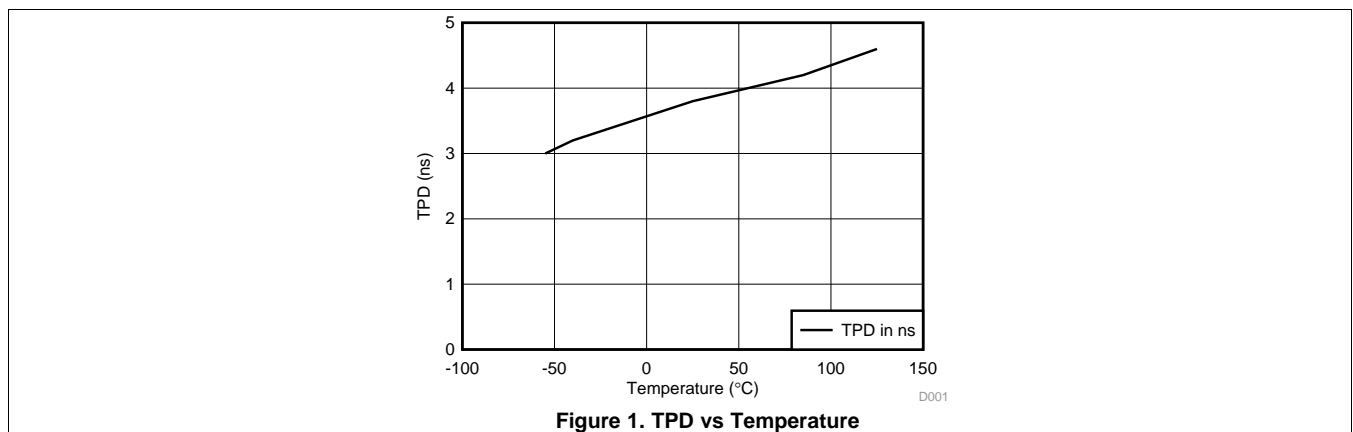
- (1) Characteristics are for surface-mount packages only.

7.8 Operating Characteristics

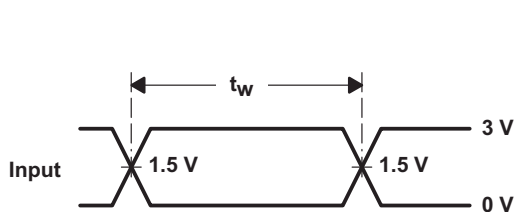
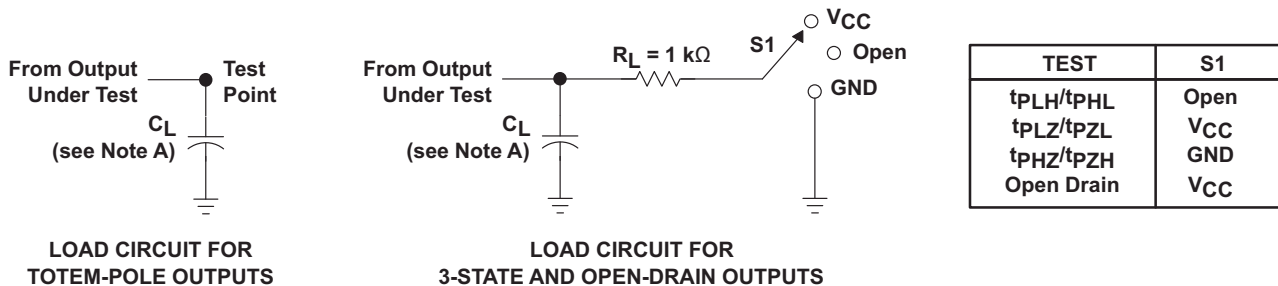
 $V_{CC} = 5 V$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd}	No load, $f = 1 \text{ MHz}$	14	pF

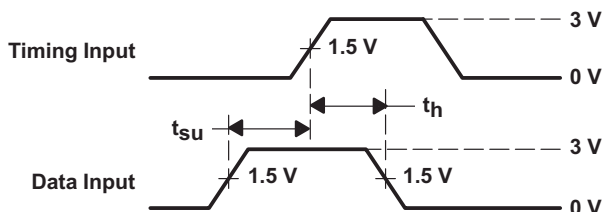
7.9 Typical Characteristics



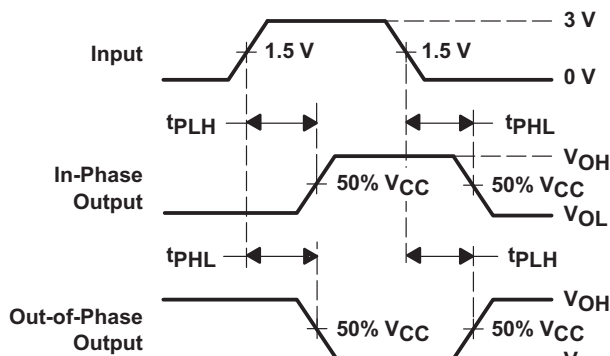
8 Parameter Measurement Information



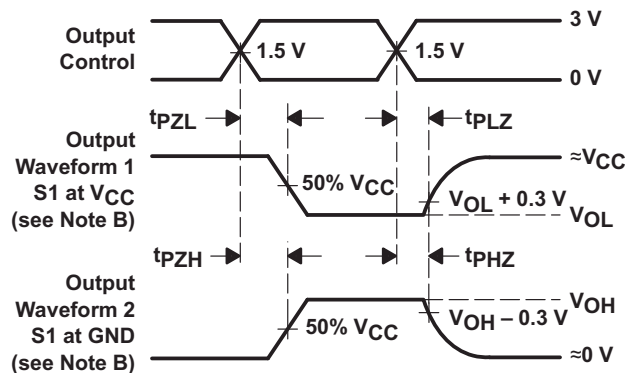
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage and Waveforms

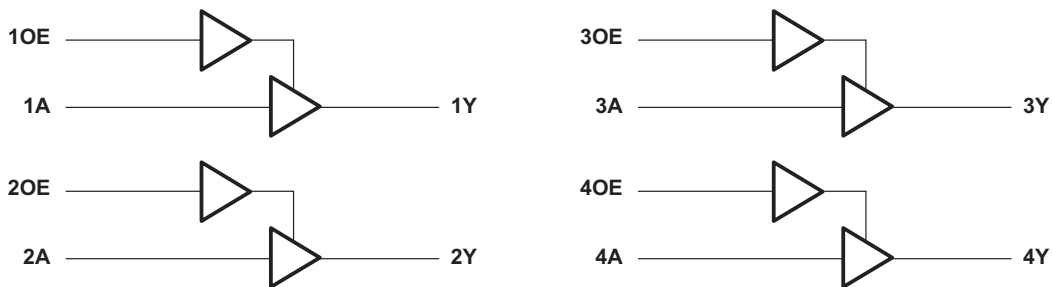
9 Detailed Description

9.1 Overview

The SNxAHCT126 devices are quadruple-bus buffer gates featuring independent line drivers with 3-state outputs.

Each output is disabled when the associated output-enable (OE) input is low. When OE is high, the respective gate passes the data from the A input to its Y output. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

9.2 Functional Block Diagram



9.3 Feature Description

- TTL inputs
 - Lowered switching threshold allows up translation from 3.3 V to 5 V
- Slow edges reduce output ringing

9.4 Device Functional Modes

**Table 1. Function Table
(Each Buffer)**

INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	X	Z

10 Application and Implementation

10.1 Application Information

The SNx4AHCT126 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8-V V_{IL} and 2-V V_{IH} . This feature makes it ideal for translating up from 3.3 V to 5 V. Figure 4 shows this type of translation.

10.2 Typical Application

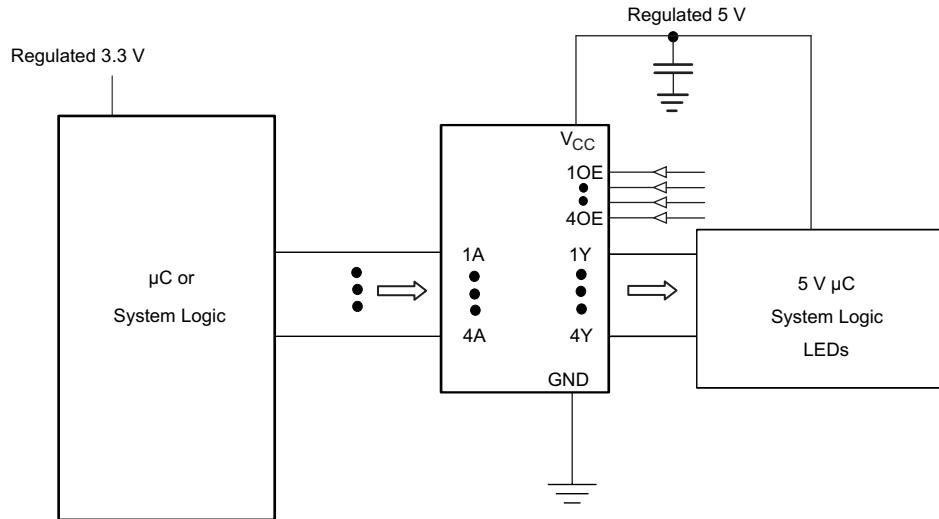


Figure 3. Typical Application Schematic

10.2.1 Design Requirements

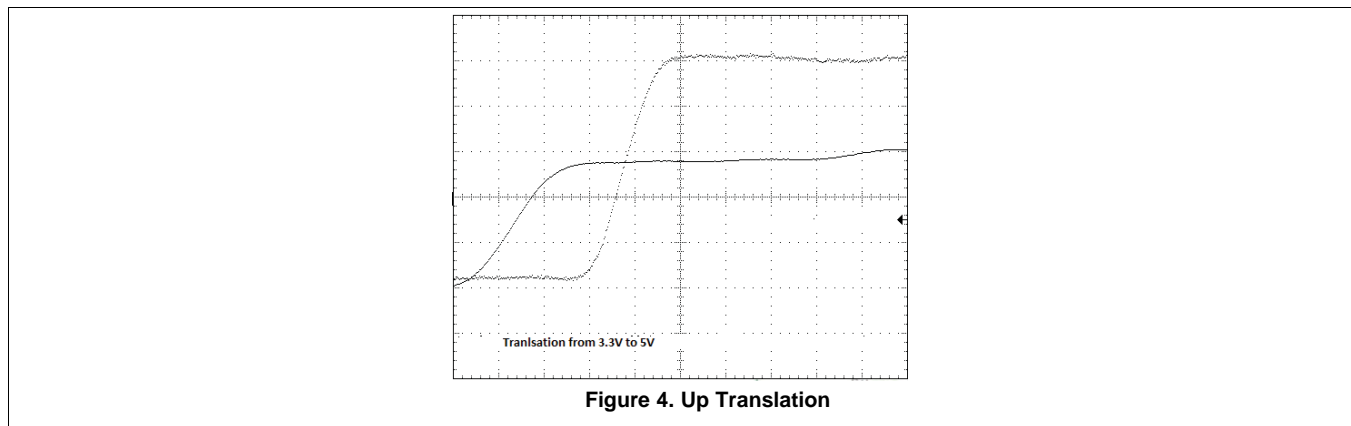
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended input conditions
 - Rise time and fall time specs: See $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
 - Specified High and low levels: See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
2. Recommend output conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part
 - Outputs should not be pulled above V_{CC}

Typical Application (continued)

10.2.3 Application Curves



11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in [Figure 5](#) are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} ; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the IO's so they cannot float when disabled.

12.2 Layout Example

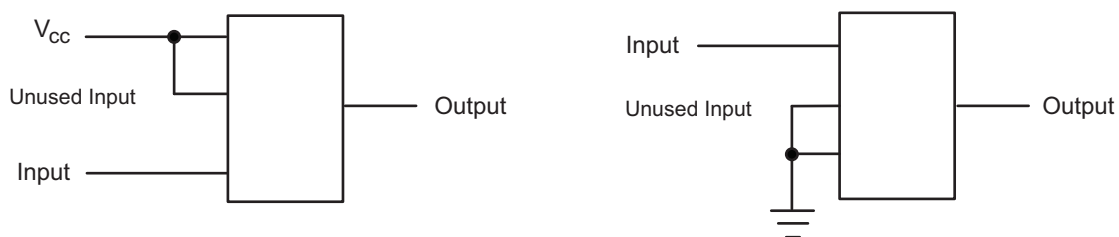


Figure 5. Layout Diagram

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHCT126	Click here	Click here	Click here	Click here	Click here
SN74AHCT126	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

[SLYZ022](#) — *TI Glossary*.




This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9686301Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9686301Q2A SNJ54AHCT 126FK	Samples
5962-9686301QCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9686301QC A SNJ54AHCT126J	Samples
5962-9686301QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9686301QD A SNJ54AHCT126W	Samples
SN74AHCT126D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT126	Samples
SN74AHCT126DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	-40 to 85		
SN74AHCT126DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB126	Samples
SN74AHCT126DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT126	Samples
SN74AHCT126DGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB126	Samples
SN74AHCT126DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT126	Samples
SN74AHCT126DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT126	Samples
SN74AHCT126N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHCT126N	Samples
SN74AHCT126NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT126	Samples
SN74AHCT126PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB126	Samples
SN74AHCT126PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB126	Samples
SN74AHCT126PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85		
SN74AHCT126PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB126	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54AHCT126FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9686301Q2A SNJ54AHCT 126FK	
SNJ54AHCT126J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9686301QC A SNJ54AHCT126J	
SNJ54AHCT126W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9686301QD A SNJ54AHCT126W	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AHCT126, SN74AHCT126 :

- Catalog: [SN74AHCT126](#)
- Automotive: [SN74AHCT126-Q1](#), [SN74AHCT126-Q1](#)
- Enhanced Product: [SN74AHCT126-EP](#), [SN74AHCT126-EP](#)
- Military: [SN54AHCT126](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT126DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AHCT126DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHCT126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHCT126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT126DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74AHCT126DGVR	TVSOP	DGV	14	2000	367.0	367.0	35.0
SN74AHCT126DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74AHCT126PWR	TSSOP	PW	14	2000	367.0	367.0	35.0

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

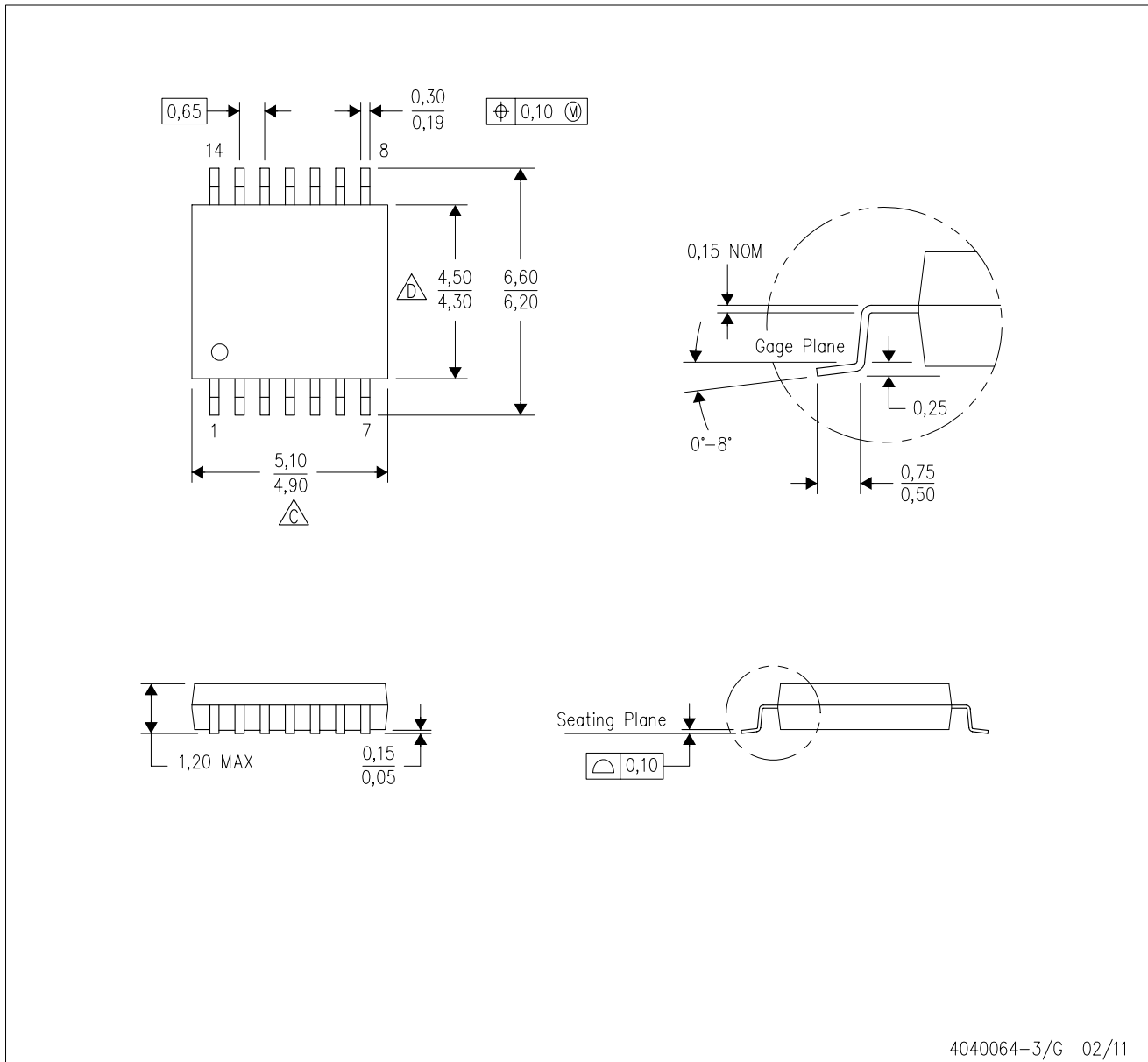


4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

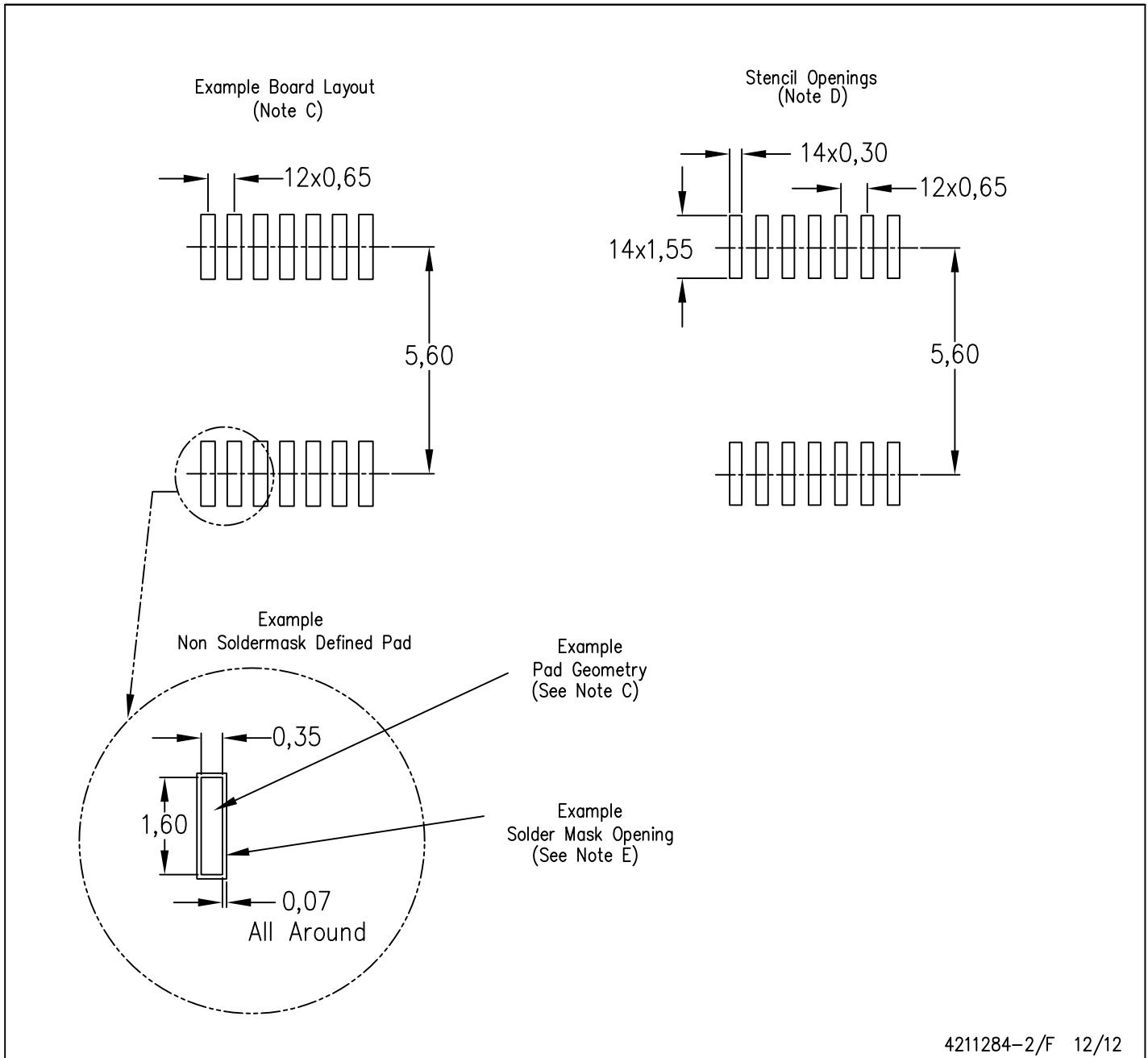
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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