

SN54AHC573, SN74AHC573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCLS242K – OCTOBER 1995 – REVISED JANUARY 2004

- Operating Range 2-V to 5.5-V V_{CC}
- 3-State Outputs Directly Drive Bus Lines
- Latch-Up Performance Exceeds 250 mA Per JESD 17

description/ordering information

The 'AHC573 devices are octal transparent D-type latches designed for 2-V to 5.5-V V_{CC} operation.

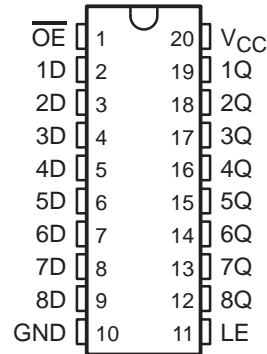
When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

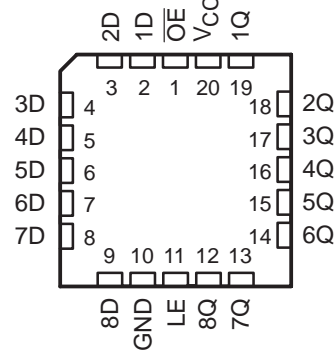
\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54AHC573 . . . J OR W PACKAGE
SN74AHC573 . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC573 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74AHC573N	SN74AHC573N
	SOIC – DW	Tube	SN74AHC573DW	AHC573
		Tape and reel	SN74AHC573DWR	
	SOP – NS	Tape and reel	SN74AHC573NSR	AHC573
	SSOP – DB	Tape and reel	SN74AHC573DBR	HA573
	TSSOP – PW	Tube	SN74AHC573PW	HA573
		Tape and reel	SN74AHC573PWR	
TVSOP – DGV	Tape and reel	SN74AHC573DGVR	HA573	
-55°C to 125°C	CDIP – J	Tube	SNJ54AHC573J	SNJ54AHC573J
	CFP – W	Tube	SNJ54AHC573W	SNJ54AHC573W
	LCCC – FK	Tube	SNJ54AHC573FK	SNJ54AHC573FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

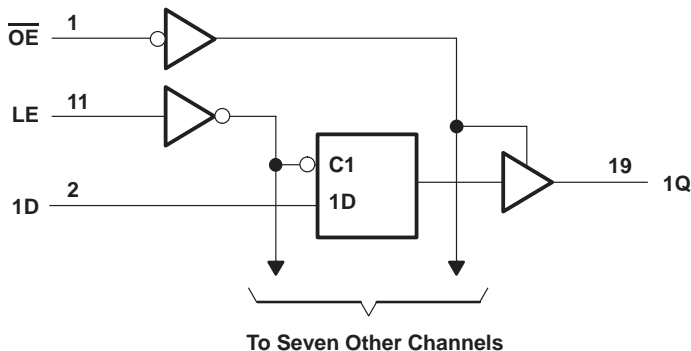
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FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Output voltage range, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	-20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND	± 75 mA
Package thermal impedance, θ_{JA} (see Note 2):	
DB package	70°C/W
DGV package	92°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

		SN54AHC573		SN74AHC573		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5	1.5	V
		V _{CC} = 3 V		2.1	2.1	
		V _{CC} = 5.5 V		3.85	3.85	
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	0.5	V
		V _{CC} = 3 V		0.9	0.9	
		V _{CC} = 5.5 V		1.65	1.65	
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		-50	-50	μA
		V _{CC} = 3.3 V ± 0.3 V		-4	-4	mA
		V _{CC} = 5 V ± 0.5 V		-8	-8	
I _{OL}	Low-level output current	V _{CC} = 2 V		50	50	μA
		V _{CC} = 3.3 V ± 0.3 V		4	4	mA
		V _{CC} = 5 V ± 0.5 V		8	8	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		100	100	ns/V
		V _{CC} = 5 V ± 0.5 V		20	20	
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC573		SN74AHC573		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1	0.1	V	
		3 V			0.1		0.1	0.1		
		4.5 V			0.1		0.1	0.1		
	I _{OL} = 4 mA	3 V			0.36		0.5	0.44		
	I _{OL} = 8 mA	4.5 V			0.36		0.5	0.44		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*	±1	μA	
I _{OZ}	V _I = V _{IL} or V _{IH} , V _O = V _{CC} or GND	5.5 V			±0.25		±2.5	±2.5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40	40	μA	
C _i	V _I = V _{CC} or GND	5 V		2.5	10			10	pF	
C _o	V _O = V _{CC} or GND	5 V		3.5					pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.



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timing requirements over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

	T _A = 25°C		SN54AHC573		SN74AHC573		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t _w Pulse duration, LE high	5		5		5		ns
t _{su} Setup time, data before LE↓	3.5		3.5		3.5		ns
t _h Hold time, data after LE↓	1.5		1.5		1.5		ns

timing requirements over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

	T _A = 25°C		SN54AHC573		SN74AHC573		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t _w Pulse duration, LE high	5		5		5		ns
t _{su} Setup time, data before LE↓	3.5		3.5		3.5		ns
t _h Hold time, data after LE↓	1.5		1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHC573		SN74AHC573		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	C _L = 15 pF	7*	11*		1*	13*	1	13	ns
t _{PHL}				7*	11*	1*	13*	1	13		
t _{PLH}	LE	Q	C _L = 15 pF	7.6*	11.9*		1*	14*	1	14	ns
t _{PHL}				7.6*	11.9*	1*	14*	1	14		
t _{PZH}	\overline{OE}	Q	C _L = 15 pF	7.3*	11.5*		1*	13.5*	1	13.5	ns
t _{PZL}				7.3*	11.5*	1*	13.5*	1	13.5		
t _{PHZ}	\overline{OE}	Q	C _L = 15 pF	8.3*	11*		1*	13*	1	13	ns
t _{PLZ}				8.3*	11*	1*	13*	1	13		
t _{PLH}	D	Q	C _L = 50 pF	9.5	14.5		1	16.5	1	16.5	ns
t _{PHL}				9.5	14.5	1	16.5	1	16.5		
t _{PLH}	LE	Q	C _L = 50 pF	10.1	15.4		1	17.5	1	17.5	ns
t _{PHL}				10.1	15.4	1	17.5	1	17.5		
t _{PZH}	\overline{OE}	Q	C _L = 50 pF	9.8	15		1	17	1	17	ns
t _{PZL}				9.8	15	1	17	1	17		
t _{PHZ}	\overline{OE}	Q	C _L = 50 pF	10.7	14.5		1	16.5	1	16.5	ns
t _{PLZ}				10.7	14.5	1	16.5	1	16.5		
t _{sk(o)}			C _L = 50 pF			1.5**			1.5	ns	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.



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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC573		SN74AHC573		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	$C_L = 15\text{ pF}$		4.5*	6.8*	1	8*	1	8	ns
t_{PHL}				4.5*	6.8*	1	8*	1	8		
t_{PLH}	LE	Q	$C_L = 15\text{ pF}$		5*	7.7*	1	9*	1	9	ns
t_{PHL}				5*	7.7*	1	9*	1	9		
t_{PZH}	\overline{OE}	Q	$C_L = 15\text{ pF}$		5.2*	7.7*	1	9*	1	9	ns
t_{PZL}				5.2*	7.7*	1	9*	1	9		
t_{PHZ}	\overline{OE}	Q	$C_L = 15\text{ pF}$		5.2*	7.7*	1	9*	1	9	ns
t_{PLZ}				5.2*	7.7*	1	9*	1	9		
t_{PLH}	D	Q	$C_L = 50\text{ pF}$		6	8.8	1	10	1	10	ns
t_{PHL}				6	8.8	1	10	1	10		
t_{PLH}	LE	Q	$C_L = 50\text{ pF}$		6.5	9.7	1	11	1	11	ns
t_{PHL}				6.5	9.7	1	11	1	11		
t_{PZH}	\overline{OE}	Q	$C_L = 50\text{ pF}$		6.7	9.7	1	11	1	11	ns
t_{PZL}				6.7	9.7	1	11	1	11		
t_{PHZ}	\overline{OE}	Q	$C_L = 50\text{ pF}$		6.7	9.7	1	11	1	11	ns
t_{PLZ}				6.7	9.7	1	11	1	11		
$t_{sk(o)}$			$C_L = 50\text{ pF}$			1**			1	ns	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER		SN74AHC573		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		1	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4	V
$V_{IH(D)}$	High-level dynamic input voltage		3.5	V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

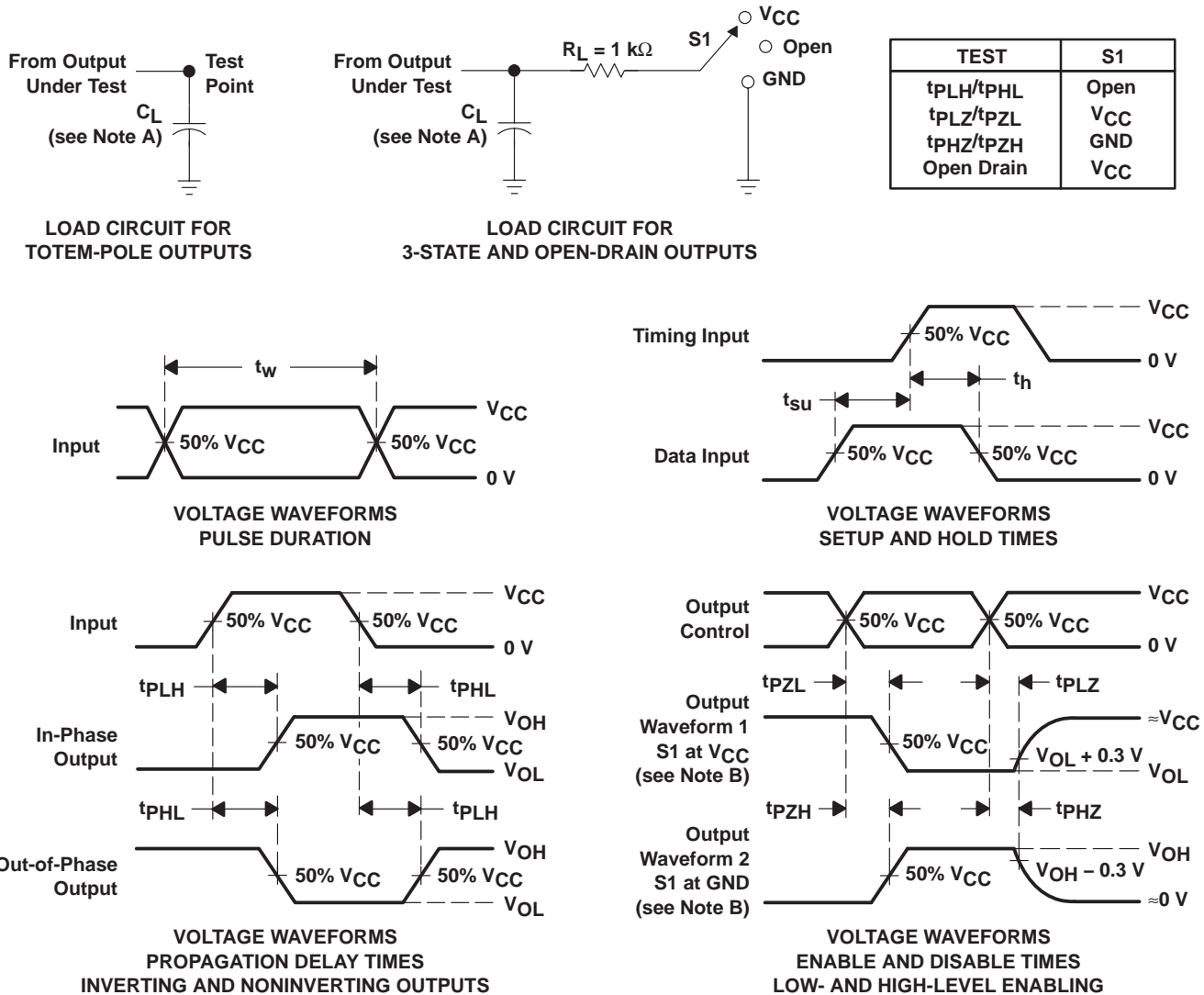
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	16	pF



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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 - The outputs are measured one at a time with one input transition per measurement.
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

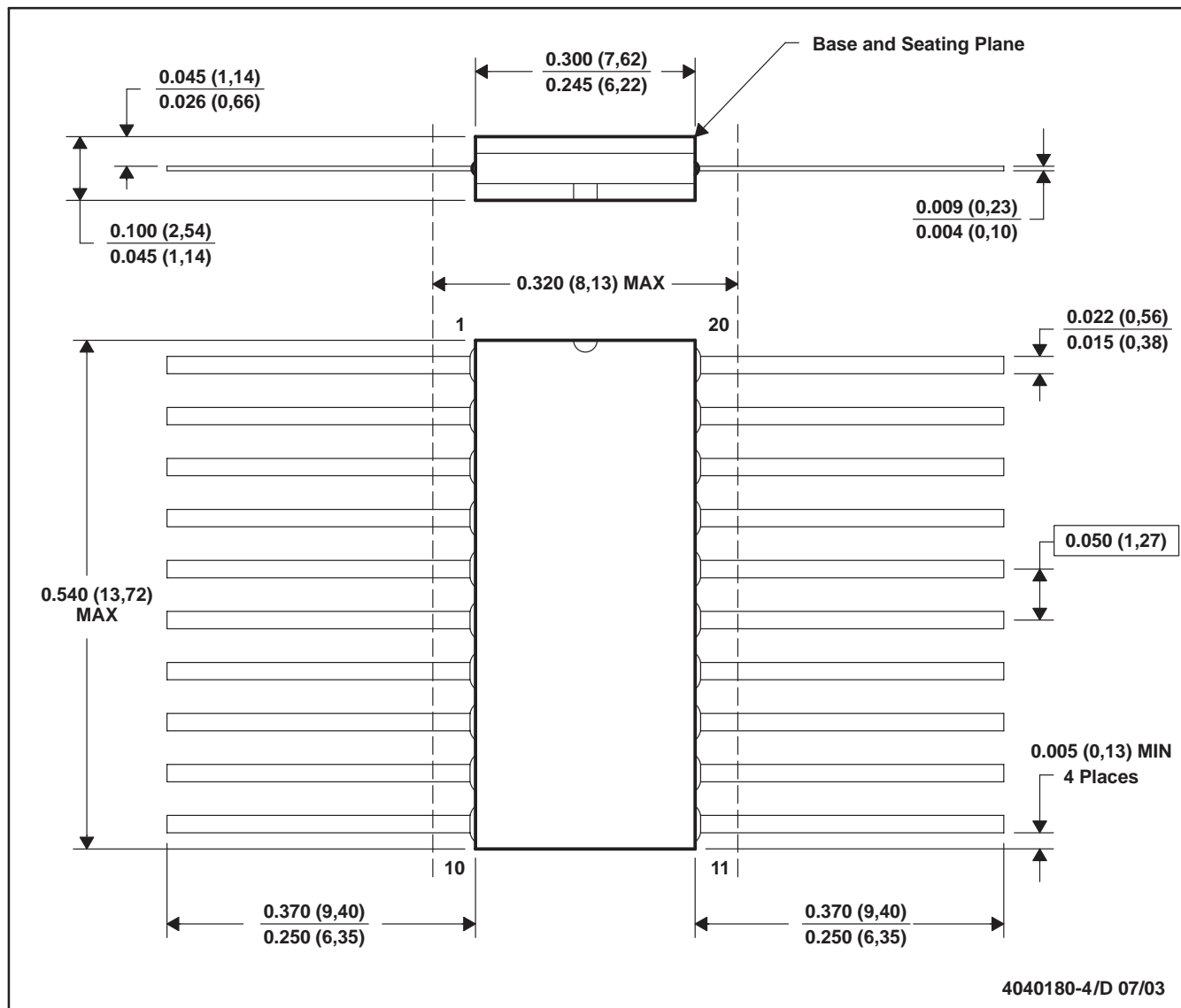


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only.
 E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



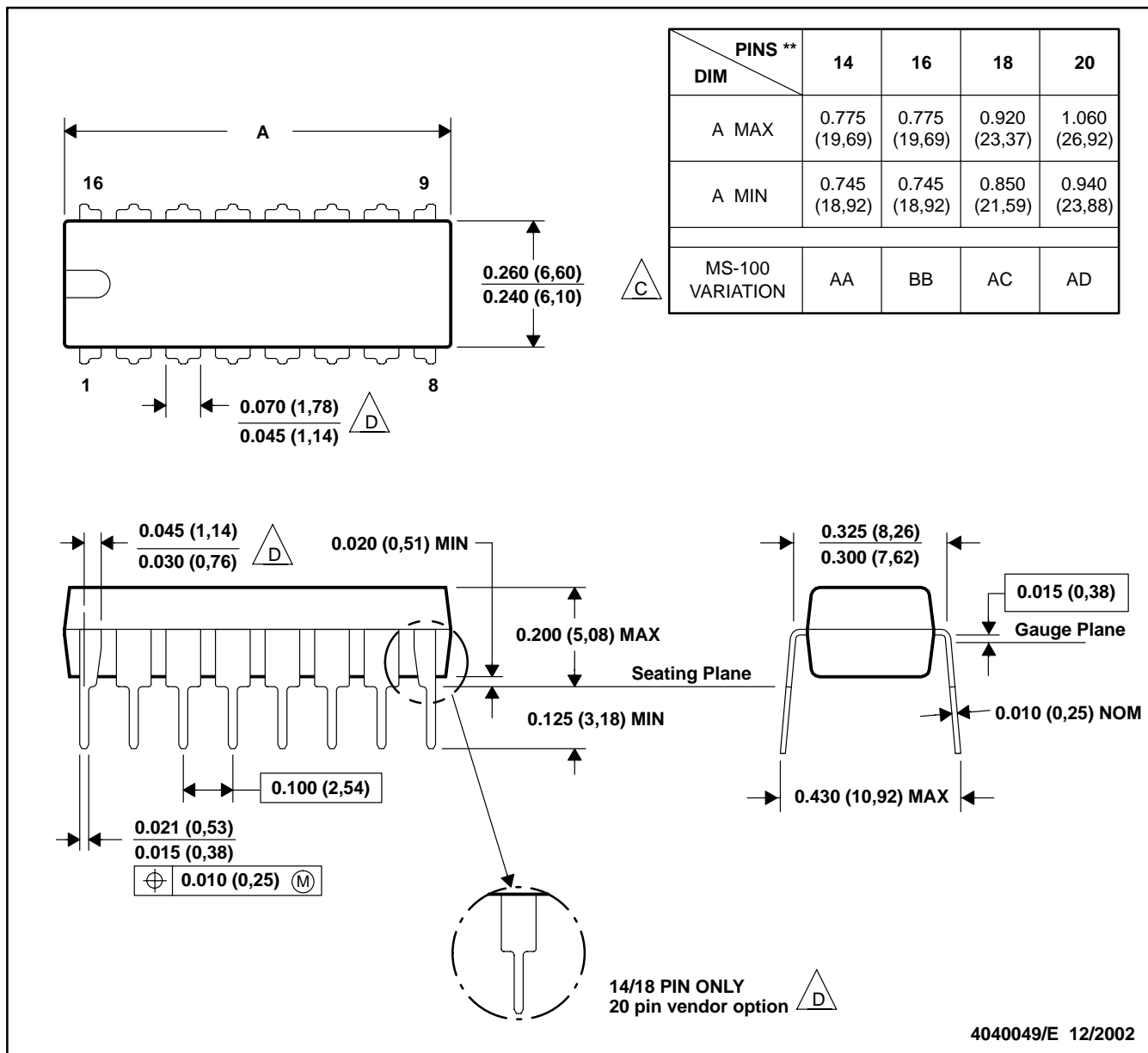
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- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



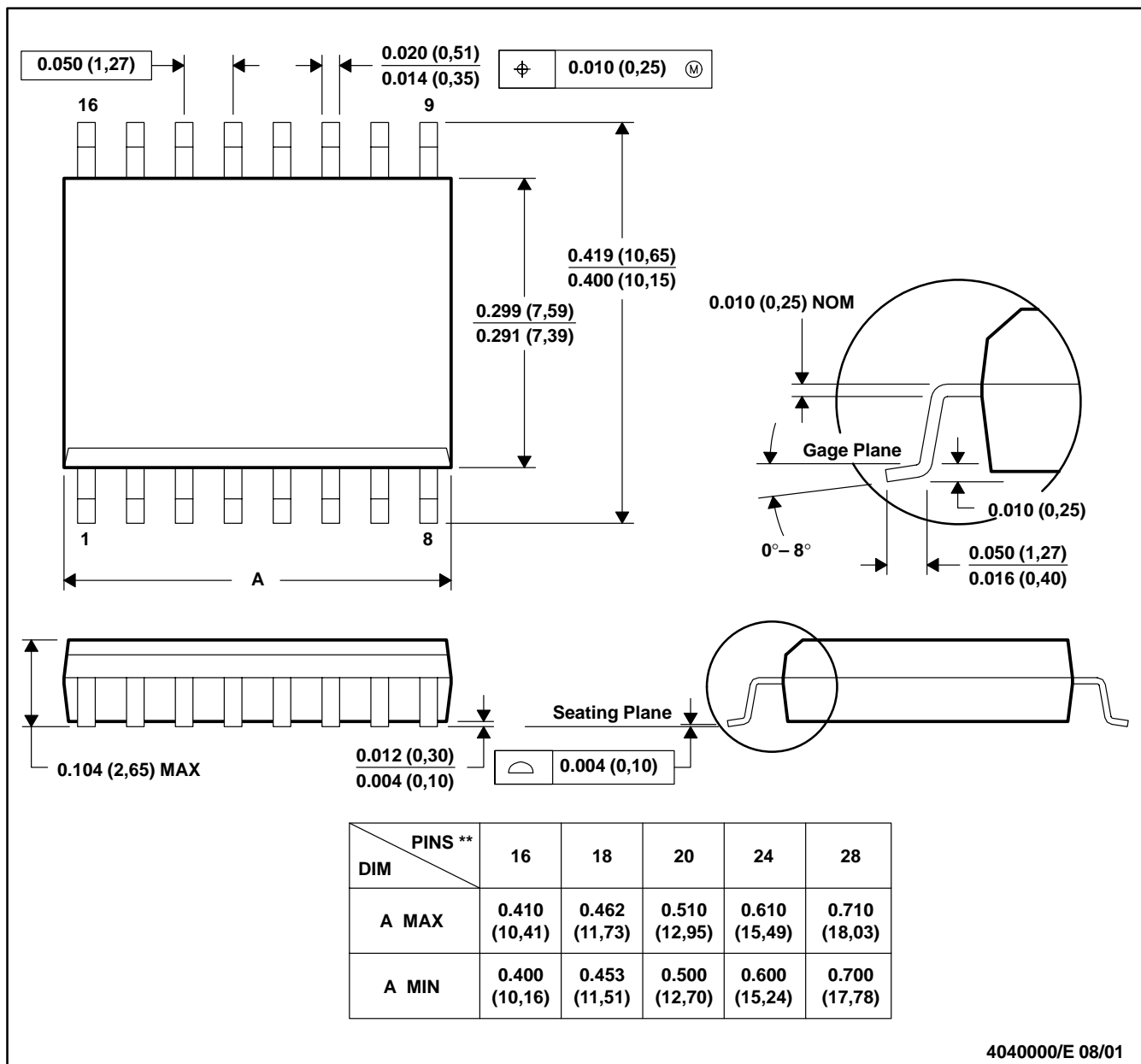
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- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



4040000/E 08/01

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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