

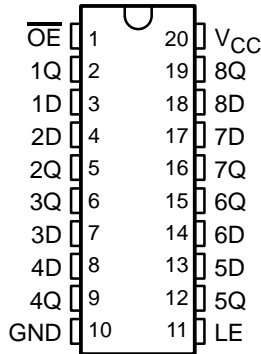
SN54AHC373, SN74AHC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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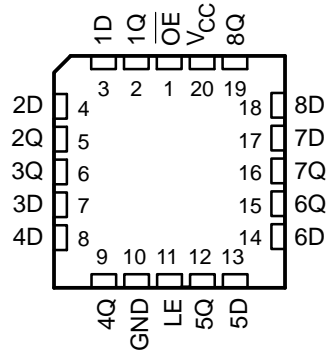
- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17

- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SN54AHC373 . . . J OR W PACKAGE
SN74AHC373 . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC373 . . . FK PACKAGE
(TOP VIEW)



description/ordering information

The 'AHC373 devices are octal transparent D-type latches designed for 2-V to 5.5-V V_{CC} operation.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------|---------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube | SN74AHC373N | SN74AHC373N |
| | SOIC – DW | Tube | SN74AHC373DW | AHC373 |
| | | Tape and reel | SN74AHC373DWR | |
| | SOP – NS | Tape and reel | SN74AHC373NSR | AHC373 |
| | SSOP – DB | Tape and reel | SN74AHC373DBR | HA373 |
| | TSSOP – PW | Tube | SN74AHC373PW | HA373 |
| | | Tape and reel | SN74AHC373PWR | |
| TVSOP – DGV | Tape and reel | SN74AHC373DGV | HA373 | |
| -55°C to 125°C | CDIP – J | Tube | SNJ54AHC373J | SNJ54AHC373J |
| | CFP – W | Tube | SNJ54AHC373W | SNJ54AHC373W |
| | LCCC – FK | Tube | SNJ54AHC373FK | SNJ54AHC373FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54AHC373, SN74AHC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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description/ordering information (continued)

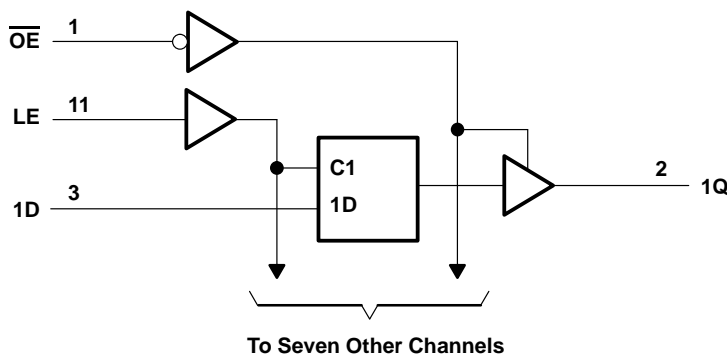
\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each latch)

| INPUTS | | | OUTPUT |
|-----------------|----|---|--------|
| \overline{OE} | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|----------------------------------------------------------------|----------------------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Output voltage range, V_O (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | -20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ± 20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 25 mA |
| Continuous current through V_{CC} or GND | ± 75 mA |
| Package thermal impedance, θ_{JA} (see Note 2): | |
| DB package | 70°C/W |
| DGV package | 92°C/W |
| DW package | 58°C/W |
| N package | 69°C/W |
| NS package | 60°C/W |
| PW package | 83°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.



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SN54AHC373, SN74AHC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

| | | SN54AHC373 | | SN74AHC373 | | UNIT |
|-----------------|------------------------------------|---------------------------------|-----------------|------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 2 | 5.5 | 2 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | | 1.5 | 1.5 | V |
| | | V _{CC} = 3 V | | 2.1 | 2.1 | |
| | | V _{CC} = 5.5 V | | 3.85 | 3.85 | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | | 0.5 | 0.5 | V |
| | | V _{CC} = 3 V | | 0.9 | 0.9 | |
| | | V _{CC} = 5.5 V | | 1.65 | 1.65 | |
| V _I | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 2 V | | -50 | -50 | μA |
| | | V _{CC} = 3.3 V ± 0.3 V | | -4 | -4 | mA |
| | | V _{CC} = 5 V ± 0.5 V | | -8 | -8 | |
| I _{OL} | Low-level output current | V _{CC} = 2 V | | 50 | 50 | μA |
| | | V _{CC} = 3.3 V ± 0.3 V | | 4 | 4 | mA |
| | | V _{CC} = 5 V ± 0.5 V | | 8 | 8 | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 3.3 V ± 0.3 V | | 100 | 100 | ns/V |
| | | V _{CC} = 5 V ± 0.5 V | | 20 | 20 | |
| T _A | Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54AHC373 | | SN74AHC373 | | UNIT |
|-----------------|-----------------------------------------------------------------------------------------------|-----------------|-----------------------|-----|-------|------------|------|------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = -50 μA | 2 V | 1.9 | | | 1.9 | 1.9 | V | | |
| | | 3 V | 2.9 | | | 2.9 | 2.9 | | | |
| | | 4.5 V | 4.4 | | | 4.4 | 4.4 | | | |
| | I _{OH} = -4 mA | 3 V | 2.58 | | | 2.48 | 2.48 | | | |
| | I _{OH} = -8 mA | 4.5 V | 3.94 | | | 3.8 | 3.8 | | | |
| V _{OL} | I _{OL} = 50 μA | 2 V | | | 0.1 | 0.1 | 0.1 | V | | |
| | | 3 V | | | 0.1 | 0.1 | 0.1 | | | |
| | | 4.5 V | | | 0.1 | 0.1 | 0.1 | | | |
| | I _{OL} = 4 mA | 3 V | | | 0.36 | 0.5 | 0.44 | | | |
| | I _{OL} = 8 mA | 4.5 V | | | 0.36 | 0.5 | 0.44 | | | |
| I _I | V _I = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | ±1* | ±1 | μA | | |
| I _{OZ} | V _I = V _{IH} or V _{IL} , V _O = V _{CC} or GND | 5.5 V | | | ±0.25 | ±2.5 | ±2.5 | μA | | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 4 | 40 | 40 | μA | | |
| C _i | V _I = V _{CC} or GND | 5 V | | 4 | 10 | | 10 | pF | | |
| C _o | V _O = V _{CC} or GND | 5 V | | 6 | | | | pF | | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.



SN54AHC373, SN74AHC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see Figure 1)

| | | $T_A = 25^\circ C$ | | SN54AHC373 | | SN74AHC373 | | UNIT |
|----------|-----------------------------|--------------------|-----|------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration, LE high | 5 | | 5 | | 5 | | ns |
| t_{su} | Setup time, data before LE↓ | 4 | | 4 | | 4 | | ns |
| t_h | Hold time, data after LE↓ | 1 | | 1 | | 1 | | ns |

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see Figure 1)

| | | $T_A = 25^\circ C$ | | SN54AHC373 | | SN74AHC373 | | UNIT |
|----------|-----------------------------|--------------------|-----|------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration, LE high | 5 | | 5 | | 5 | | ns |
| t_{su} | Setup time, data before LE↓ | 4 | | 4 | | 4 | | ns |
| t_h | Hold time, data after LE↓ | 1 | | 1 | | 1 | | ns |

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ C$ | | | SN54AHC373 | | SN74AHC373 | | UNIT |
|-------------|-----------------|-------------|-----------------------|--------------------|-------|-------|------------|-------|------------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | D | Q | $C_L = 15 \text{ pF}$ | 7.3* | 11.4* | | 1* | 13.5* | 1 | 13.5 | ns |
| t_{PHL} | | | | 7.3* | 11.4* | | 1* | 13.5* | 1 | 13.5 | |
| t_{PLH} | LE | Q | $C_L = 15 \text{ pF}$ | 7* | 11* | | 1* | 13* | 1 | 13 | ns |
| t_{PHL} | | | | 7* | 11* | | 1* | 13* | 1 | 13 | |
| t_{PZH} | \overline{OE} | Q | $C_L = 15 \text{ pF}$ | 7.3* | 11.4* | | 1* | 13.5* | 1 | 13.5 | ns |
| t_{PZL} | | | | 7.3* | 11.4* | | 1* | 13.5* | 1 | 13.5 | |
| t_{PHZ} | \overline{OE} | Q | $C_L = 15 \text{ pF}$ | 7* | 10* | | 1* | 12* | 1 | 12 | ns |
| t_{PLZ} | | | | 7* | 10* | | 1* | 12* | 1 | 12 | |
| t_{PLH} | D | Q | $C_L = 50 \text{ pF}$ | 9.8 | 14.9 | | 1 | 17 | 1 | 17 | ns |
| t_{PHL} | | | | 9.8 | 14.9 | | 1 | 17 | 1 | 17 | |
| t_{PLH} | LE | Q | $C_L = 50 \text{ pF}$ | 9.5 | 14.5 | | 1 | 16.5 | 1 | 16.5 | ns |
| t_{PHL} | | | | 9.5 | 14.5 | | 1 | 16.5 | 1 | 16.5 | |
| t_{PZH} | \overline{OE} | Q | $C_L = 50 \text{ pF}$ | 9.8 | 14.9 | | 1 | 17 | 1 | 17 | ns |
| t_{PZL} | | | | 9.8 | 14.9 | | 1 | 17 | 1 | 17 | |
| t_{PHZ} | \overline{OE} | Q | $C_L = 50 \text{ pF}$ | 9.5 | 13.2 | | 1 | 15 | 1 | 15 | ns |
| t_{PLZ} | | | | 9.5 | 13.2 | | 1 | 15 | 1 | 15 | |
| $t_{sk(o)}$ | | | $C_L = 50 \text{ pF}$ | | | 1.5** | | | 1.5 | ns | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.



SN54AHC373, SN74AHC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | SN54AHC373 | | SN74AHC373 | | UNIT |
|-------------|-----------------|-------------|----------------------|--------------------------|------|-----|------------|-----|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | D | Q | $C_L = 15\text{ pF}$ | 5* | 7.2* | 1* | 8.5* | 1 | 8.5 | ns | |
| t_{PHL} | | | | 5* | 7.2* | 1* | 8.5* | 1 | 8.5 | | |
| t_{PLH} | LE | Q | $C_L = 15\text{ pF}$ | 4.9* | 7.2* | 1* | 8.5* | 1 | 8.5 | ns | |
| t_{PHL} | | | | 4.9* | 7.2* | 1* | 8.5* | 1 | 8.5 | | |
| t_{PZH} | \overline{OE} | Q | $C_L = 15\text{ pF}$ | 5.5* | 8.1* | 1* | 9.5* | 1 | 9.5 | ns | |
| t_{PZL} | | | | 5.5* | 8.1* | 1* | 9.5* | 1 | 9.5 | | |
| t_{PHZ} | \overline{OE} | Q | $C_L = 15\text{ pF}$ | 5* | 7.2* | 1* | 8.5* | 1 | 8.5 | ns | |
| t_{PLZ} | | | | 5* | 7.2* | 1* | 8.5* | 1 | 8.5 | | |
| t_{PLH} | D | Q | $C_L = 50\text{ pF}$ | 6.5 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns | |
| t_{PHL} | | | | 6.5 | 9.2 | 1 | 10.5 | 1 | 10.5 | | |
| t_{PLH} | LE | Q | $C_L = 50\text{ pF}$ | 6.4 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns | |
| t_{PHL} | | | | 6.4 | 9.2 | 1 | 10.5 | 1 | 10.5 | | |
| t_{PZH} | \overline{OE} | Q | $C_L = 50\text{ pF}$ | 7 | 10.1 | 1 | 11.5 | 1 | 11.5 | ns | |
| t_{PZL} | | | | 7 | 10.1 | 1 | 11.5 | 1 | 11.5 | | |
| t_{PHZ} | \overline{OE} | Q | $C_L = 50\text{ pF}$ | 6.5 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns | |
| t_{PLZ} | | | | 6.5 | 9.2 | 1 | 10.5 | 1 | 10.5 | | |
| $t_{sk(o)}$ | | | $C_L = 50\text{ pF}$ | | 1** | | | | 1 | ns | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

| PARAMETER | | SN74AHC373 | | UNIT |
|-------------|----------------------------------------|------------|-----|------|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic V_{OL} | 0.8 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic V_{OL} | -0.8 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic V_{OH} | 4.1 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | 1.5 | | V |

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

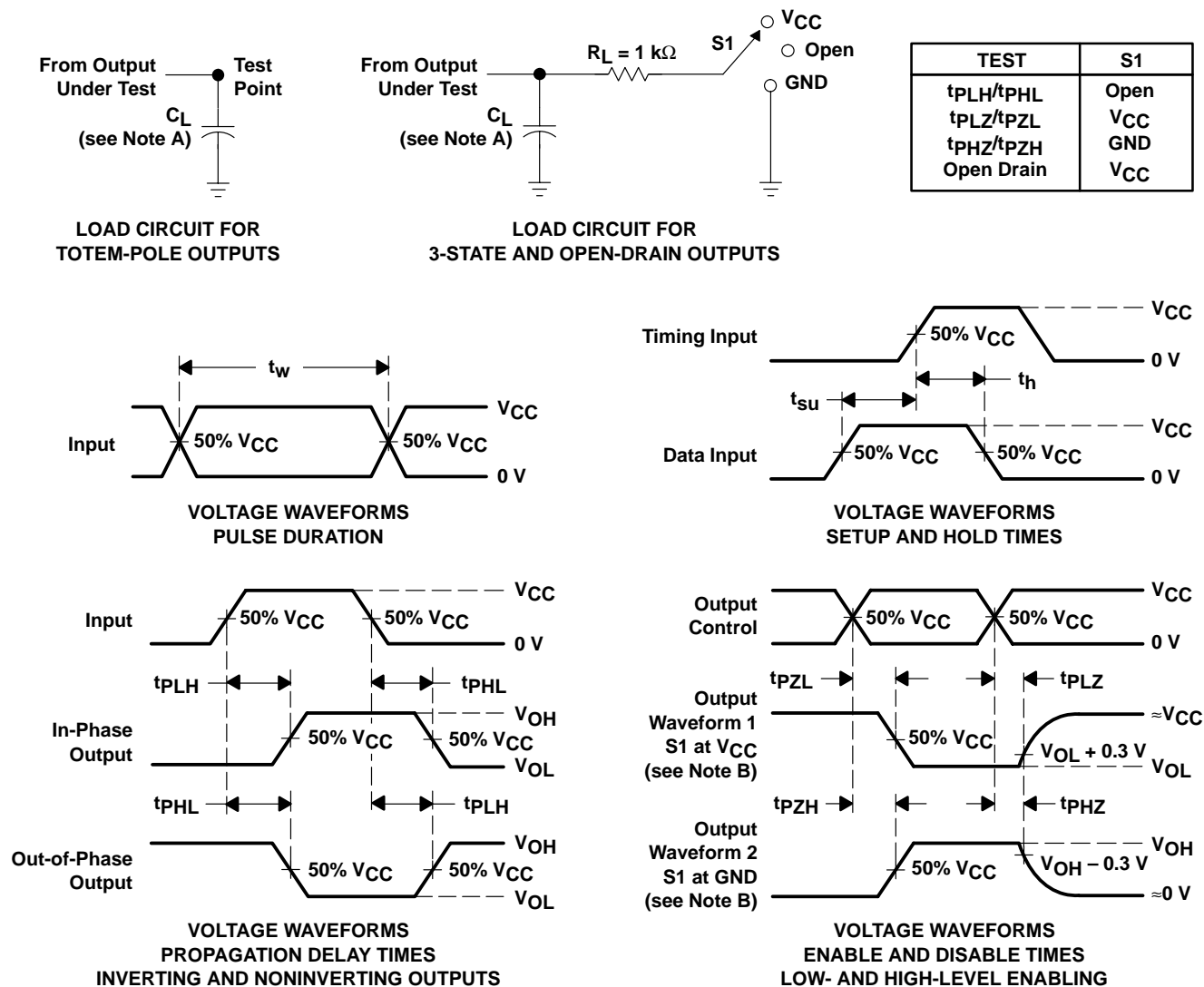
| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------|-------------------------------|-----------------------------|-----|------|
| C_{pd} | Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 18 | pF |



SN54AHC373, SN74AHC373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

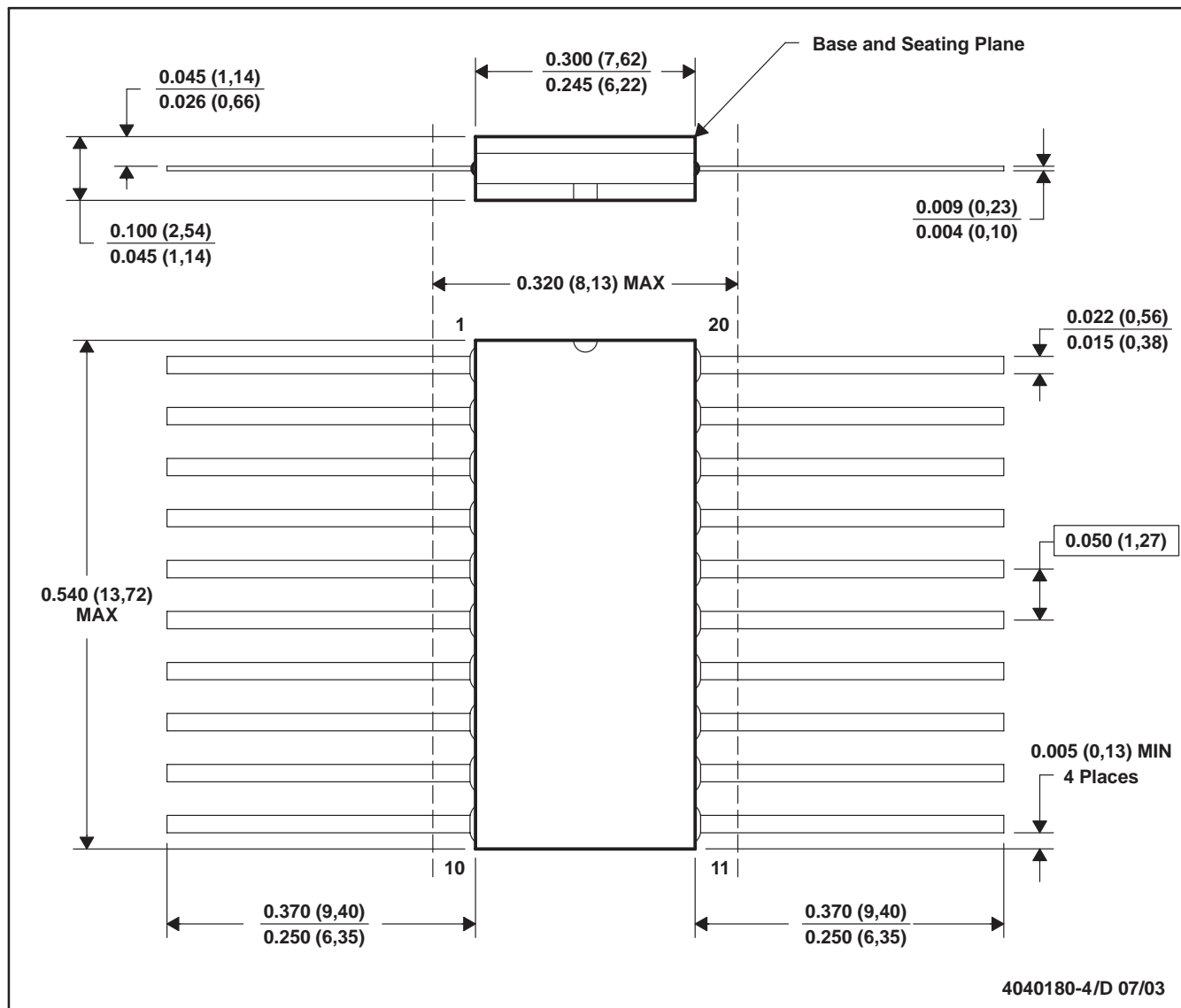


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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