

SN74AHC1G08 Single 2-Input Positive-AND Gate

1 Features

- Operating Range 2 V to 5.5 V
- Maximum t_{pd} of 7 ns at 5 V
- Low Power Consumption, 10- μ A Maximum I_{CC}
- \pm 8-mA Output Drive at 5 V
- Schmitt-Trigger Action at All Inputs Makes the Circuit Tolerant for Slower Input Rise and Fall Time
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Barcode Scanners
- Cable Solutions
- E-Books
- Embedded PCs
- Field Transmitter: Temperature or Pressure Sensors
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning
- Network-Attached Storage (NAS)
- Server Motherboard and PSU
- Software Defined Radios (SDR)
- TV: High Definition (HDTV), LCD, and Digital
- Video Communications Systems
- Wireless Data Access Cards, Headsets, Keyboards, Mice, and LAN Cards

3 Description

The SN74AHC1G08 device is a single 2-input positive-AND gate. The device performs the Boolean function $Y = A \bullet B$ or $Y = A + B$ in positive logic.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|----------------|------------|-------------------|
| SN74AHC1G08DBV | SOT-23 (5) | 2.90 mm x 1.60 mm |
| SN74AHC1G08DCK | SC70 (5) | 2.00 mm x 1.25 mm |
| SN74AHC1G08DRL | SOT (5) | 1.60 mm x 1.20 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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|---|---|

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

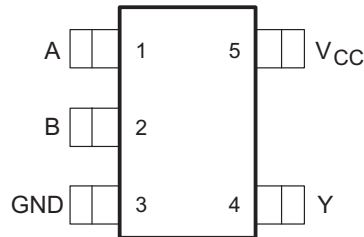
| Changes from Revision O (June 2015) to Revision P | Page |
|---|------|
| • Changed V_{IL} max value on <i>Recommended Operating Conditions</i> table from 5.5 V to 0.5 V | 4 |

| Changes from Revision N (November 2012) to Revision O | Page |
|---|------|
| • Removed <i>Ordering Information</i> table. | 1 |
| • Added <i>Applications</i> | 1 |
| • Added <i>Device Information</i> table. | 1 |
| • Added <i>ESD Ratings</i> table. | 4 |
| • Added <i>Thermal Information</i> table. | 5 |

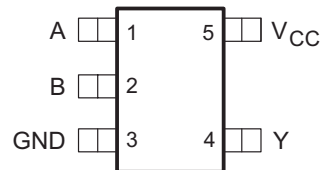
| Changes from Revision M (June 2005) to Revision N | Page |
|---|------|
| • Changed document format from Quicksilver to DocZone. | 1 |

5 Pin Configuration and Functions

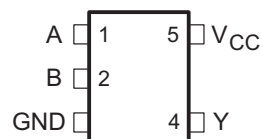
**DBV Package
5-Pin SOT-23
Top View**



**DCK Package
5-Pin SC70
Top View**



**DRL Package
5-Pin SOT
Top View**



See mechanical drawings for dimensions (in [Mechanical, Packaging, and Orderable Information](#)).

Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|------|-----|-------------|
| NO. | NAME | | |
| 1 | A | I | Data Input |
| 2 | B | I | Data Input |
| 3 | GND | — | Ground |
| 4 | Y | O | Data Output |
| 5 | VCC | — | Power |

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------|--|-----------------------------|----------------|------|
| V_{CC} | Supply voltage | -0.5 | 7 | V |
| V_I | Input voltage ⁽²⁾ | -0.5 | 7 | V |
| V_O | Output voltage ⁽²⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | -20 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ or $V_O > V_{CC}$ | ± 20 | mA |
| I_O | Continuous output current | $V_O = 0$ to V_{CC} | ± 25 | mA |
| | Continuous current through V_{CC} or GND | | ± 50 | mA |
| T_J | Junction temperature | | 150 | °C |
| T_{stg} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

| | | VALUE | UNIT |
|-------------|-------------------------|--|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | 2000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | 1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|--|----------|---------------|
| V_{CC} | Supply voltage | 2 | 5.5 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2\text{ V}$ | 1.5 | V |
| | | $V_{CC} = 3\text{ V}$ | 2.1 | |
| | | $V_{CC} = 5.5\text{ V}$ | 3.85 | |
| V_{IL} | Low-level Input voltage | $V_{CC} = 2\text{ V}$ | 0.5 | V |
| | | $V_{CC} = 3\text{ V}$ | 0.9 | |
| | | $V_{CC} = 5.5\text{ V}$ | 1.65 | |
| V_I | Input voltage | 0 | 5.5 | V |
| V_O | Output voltage | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 2\text{ V}$ | -50 | μA |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | -4 | mA |
| | | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | -8 | |
| I_{OL} | Low-level output current | $V_{CC} = 2\text{ V}$ | 50 | μA |
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 4 | mA |
| | | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 100 | ns/V |
| | | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | 20 | |
| T_A | Operating free-air temperature | -55 | 125 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SN74AHC1G08 | | | UNIT |
|---|--------------|------------|-----------|------|
| | DBV (SOT-23) | DCK (SC70) | DRL (SOT) | |
| | 5 PINS | 5 PINS | 5 PINS | |
| R _{θJA} Junction-to-ambient thermal resistance | 206 | 252 | 142 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | T _A = -55°C to 125°C | | UNIT |
|-----------------|---|-----------------|-----------------------|------|------|---------------------------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = -50 μA | 2 V | 1.9 | 2 | | 1.9 | V | |
| | | 3 V | 2.9 | 3 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | |
| | I _{OH} = -4 mA | 3 V | 2.58 | | 2.48 | | | |
| | I _{OH} = -8 mA | 4.5 V | 3.94 | | 3.8 | | | |
| V _{OL} | I _{OL} = 50 μA | 2 V | | | 0.1 | 0.1 | V | |
| | | 3 V | | | 0.1 | 0.1 | | |
| | | 4.5 V | | | 0.1 | 0.1 | | |
| | I _{OL} = 4 mA | 3 V | | 0.36 | 0.44 | | | |
| | I _{OL} = 8 mA | 4.5 V | | 0.36 | 0.44 | | | |
| I _I | V _I = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1 | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 1 | | 10 | μA |
| C _i | V _I = V _{CC} or GND | 5 V | | 4 | 10 | | 10 | pF |

6.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Figure 2](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | OUTPUT CAPACITANCE | T _A = 25°C | | | T _A = -40°C to 85°C | | T _A = -55°C to 125°C | | UNIT |
|------------------|--------------|-------------|------------------------|-----------------------|------|-----|--------------------------------|------|---------------------------------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A or B | Y | C _L = 15 pF | 6.2 | 8.8 | | 1 | 10.5 | 1 | 11 | ns |
| t _{PHL} | | | | 6.2 | 8.8 | | 1 | 10.5 | 1 | 11 | |
| t _{PLH} | A or B | Y | C _L = 50 pF | 8.7 | 12.3 | | 1 | 14 | 1 | 14.5 | ns |
| t _{PHL} | | | | 8.7 | 12.3 | | 1 | 14 | 1 | 14.5 | |

6.7 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 2](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | OUTPUT CAPACITANCE | T _A = 25°C | | | T _A = -40°C to 85°C | | T _A = -55°C to 125°C | | UNIT |
|------------------|--------------|-------------|------------------------|-----------------------|-----|-----|--------------------------------|-----|---------------------------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A or B | Y | C _L = 15 pF | 4.3 | 5.9 | | 1 | 7 | 1 | 7.5 | ns |
| t _{PHL} | | | | 4.3 | 5.9 | | 1 | 7 | 1 | 7.5 | |
| t _{PLH} | A or B | Y | C _L = 50 pF | 5.8 | 7.9 | | 1 | 9 | 1 | 9.5 | ns |
| t _{PHL} | | | | 5.8 | 7.9 | | 1 | 9 | 1 | 9.5 | |

SN74AHC1G08

SCLS314P – MARCH 1996 – REVISED MARCH 2016

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6.8 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------------------|-----|------|
| C_{pd} Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 18 | pF |

6.9 Typical Characteristics

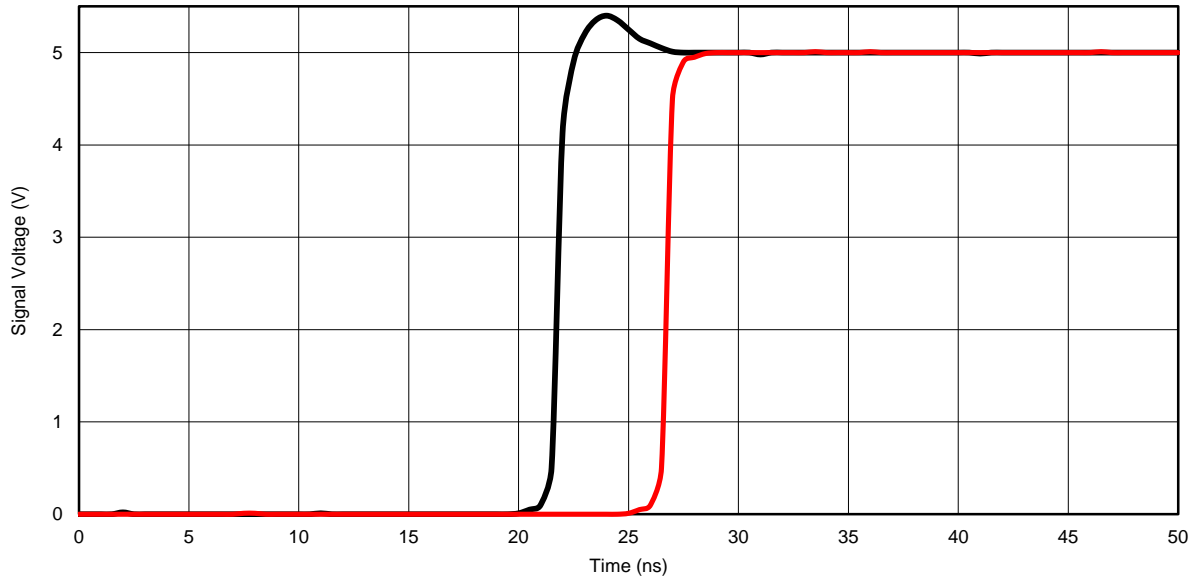
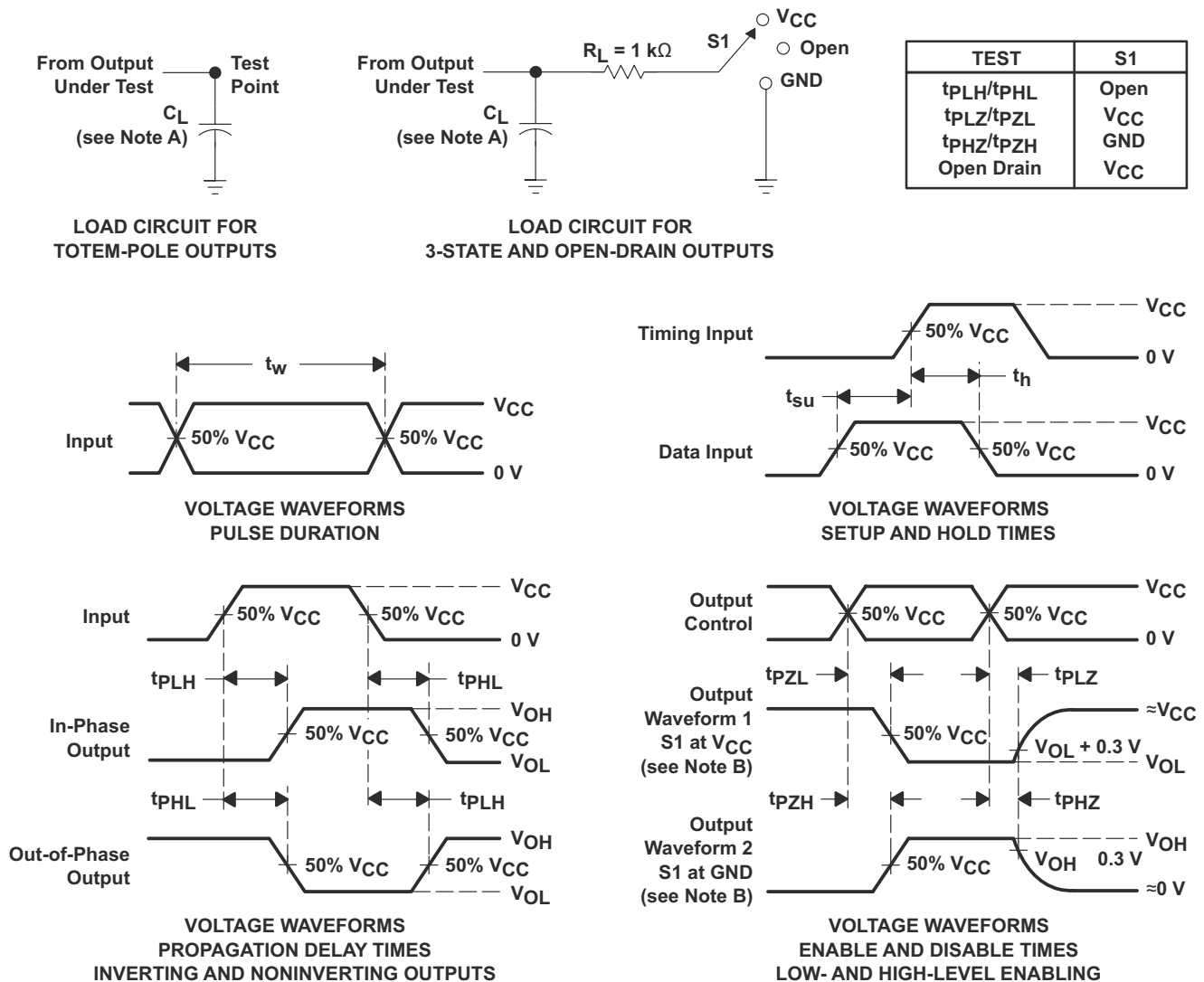


Figure 1. Response Time vs Output Voltage ($T_A = 25^\circ\text{C}$, $V_A = 5\text{ V}$)

7 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74AHC1G08 device is a single 2-input positive-AND gate. The device performs the Boolean function $Y = A \bullet B$ or $Y = A + B$ in positive logic.

8.2 Functional Block Diagram

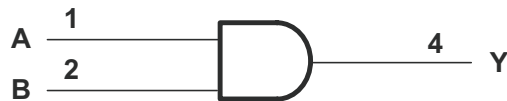


Figure 3. Logic Diagram (Positive Side)

8.3 Feature Description

The SN74AHC1G08 device has a wide operating V_{CC} range of 2 V to 5.5 V, which allows it to be used in a broad range of systems. The low propagation delay allows fast switching and higher operation speeds. In addition, the low-power consumption makes this device a good choice for portable and battery power-sensitive applications.

8.4 Device Functional Modes

[Table 1](#) lists the functional modes for SN74AHC1G08.

Table 1. Function Table

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| H | H | H |
| L | X | L |
| X | L | L |

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A common application for AND gates is their use in power sequencing. Power sequencing is often employed in applications that require a processor or other delicate device with specific voltage timing requirements in order to protect the device from malfunctioning. Using the SN74AHC1G08 to verify that the processor has turned on can protect it from any harmful signals.

9.2 Typical Application

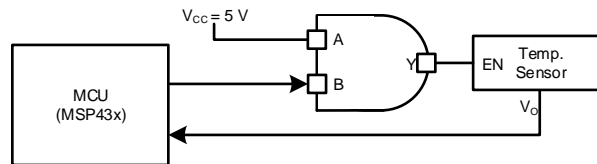


Figure 4. Power Sequencing Application

9.2.1 Design Requirements

The SN74AHC1G08 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

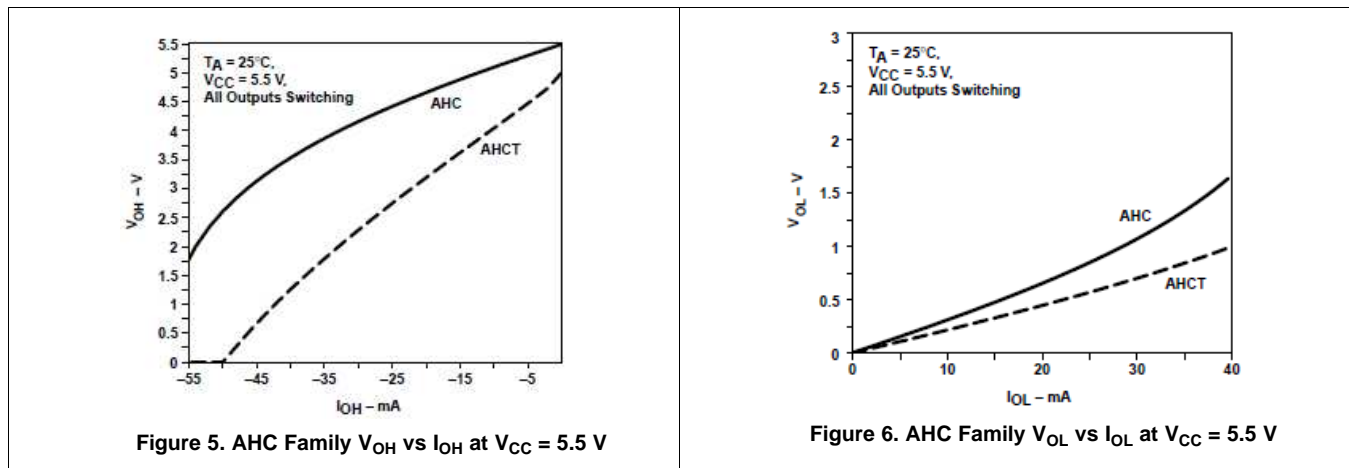
The SN74AHC1G08 allows switching control of analog and digital signals with a digital control signal. All input signals should remain as close to either 0 V or V_{CC} as possible for optimal operation.

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta v$ in the [Recommended Operating Conditions](#) table.
 - For specified high and low levels, see V_{IH} and V_{IL} in the [Recommended Operating Conditions](#) table.
 - Inputs and outputs are overvoltage tolerant and can therefore go as high as 5.5 V at any valid V_{CC} .
2. Recommended output conditions:
 - Load currents should not exceed ± 50 mA.
3. Frequency selection criterion:
 - The effects of frequency upon the device's power consumption should be studied in *CMOS Power Consumption and CPD Calculation*, [SCAA035](#).
 - Added trace resistance and capacitance can reduce maximum frequency capability; follow the layout practices listed in the [Layout](#) section.

Typical Application (continued)

9.2.3 Application Curves



10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the [Recommended Operating Conditions](#) table.

Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A $0.1\text{-}\mu\text{F}$ bypass capacitor is recommended for devices with a single supply. If multiple pins are labeled V_{CC} , then a $0.01\text{-}\mu\text{F}$ or $0.022\text{-}\mu\text{F}$ capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD} , a $0.1\text{-}\mu\text{F}$ bypass capacitor is recommended for each supply pin. Use multiple bypass capacitors in parallel to reject different frequencies of noise. Capacitors with values of $0.1\text{ }\mu\text{F}$ and $1\text{ }\mu\text{F}$ are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [Figure 7](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

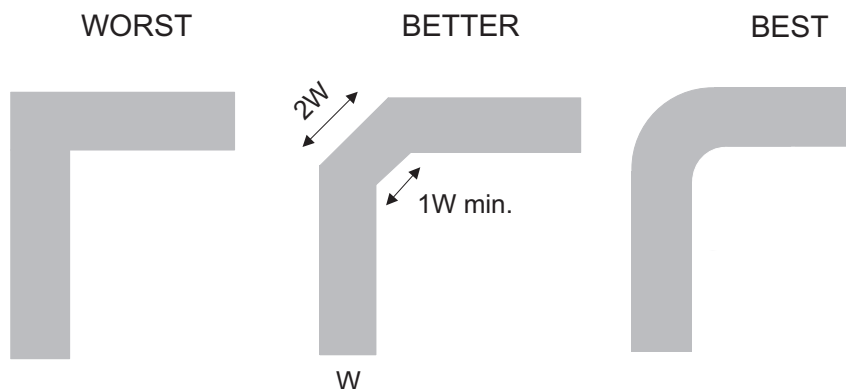


Figure 7. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)
- *CMOS Power Consumption and CPD Calculation*, [SCAA035](#)
- *Selecting the Right Texas Instruments Signal Switch*, [SZZA030](#)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-----------------------------|-------------------------|
| SN74AHC1G08DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -55 to 125 | (A083 ~ A08G ~ A08L ~ A08S) | Samples |
| SN74AHC1G08DBVRE4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | A08G | Samples |
| SN74AHC1G08DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | A08G | Samples |
| SN74AHC1G08DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -55 to 125 | (A083 ~ A08G ~ A08L ~ A08S) | Samples |
| SN74AHC1G08DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | A08G | Samples |
| SN74AHC1G08DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | (AE3 ~ AEG ~ AEL ~ AES) | Samples |
| SN74AHC1G08DCKRE4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | (AE3 ~ AEG ~ AEL ~ AES) | Samples |
| SN74AHC1G08DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | (AE3 ~ AEG ~ AEL ~ AES) | Samples |
| SN74AHC1G08DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | (AE3 ~ AEG ~ AEL ~ AES) | Samples |
| SN74AHC1G08DCKTE4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | (AE3 ~ AEG ~ AEL ~ AES) | Samples |
| SN74AHC1G08DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | (AE3 ~ AEG ~ AEL ~ AES) | Samples |
| SN74AHC1G08DRLR | ACTIVE | SOT | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | (AEB ~ AES) | Samples |
| SN74AHC1G08DRLRG4 | ACTIVE | SOT | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | (AEB ~ AES) | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74AHC1G08 :

- Automotive: [SN74AHC1G08-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHC1G08DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AHC1G08DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.2 | 3.17 | 3.23 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AHC1G08DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AHC1G08DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AHC1G08DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AHC1G08DBVTG4 | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AHC1G08DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AHC1G08DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AHC1G08DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AHC1G08DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AHC1G08DCKT | SC70 | DCK | 5 | 250 | 180.0 | 9.2 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AHC1G08DRLR | SOT | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74AHC1G08DRLR | SOT | DRL | 5 | 4000 | 180.0 | 9.5 | 1.78 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |

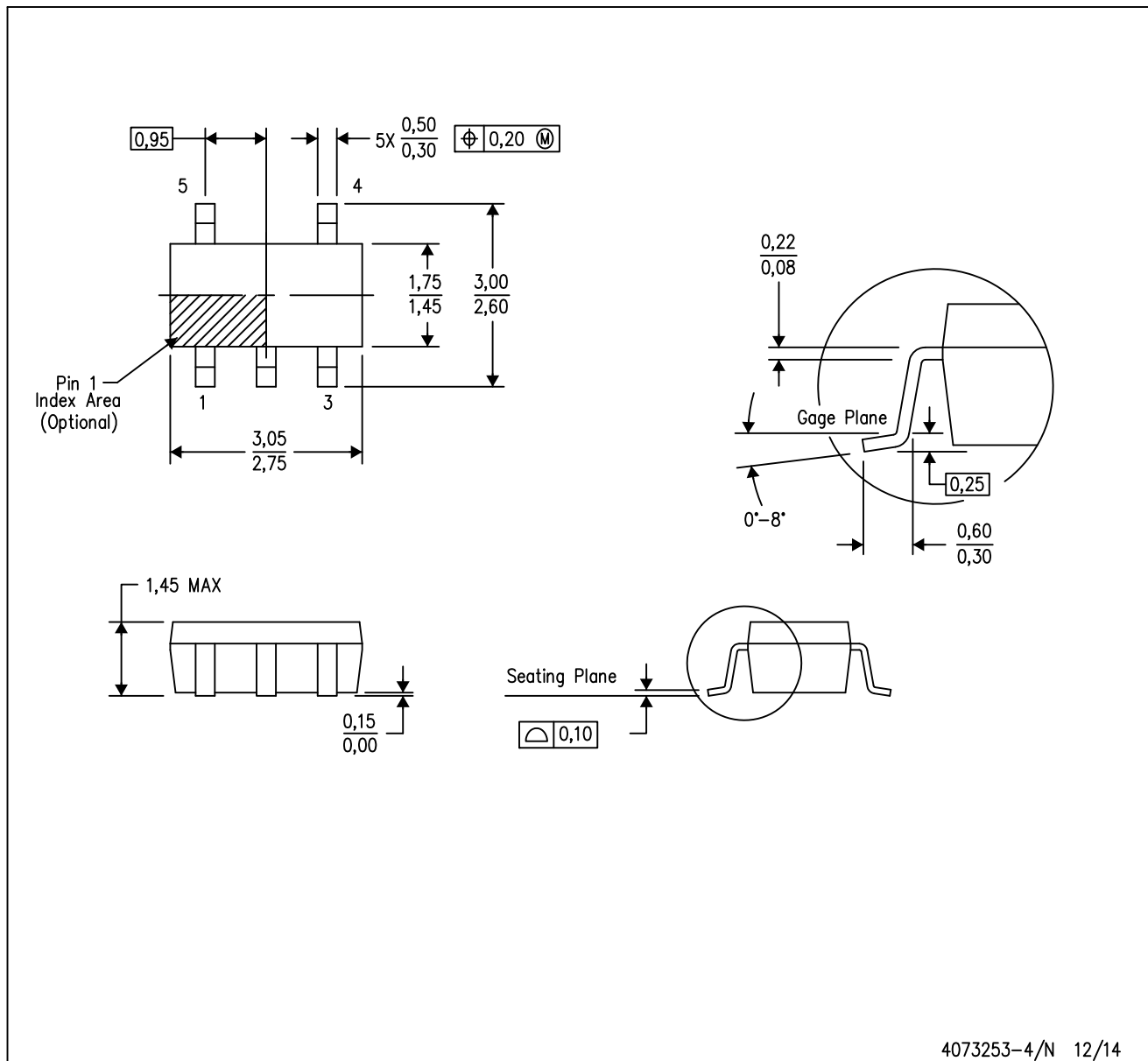
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHC1G08DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AHC1G08DBVR | SOT-23 | DBV | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74AHC1G08DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AHC1G08DBVT | SOT-23 | DBV | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74AHC1G08DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74AHC1G08DBVTG4 | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74AHC1G08DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AHC1G08DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AHC1G08DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74AHC1G08DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74AHC1G08DCKT | SC70 | DCK | 5 | 250 | 205.0 | 200.0 | 33.0 |
| SN74AHC1G08DRLR | SOT | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74AHC1G08DRLR | SOT | DRL | 5 | 4000 | 184.0 | 184.0 | 19.0 |

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/N 12/14

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



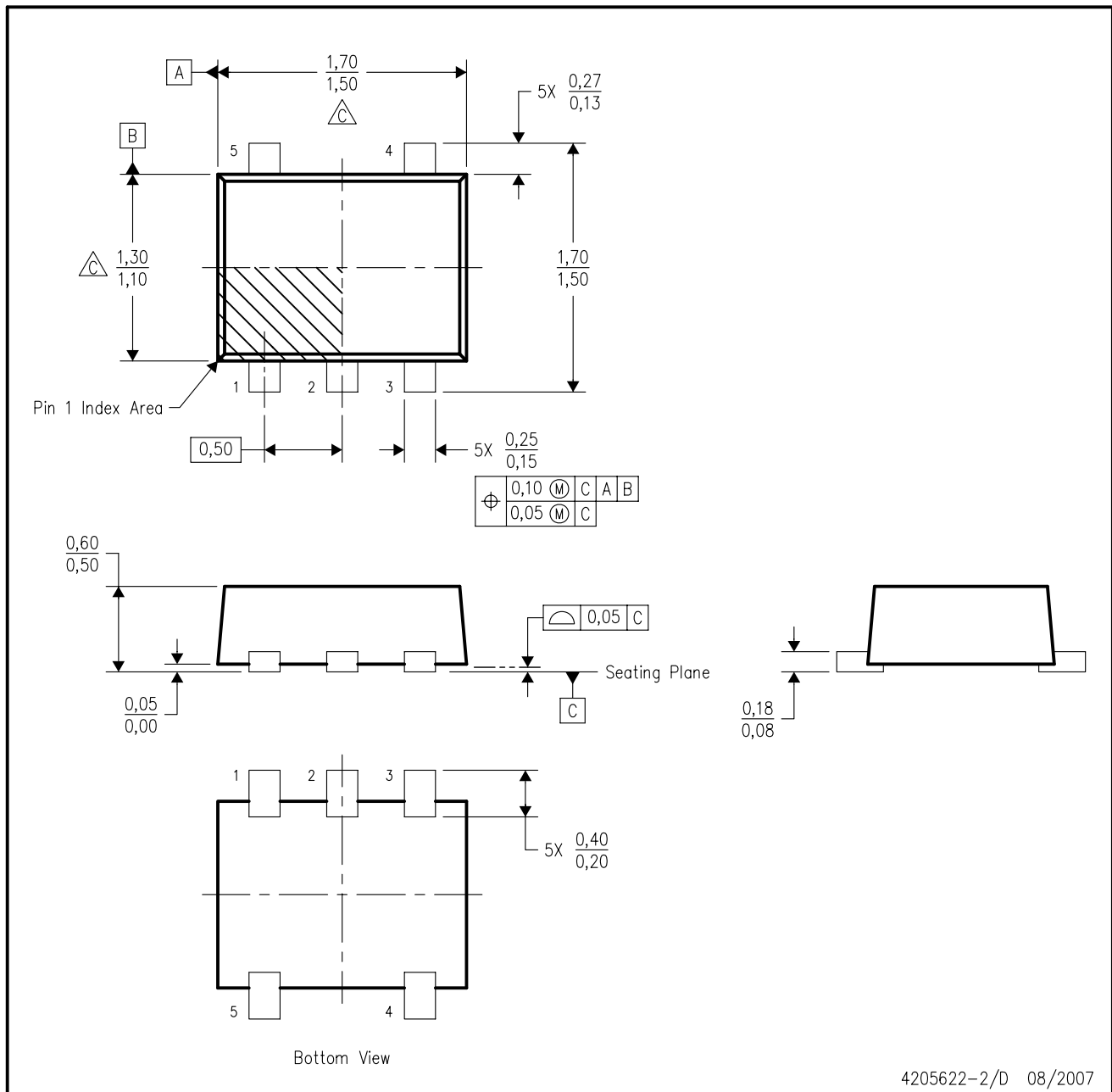
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

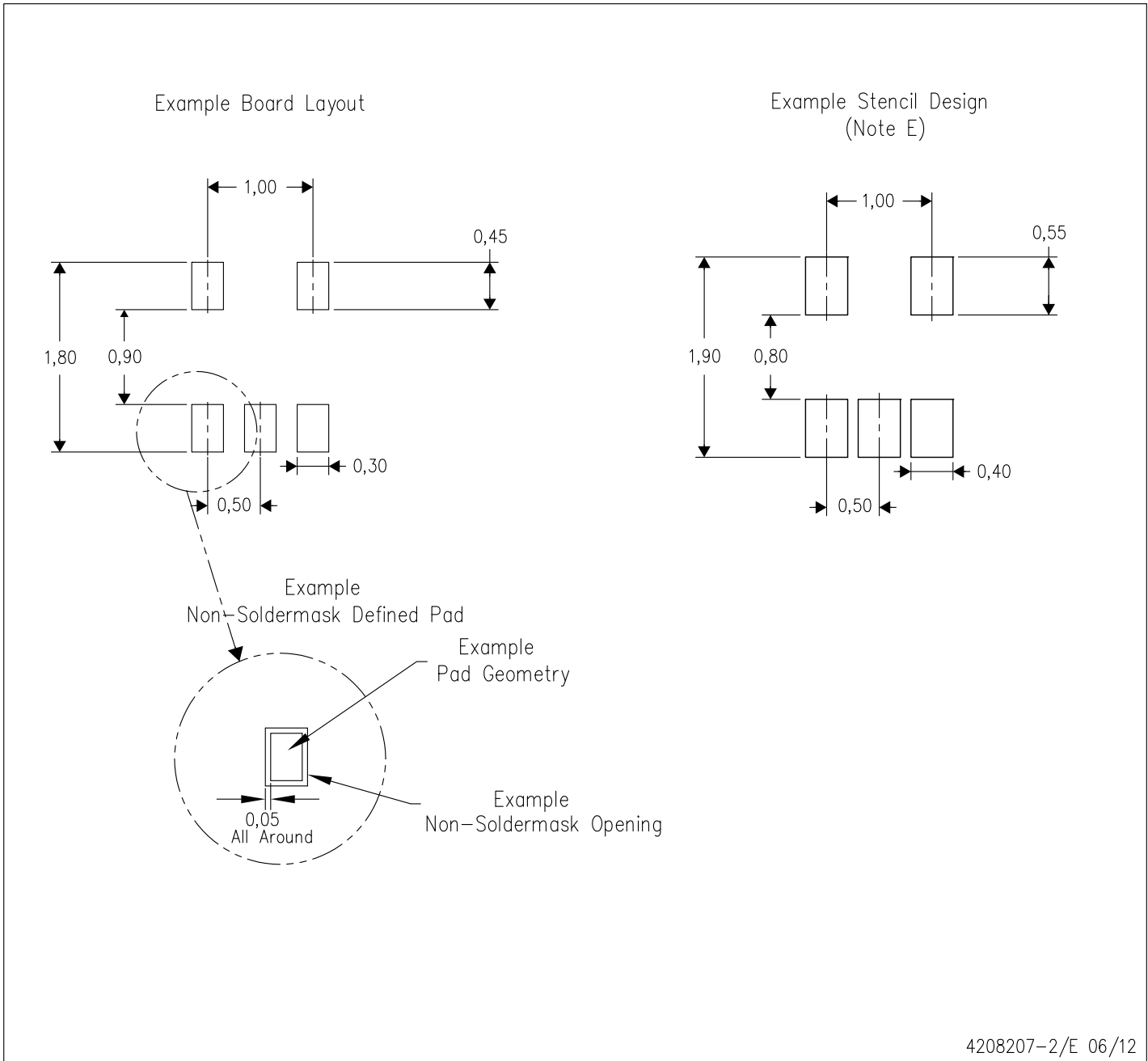
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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