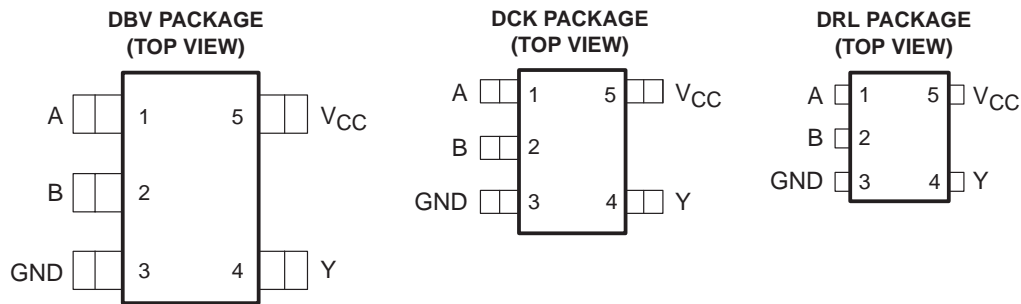


SN74AHC1G02 SINGLE 2-INPUT POSITIVE-NOR GATE

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- Operating Range of 2 V to 5.5 V
- Max t_{pd} of 6.5 ns at 5 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 8 -mA Output Drive at 5 V
- Schmitt Trigger Action at All Inputs Makes the Circuit Tolerant for Slower Input Rise and Fall Time
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

description/ordering information

This device contains a single 2-input NOR gate that performs the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

ORDERING INFORMATION

| T_A | PACKAGE [†] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING [‡] |
|---------------|----------------------|--------------|-----------------------|-------------------------------|
| -40°C to 85°C | SOT (SOT-23) – DBV | Reel of 3000 | SN74AHC1G02DBVR | A02_ |
| | | Reel of 250 | SN74AHC1G02DBVT | |
| | SOT (SC-70) – DCK | Reel of 3000 | SN74AHC1G02DCKR | AB_ |
| | | Reel of 250 | SN74AHC1G02DCKT | |
| | SOT (SOT-553) – DRL | Reel of 4000 | SN74AHC1G02DRLR | AB_ |

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

[‡] The actual top-side marking has one additional character that designates the assembly/test site.

FUNCTION TABLE

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | X | L |
| X | H | L |
| L | L | H |

logic diagram (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN74AHC1G02

SINGLE 2-INPUT POSITIVE-NOR GATE

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Output voltage range, V_O (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | -20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±25 mA |
| Continuous current through V_{CC} or GND | ±50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): DBV package | 206°C/W |
| DCK package | 252°C/W |
| DRL package | 142°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|------------------------------------|----------|------|
| V_{CC} | Supply voltage | 2 | 5.5 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2$ V | 1.5 | V |
| | | $V_{CC} = 3$ V | 2.1 | |
| | | $V_{CC} = 5.5$ V | 3.85 | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2$ V | 0.5 | V |
| | | $V_{CC} = 3$ V | 0.9 | |
| | | $V_{CC} = 5.5$ V | 1.65 | |
| V_I | Input voltage | 0 | 5.5 | V |
| V_O | Output voltage | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 2$ V | -50 | μA |
| | | $V_{CC} = 3.3 \text{ V} \pm 0.3$ V | -4 | mA |
| | | $V_{CC} = 5 \text{ V} \pm 0.5$ V | -8 | |
| I_{OL} | Low-level output current | $V_{CC} = 2$ V | 50 | μA |
| | | $V_{CC} = 3.3 \text{ V} \pm 0.3$ V | 4 | mA |
| | | $V_{CC} = 5 \text{ V} \pm 0.5$ V | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 3.3 \text{ V} \pm 0.3$ V | 100 | ns/V |
| | | $V_{CC} = 5 \text{ V} \pm 0.5$ V | 20 | |
| T_A | Operating free-air temperature | -40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN74AHC1G02

SINGLE 2-INPUT POSITIVE-NOR GATE

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|-----------------|---|-----------------|-----------------------|-----|------|------|-----|------|
| | | | MIN | TYP | MAX | | | |
| V _{OH} | I _{OH} = -50 μA | 2 V | 1.9 | 2 | | 1.9 | V | |
| | | 3 V | 2.9 | 3 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | |
| | I _{OH} = -4 mA | 3 V | 2.58 | | | 2.48 | | |
| | I _{OH} = -8 mA | 4.5 V | 3.94 | | | 3.8 | | |
| V _{OL} | I _{OL} = 50 μA | 2 V | | | 0.1 | 0.1 | V | |
| | | 3 V | | | 0.1 | 0.1 | | |
| | | 4.5 V | | | 0.1 | 0.1 | | |
| | I _{OL} = 4 mA | 3 V | | | 0.36 | 0.44 | | |
| | I _{OL} = 8 mA | 4.5 V | | | 0.36 | 0.44 | | |
| I _I | V _I = 5.5 V or GND | 0 V to 5.5 V | | | | ±0.1 | ±1 | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | | 1 | 10 | μA |
| C _i | V _I = V _{CC} or GND | 5 V | | 4 | 10 | | 10 | pF |

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | MIN | MAX | UNIT |
|------------------|--------------|-------------|------------------------|-----------------------|-----|------|-----|-----|------|
| | | | | MIN | TYP | MAX | | | |
| t _{PLH} | A or B | Y | C _L = 15 pF | | 5.6 | 7.9 | 1 | 9.5 | ns |
| t _{PHL} | | | | | 5.6 | 7.9 | 1 | 9.5 | |
| t _{PLH} | A or B | Y | C _L = 50 pF | | 8.1 | 11.4 | 1 | 13 | ns |
| t _{PHL} | | | | | 8.1 | 11.4 | 1 | 13 | |

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | MIN | MAX | UNIT |
|------------------|--------------|-------------|------------------------|-----------------------|-----|-----|-----|-----|------|
| | | | | MIN | TYP | MAX | | | |
| t _{PLH} | A or B | Y | C _L = 15 pF | | 3.6 | 5.5 | 1 | 6.5 | ns |
| t _{PHL} | | | | | 3.6 | 5.5 | 1 | 6.5 | |
| t _{PLH} | A or B | Y | C _L = 50 pF | | 5.1 | 7.5 | 1 | 8.5 | ns |
| t _{PHL} | | | | | 5.1 | 7.5 | 1 | 8.5 | |

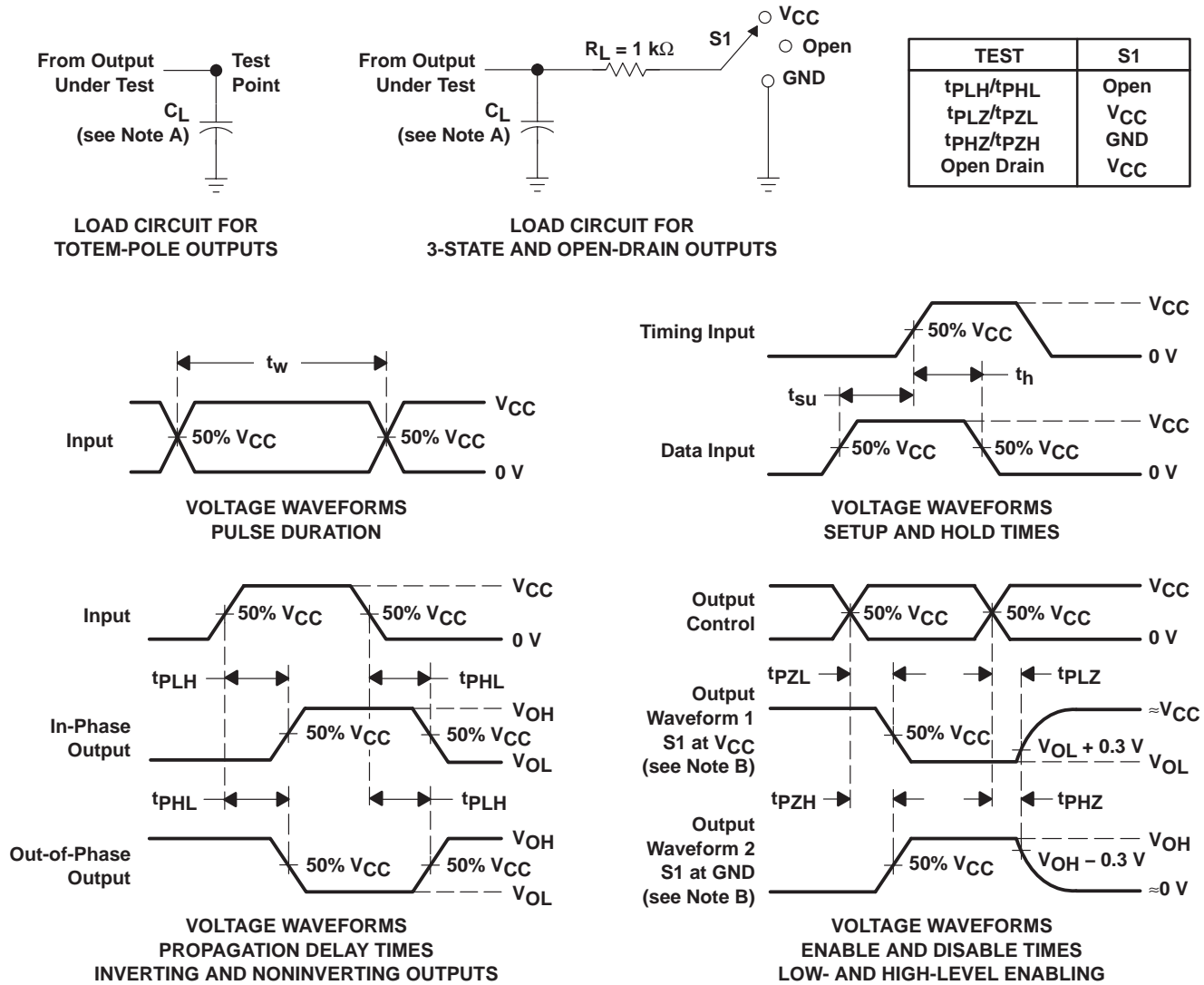
operating characteristics, V_{CC} = 5 V, T_A = 25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|---|--------------------|-----|------|
| C _{pd} Power dissipation capacitance | No load, f = 1 MHz | 15 | pF |

SN74AHC1G02 SINGLE 2-INPUT POSITIVE-NOR GATE

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74AHC1G02DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC1G02DBVRE4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC1G02DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC1G02DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC1G02DBVTE4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC1G02DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC1G02DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC1G02DCKRE4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC1G02DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC1G02DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC1G02DCKTE4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC1G02DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC1G02DRLR | ACTIVE | SOT | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74AHC1G02DRLRG4 | ACTIVE | SOT | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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- Enhanced Product: [SN74AHC1G02-EP](#)

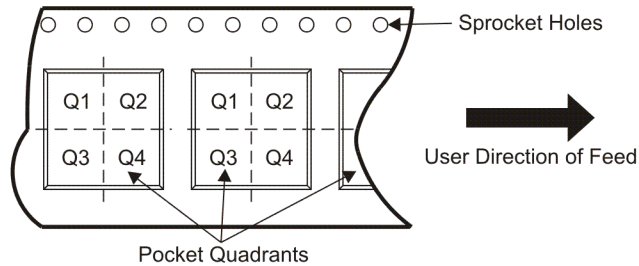
NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHC1G02DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AHC1G02DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 9.2 | 2.24 | 2.34 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AHC1G02DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AHC1G02DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AHC1G02DRLR | SOT | DRL | 5 | 4000 | 180.0 | 9.2 | 1.78 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS

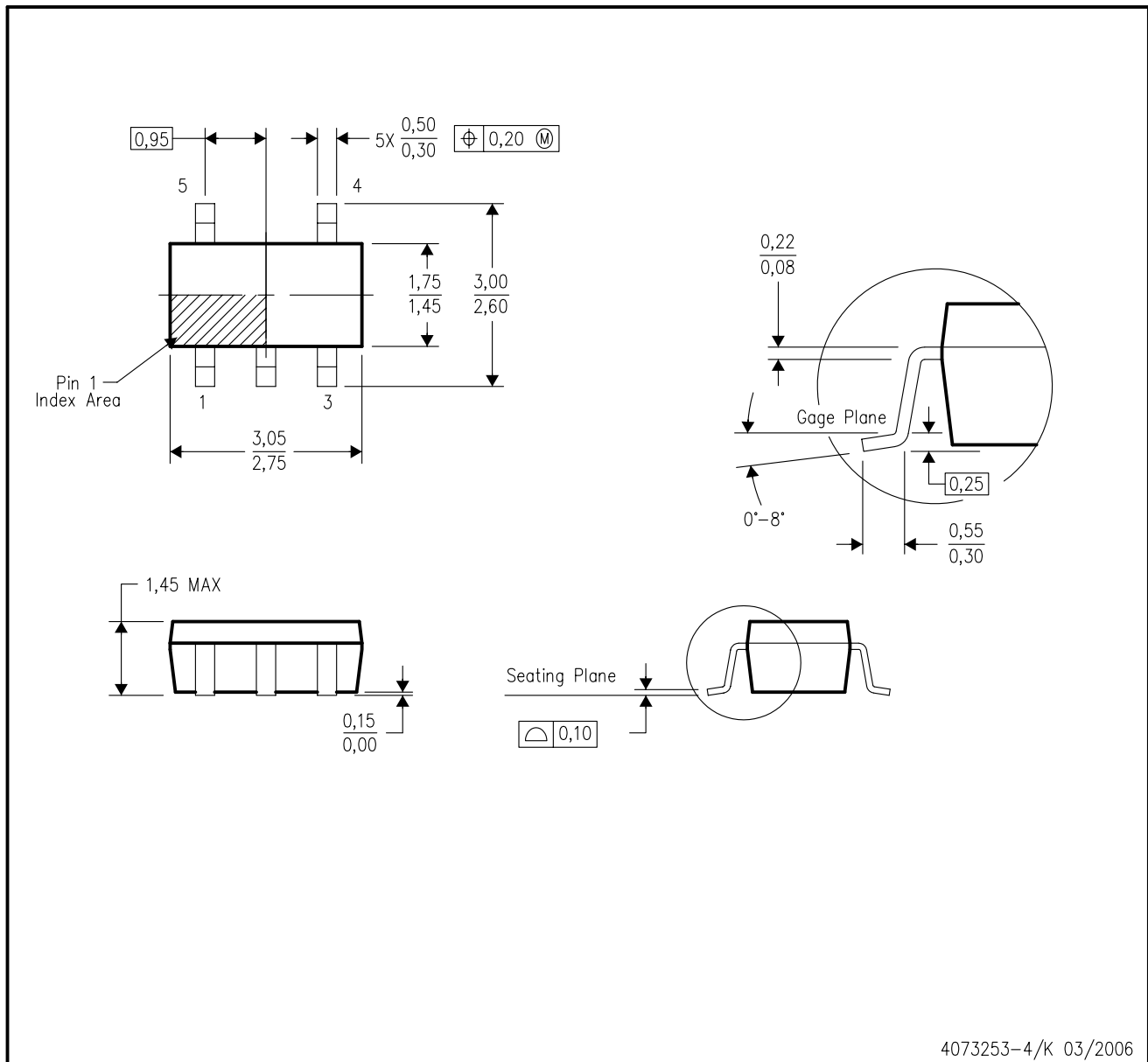


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHC1G02DBVR | SOT-23 | DBV | 5 | 3000 | 565.0 | 140.0 | 75.0 |
| SN74AHC1G02DCKR | SC70 | DCK | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74AHC1G02DCKR | SC70 | DCK | 5 | 3000 | 565.0 | 140.0 | 75.0 |
| SN74AHC1G02DCKT | SC70 | DCK | 5 | 250 | 565.0 | 140.0 | 75.0 |
| SN74AHC1G02DRLR | SOT | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |

DBV (R-PDSO-G5)

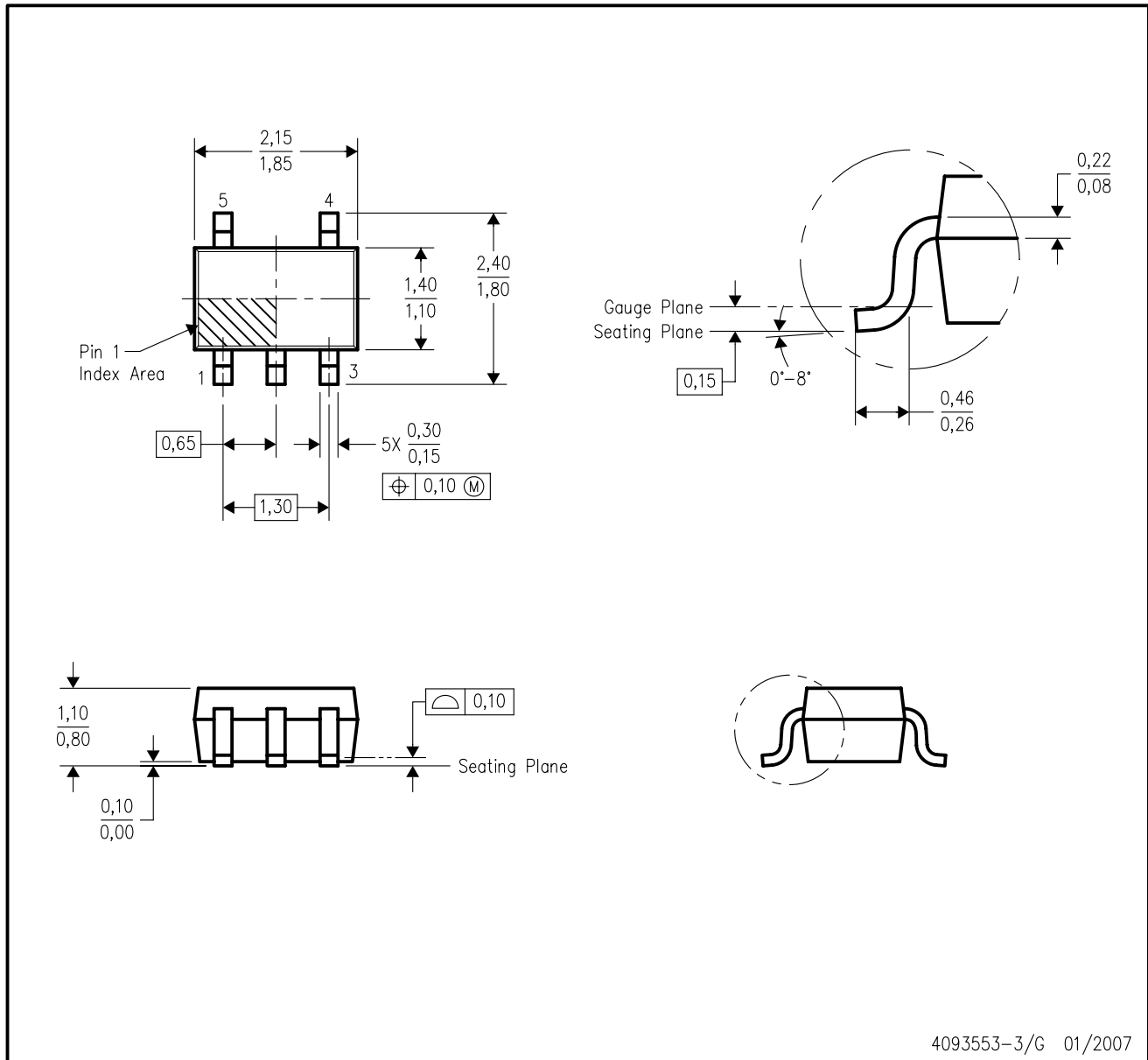
PLASTIC SMALL-OUTLINE PACKAGE



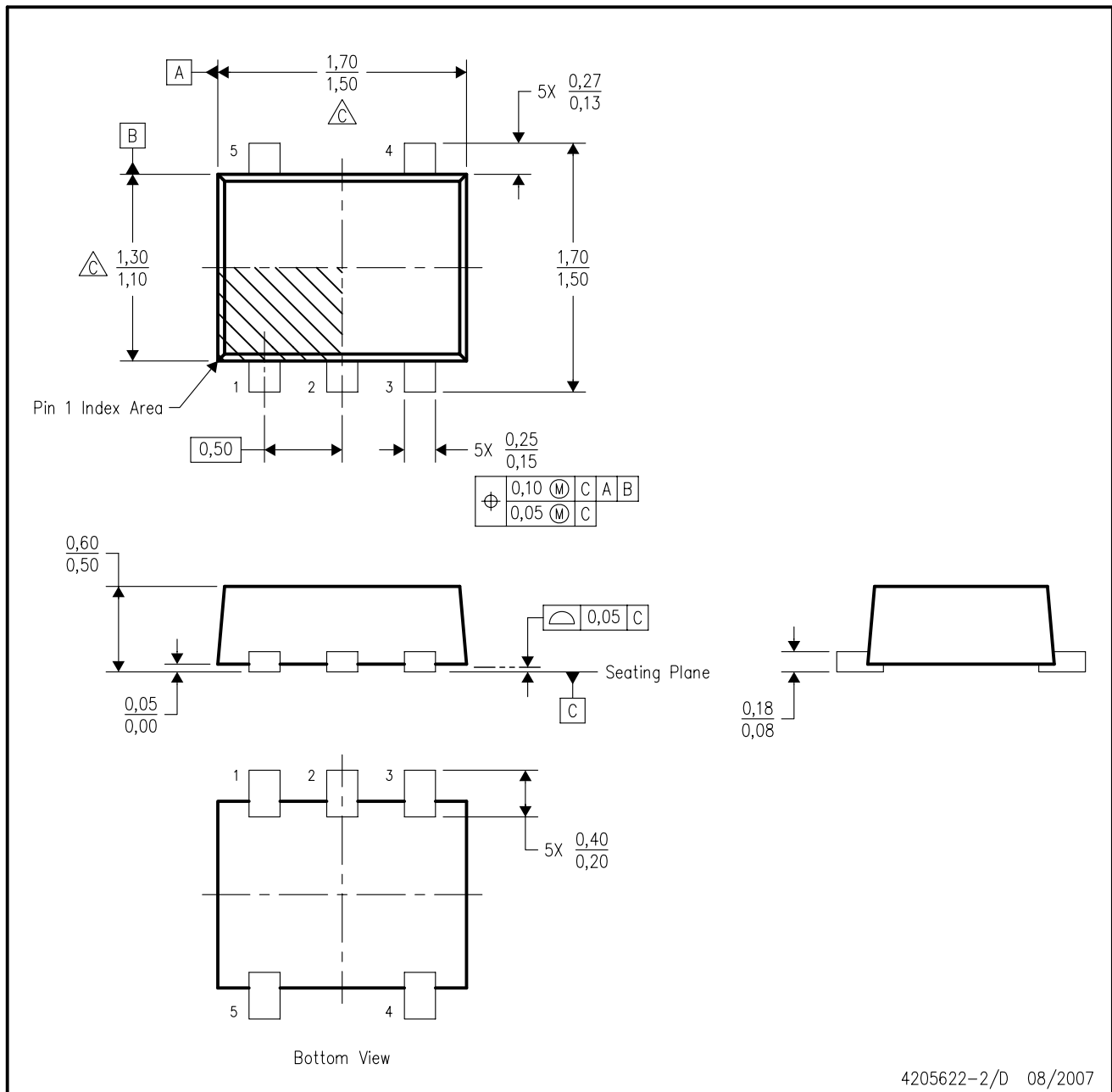
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

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