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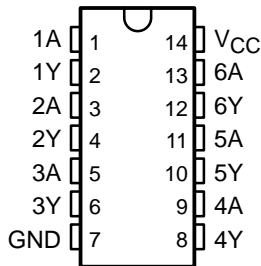
Jameco Part Number 912691

SN54AHC04, SN74AHC04 HEX INVERTERS

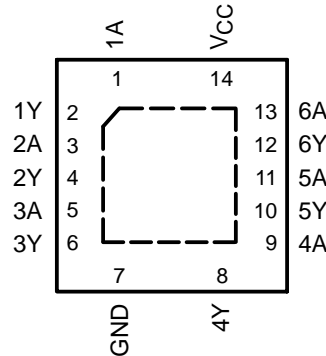
SCLS231M – OCTOBER 1995 – REVISED JULY 2003

- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

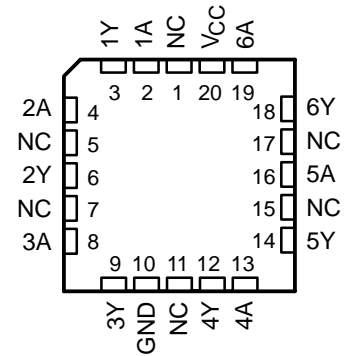
SN54AHC04 . . . J OR W PACKAGE
SN74AHC04 . . . D, DB, DGV, N, NS,
OR PW PACKAGE
(TOP VIEW)



SN74AHC04 . . . RGY PACKAGE
(TOP VIEW)



SN54AHC04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'AHC04 devices contain six independent inverters. These devices perform the Boolean function $Y = \bar{A}$.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74AHC04RGYR	HA04
	PDIP – N	Tube	SN74AHC04N	SN74AHC04N
	SOIC – D	Tube	SN74AHC04D	AHC04
		Tape and reel	SN74AHC04DR	
	SOP – NS	Tape and reel	SN74AHC04NSR	AHC04
	SSOP – DB	Tape and reel	SN74AHC04DBR	HA04
		TSSOP – PW	Tube	SN74AHC04PW
Tape and reel			SN74AHC04PWR	
TVSOP – DGV	Tape and reel	SN74AHC04DGV	HA04	
–55°C to 125°C	CDIP – J	Tube	SNJ54AHC04J	SNJ54AHC04J
	CFP – W	Tube	SNJ54AHC04W	SNJ54AHC04W
	LCCC – FK	Tube	SNJ54AHC04FK	SNJ54AHC04FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54AHC04, SN74AHC04 HEX INVERTERS

SCLS231M – OCTOBER 1995 – REVISED JULY 2003

recommended operating conditions (see Note 4)

		SN54AHC04		SN74AHC04		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5		V
		V _{CC} = 3 V		2.1		
		V _{CC} = 5.5 V		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		V
		V _{CC} = 3 V		0.9		
		V _{CC} = 5.5 V		1.65		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		-50		μA
		V _{CC} = 3.3 V ± 0.3 V		-4		
		V _{CC} = 5 V ± 0.5 V		-8		
I _{OL}	Low-level output current	V _{CC} = 2 V		50		μA
		V _{CC} = 3.3 V ± 0.3 V		4		
		V _{CC} = 5 V ± 0.5 V		8		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V		100		ns/V
		V _{CC} = 5 V ± 0.5 V		20		
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC04		SN74AHC04		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1	0.1	V	
		3 V			0.1		0.1	0.1		
		4.5 V			0.1		0.1	0.1		
	I _{OL} = 4 mA	3 V			0.36		0.5	0.44		
	I _{OL} = 8 mA	4.5 V			0.36		0.5	0.44		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*	±1	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		20	20	μA	
C _i	V _I = V _{CC} or GND	5 V		2	10			10	pF	

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.



SN54AHC04, SN74AHC04 HEX INVERTERS

SCLS231M – OCTOBER 1995 – REVISED JULY 2003

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC04		SN74AHC04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	5*	8.9*	1*	10.5*	1	10.5	ns	
t_{PHL}				5*	8.9*	1*	10.5*	1	10.5		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	7.5	11.4	1	13	1	13	ns	
t_{PHL}				7.5	11.4	1	13	1	13		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC04		SN74AHC04		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.8*	5.5*	1*	6.5*	1	6.5	ns	
t_{PHL}				3.8*	5.5*	1*	6.5*	1	6.5		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.3	7.5	1	8.5	1	8.5	ns	
t_{PHL}				5.3	7.5	1	8.5	1	8.5		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 5)

PARAMETER		SN74AHC04			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.4		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.8		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

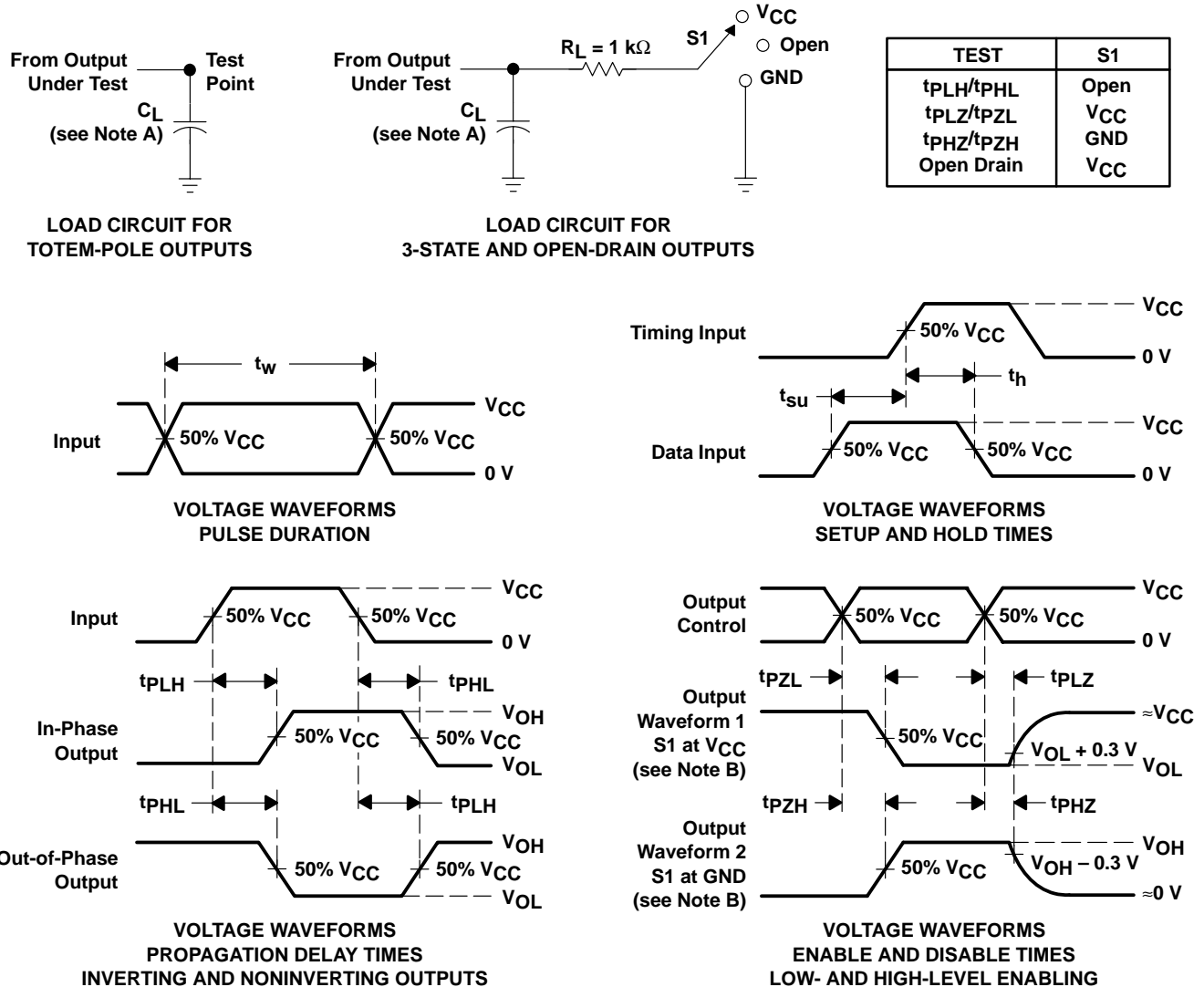
NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	12	pF



PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9680501Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
5962-9680501QCA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
5962-9680501QDA	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC
SN74AHC04D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHC04DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN74AHC04DBR	ACTIVE	SSOP	DB	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHC04DGVR	ACTIVE	TVSOP	DGV	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AHC04DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHC04N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74AHC04NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74AHC04PW	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AHC04PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74AHC04PWR	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AHC04RGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SNJ54AHC04FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54AHC04J	ACTIVE	CDIP	J	14	1	TBD	Call TI	Level-NC-NC-NC
SNJ54AHC04W	ACTIVE	CFP	W	14	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a metal lid.
 D. The terminals are gold plated.
 E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

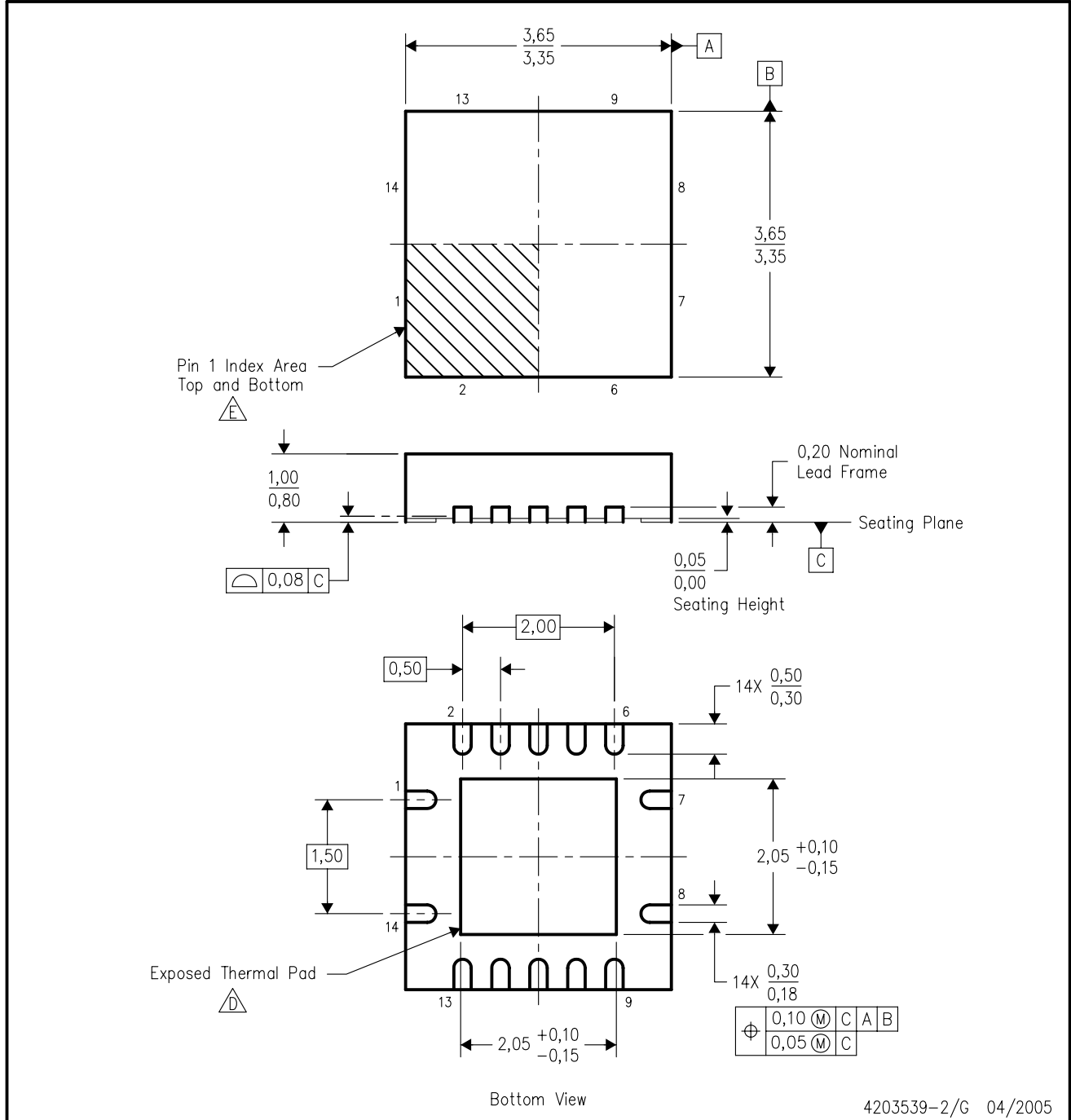
24 PINS SHOWN





- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



4203539-2/G 04/2005

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance.
 -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - F. Package complies to JEDEC MO-241 variation BA.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9680501Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9680501QCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9680501QDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SN74AHC04D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN74AHC04DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04DBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04DGV	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04DGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHC04NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHC04NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74AHC04PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC04RGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74AHC04RGYRG4	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SNJ54AHC04FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54AHC04J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54AHC04W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

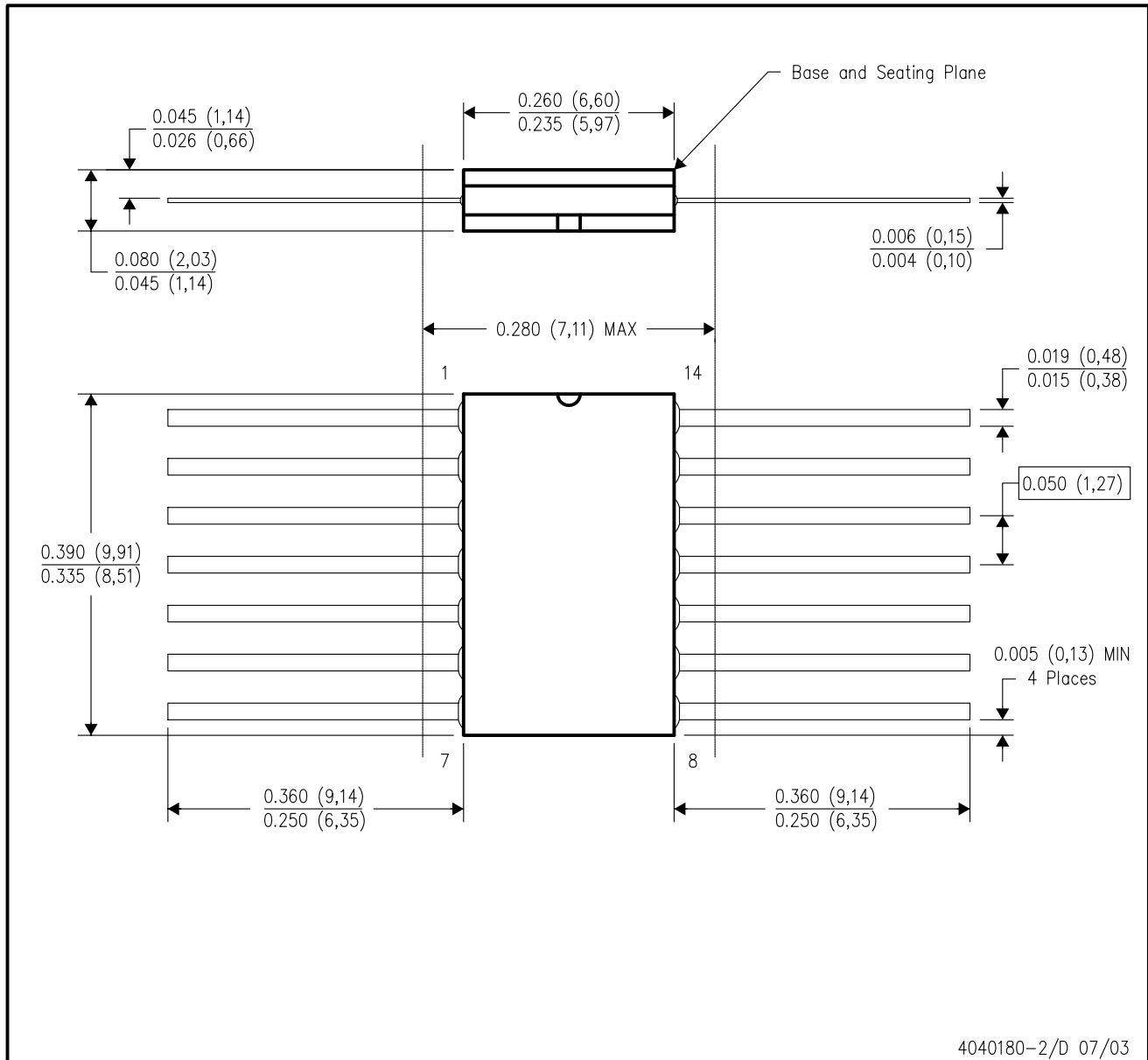
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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W (R-GDFP-F14)

CERAMIC DUAL FLATPACK

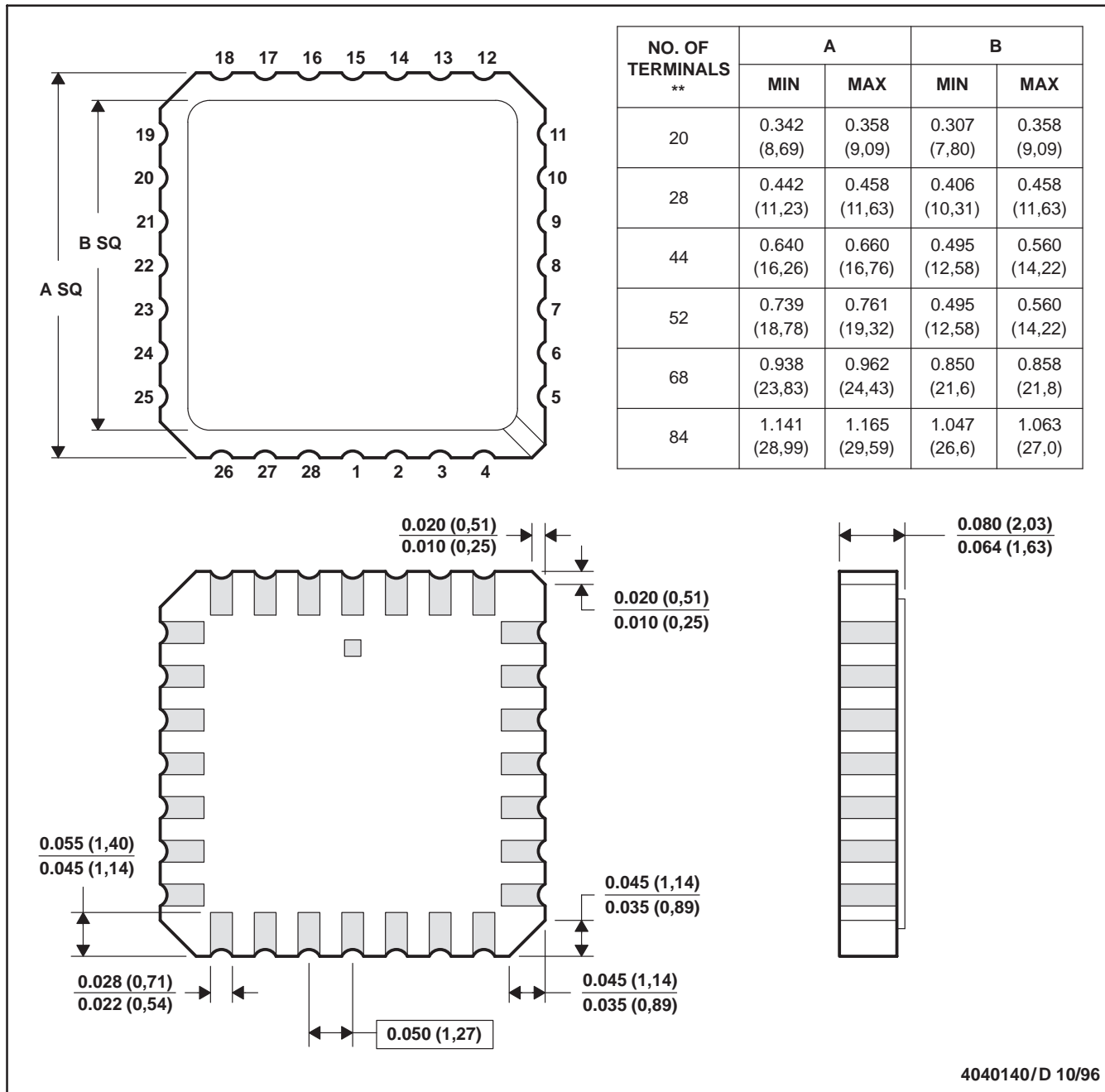


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

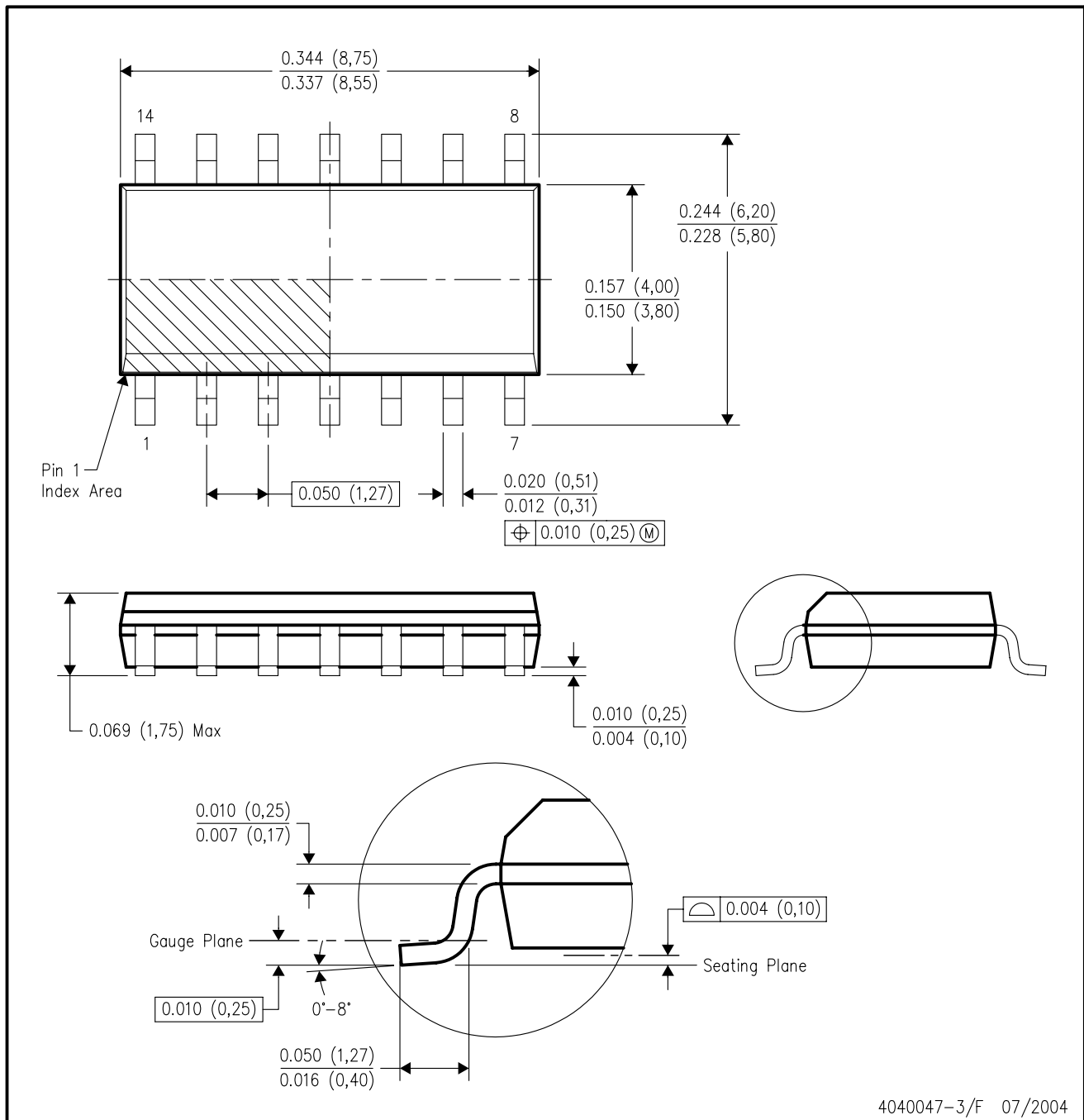


4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

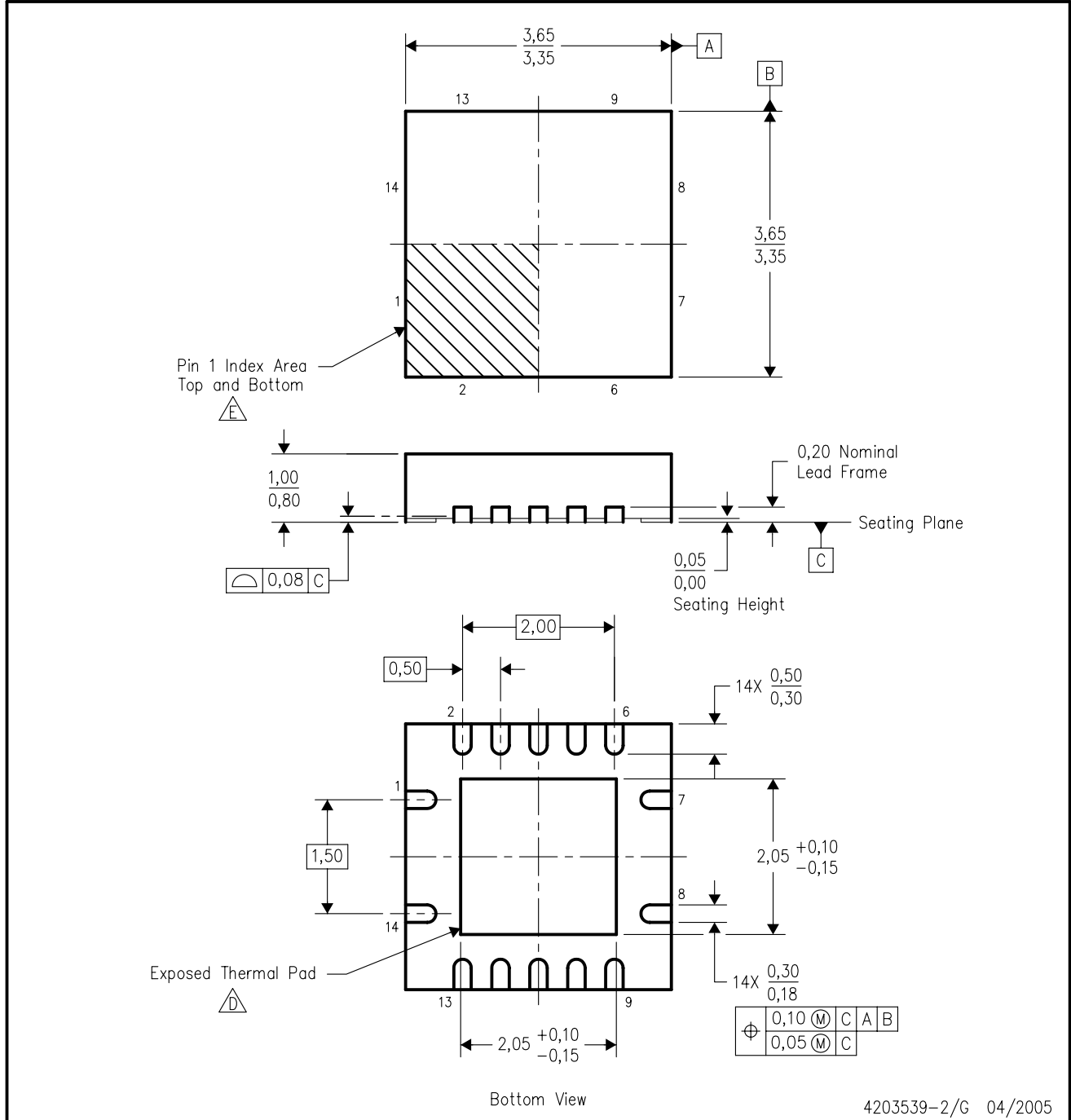
PLASTIC SMALL-OUTLINE PACKAGE





- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



4203539-2/G 04/2005

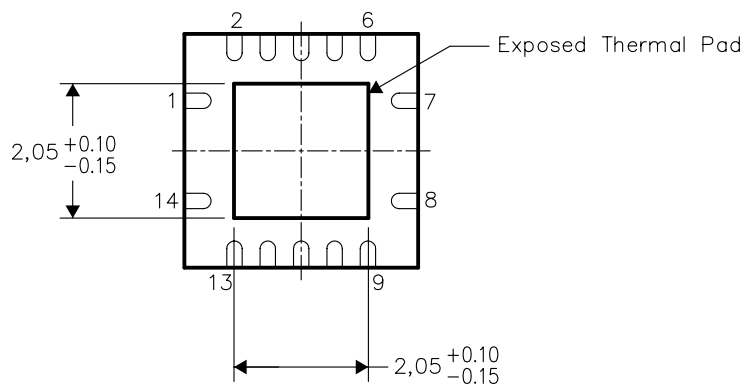
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance.
 -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - F. Package complies to JEDEC MO-241 variation BA.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

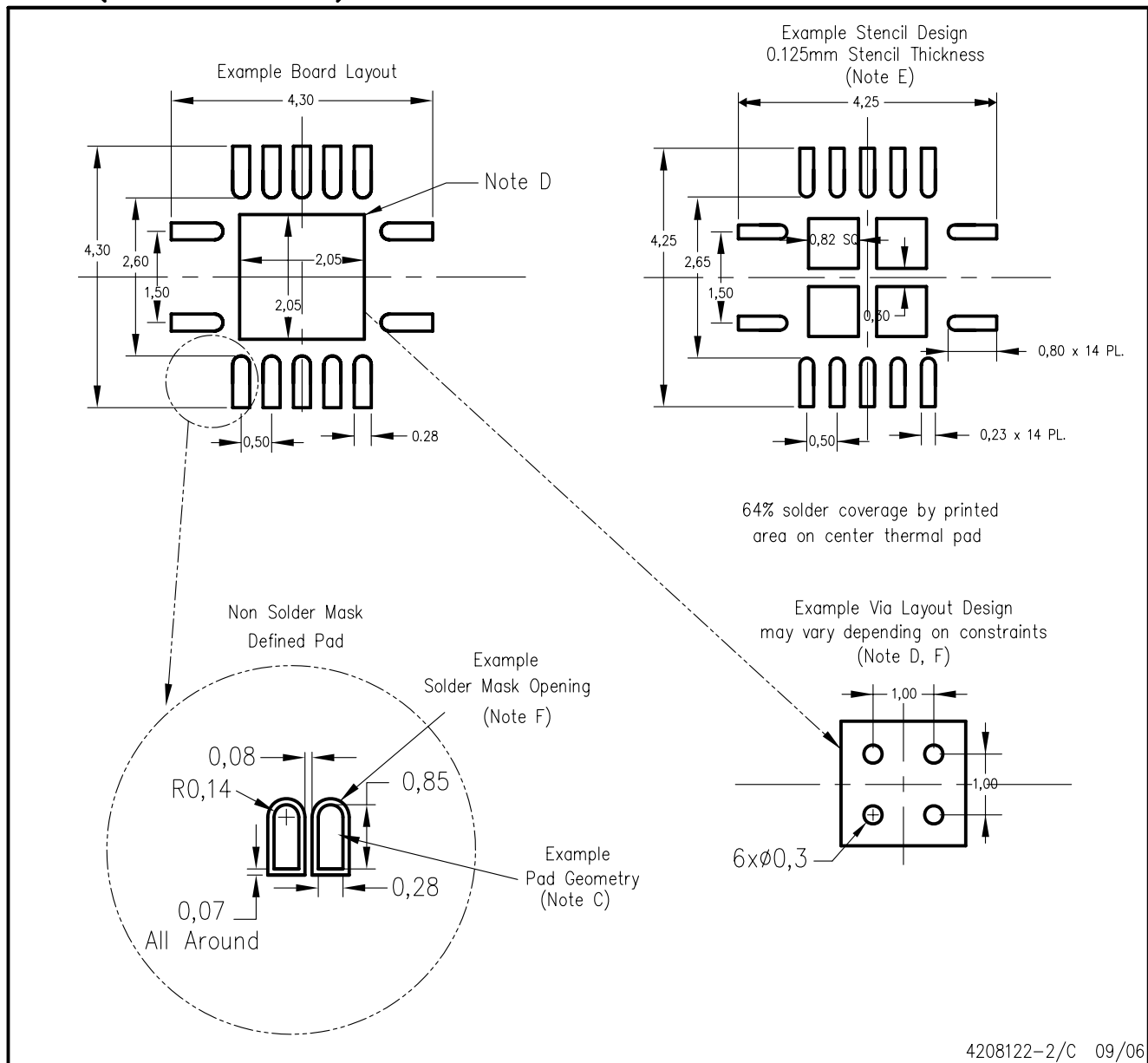


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGY (R-PQFP-N14)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

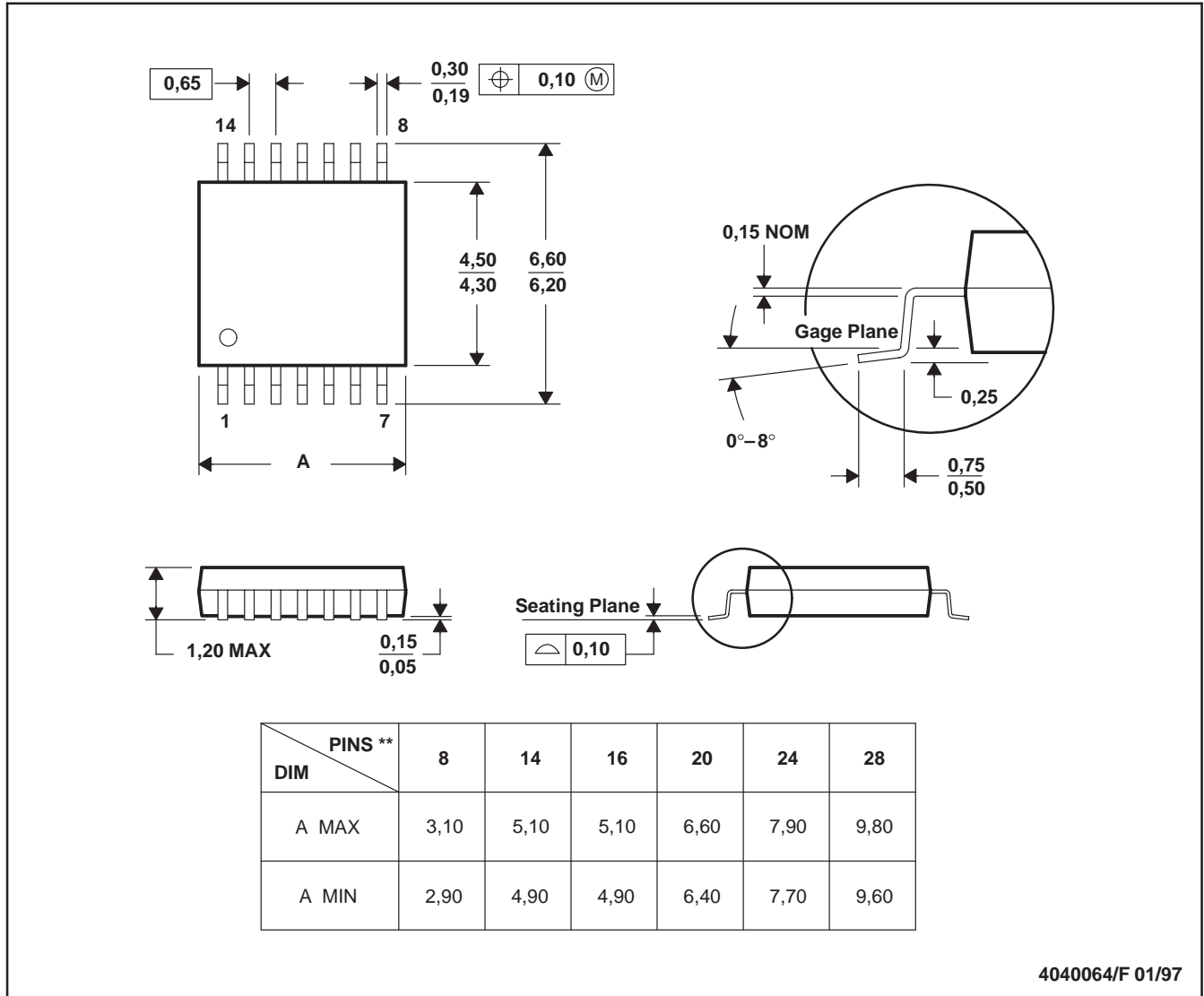


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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